The Development and Characterisation of a Parameterised RSFQ Cell Library for Layout Synthesis

by

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Abstract

The Development and Characterisation of a Parameterised RSFQ Cell Library for Layout Synthesis

L. Schindler
Dissertation: PhD
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Superconductor electronics have shown great promise for interfacing quantum computers to conventional electronics. Several superconductor logic families show potential, but one particular logic family has shown reliable results: Rapid Single Flux Quantum (RSFQ). RSFQ logic implements single SFQ pulses to represent binary data instead of the traditional voltage levels used by semiconductor electronics. RSFQ is so ubiquitous to superconductor digital systems that it serves as the entry to superconductor digital design. Presently, however, the field of RSFQ logic cell design is very exclusive with a small number of physicists and engineers able to design efficient RSFQ cells. This research aims to provide a formalised RSFQ design methodology with education quality circuit theory. Several RSFQ examples are designed, analysed and improved using phase-based circuit equations. Similar to Kirchhoff's current and voltage laws, these phase-based equations can be used to accurately determine the current distribution within a cell. The design methodology for multi-state RSFQ cells is also discussed. Multiple simulation methods confirming cell functionality and operating margins are also presented. The education regarding the design, analysis and implementation of RSFQ cells is vastly expanded through this research which can accelerate the field of quantum circuit design.

RSFQ cells can be connected using a non-storing inductive loop, Josephson transmission lines (JTLs) or, alternatively, superconductor passive transmission lines (PTLs) to bridge longer distances. Signal transmission of SFQ pulses through PTLs and JTLs are analysed and compared. Impedance matching for PTL interconnects to reduce pulse reflection is also investigated.

An example of a portable RSFQ cell library for layout synthesis is developed as part of the IARPA SuperTools program. The challenges of RSFQ cell layouts for the Massachusetts Institute of Technology Lincoln Laboratory (MIT-LL) SFQ5ee fabrication process are discussed. A methodology for establishing a standardised cell layout synthesis is presented. The research contributes to the design and characterisation of track routing architecture for RSFQ on a multilayer fabrication process.

Lastly, methods to test fabricated RSFQ circuits are presented. This includes testing the functionality of individual cells, as well as measuring throughput delays. As the SFQ pulses are only a few picoseconds wide, it is not possible to observe these pulses using conventional measuring equipment. The fabricated tests must therefore be designed in such a way that it is possible to extract meaningful measurements.

Uittreksel

Geparametreerde RSFQ-selbiblioteek vir uitlegsintese: Ontwikkeling en karakterisering

L. Schindler
Proefskrif: PhD
Maart 2021

Tot op hede het supergeleier-elektronika groot belofte getoon vir die koppeling van kwantumrekenaars, aan konvensionele elektronika. Verskeie supergeleierlogika-families toon potensiaal, maar tot dusver toon die "*Rapid Single Flux Quantum*" (RSFQ) logika-familie baie betroubare resultate. In kontras met tradisionele halfgeleier-elektronika, wat spanningsvlakke benut, implementeer RSFQ-logika enkele SFQ-pulse om binêre data voor te stel. RSFQ is so alomteenwoordig vir supergeleier-digitale stelsels dat dit as toegang dien tot digitale supergeleier-ontwerp. Op die oomblik is die veld van RSFQ-logika selontwerp egter baie eksklusief, met slegs 'n handvol fisici en ingenieurs wat RSFQ-selle doeltreffend kan ontwerp. Hierdie navorsing mik om 'n geformaliseerde RSFQ-ontwerpmetodologie te bied tesame met onderwys-kwaliteit RSFQ-teorie. Verskeie RSFQ-selle word ontwerp, geanaliseer en verbeter deur middel van fase-gebaseerde stroombaanvergelykings. Hierdie fase-gebaseerde vergelykings kan gebruik word om die stroomverdeling binne 'n sel, akkuraat te voorspel. Die ontwerpmetodiek vir multi-stadium RSFQ-selle word ook bespreek. Verskeie simulasiemetodes word aangebied om selfunksionaliteit te bevestig. Die navorsing brei uit oor die opleiding rakende die ontwerp, analise en implementering van RSFQ-selle wat verder kan lei tot die versnelling van die kwantumstroomontwerp-veld.

RSFQ-selle kan verbind word met 'n induktiewe lus (wat nie vloed stoor nie), Josephson-transmissielyne (JTL's) of supergeleier-passiewe transmissielyne (PTL's) om langer afstande te oorbrug. Die seinoordrag van SFQ pulse deur PTL's en JTL's word geanaliseer en vergelyk. Impedansie-aanpassing vir PTL-verbindings om pulsrefleksie te verminder, word ook ondersoek.

'n Voorbeeld van 'n draagbare RSFQ-selbiblioteek vir uitlegsintese is ontwikkel as deel van die IARPA SuperTools-program. Die uitdagings vir RSFQ-seluitleg vir die SFQ5ee vervaardigingsproses aan die Massachusetts Institute of Technology Lincoln Laboratory (MIT-LL), word bespreek. 'n Metodiek vir die stigting van 'n gestandaardiseerde seluitlegsintese word aangebied. Die navorsing dra by tot die ontwikkeling en karakterisering van 'n spoorroete-argitektuur vir RSFQ vir 'n multilaag-vervaardigingsproses.

Laastens word metodes aangebied om vervaardigde RSFQ-stroombane te toets. Dit sluit in die toets van die funksionaliteit van individuele selle, asook die meting van deursetvertragings. Aangesien die SFQ-pulse slegs 'n paar piko-sekondes breed is, is dit nie moontlik om hierdie pulse bloot waar te neem deur gebruik te maak van konvensionele meettoerusting nie. Die vervaardigde toetse moet dus so ontwerp word dat dit moontlik is om betekenisvolle metings te onttrek.

Acknowledgements

Firstly, I would like to thank Prof. Coenrad Fourie for guiding me through this journey. Without the multiple conference and research exchange opportunities you provided, this dissertation would not have been possible.

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Chapter 1

Introduction

Rapid Single Flux Quantum (RSFQ) circuits currently hold the most promising interface between classical electronics and quantum computers [1], [2]. Although much work has gone into developing how high-level functional models of RSFQ circuits can be realised [3]–[9], little effort has been done to formalise the education of basic RSFQ logic cell design. RSFQ cells are often published with parameter values, but no indication is given on how these values were calculated. The aim of this research is to provide a formalised design methodology for RSFQ logic cells.

1.1 Motivation

The SuperTools programme [10] was launched by Intelligence Advanced Research Projects Activity (IARPA) in mid-2017 to address the lack of standard open-source tools used for Superconductor Electronics (SCE) development. The SuperTools programme aims to develop tools capable of designing 64-bit reduced instruction set computer (RISC) circuits. This research initially focused on developing a RSFQ cell library for the ColdFlux project [11] within the IARPA SuperTools programme. The cell library was developed using the tools emerging from the ColdFlux project as an additional confirmation of viability and usability for the various tools. Through the development of various RSFQ cells, it became clear that there is currently no widely accepted formalised design methodology for circuits implementing RSFQ logic. Inexperienced circuit designers generally recycle and adjust published circuit templates without understanding why the circuits function as they do. The initial research was therefore expanded to formalise education quality RSFQ logic circuit theory. The education regarding the design, analysis and implementation of RSFQ cells is vastly expanded through this research which can accelerate the field of quantum circuit design.

1.2 Background

1.2.1 A Brief History of RSFQ

The RSFQ logic was first reported on by Likharev and Semenov in 1991 while analysing the failure of a famous IBM research project in the 1980s [12], [13]. The project aimed to develop a prototype Josephson junction computer, but lacked practical logic circuitry. The project implemented the representation of binary logic in terms of DC-voltage; as this method has been successful in the semiconductor industry. The amount of power required to drive the circuit along with the lack of computational speed ultimately caused the project's downfall [12].

The race was then on to find an alternative way to represent binary logic in superconducting circuits. Likharev, Mukhanov and Semenov of the Moscow State University presented the first iteration of single flux quantum (SFQ) logic in 1985 [14]. They announced the implementation of short voltage pulses for the representation of binary data. A binary '1' is represented through a pulse with a quantised area [15]:

$$\int_{t1}^{t2} v(t)\mathrm{d}t = \Phi_0 \simeq 2.07\mathrm{mV}\cdot\mathrm{ps}. \tag{1.1}$$

The lack of an SFQ pulse represents a binary '0'. The use of SFQ pulses meant that superconductor circuits could be realised with faster operating speeds and lower power consumption compared to traditional semiconductor electronics. The accelerated operating speed attributed to the logic being dubbed *rapid* single flux quantum.

Other technologies such as energy-efficient RSFQ (ERSFQ) [16] and Adiabatic Quantum Flux Parametron (AQFP) [17] have been developed as a result of the SFQ logic breakthrough in [12].

1.2.2 The Josephson junction and the Josephson effect

A Josephson junction (JJ) is a device which consists of two superconductors separated by a thin barrier. We will consider superconductor-isolation-superconductor (SIS) tunnel junctions for this research. A 3D TCAD rendering for a JJ is shown in Fig. 1.1. The isolation is stretched within the render as the isolation layer is only a few nanometres thick. The electrical symbol for a JJ is shown in Fig. 1.2.

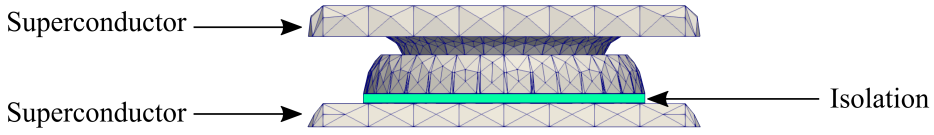


Figure 1.1: 3D TCAD Josephson junction render.

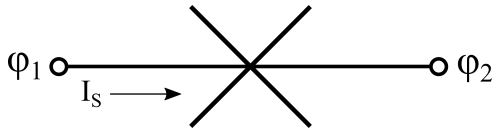
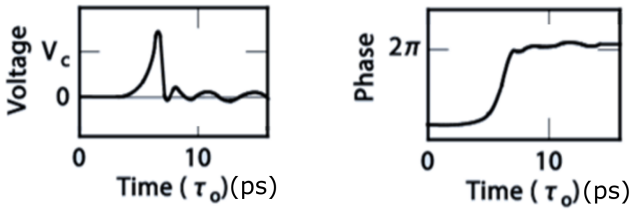


Figure 1.2: Symbol for a Josephson junction.

The DC Josephson effect states that a supercurrent will flow through the JJ in the absence of an external electromagnetic field through superconductive tunnelling [18]. This supercurrent through the JJ can be described through:

$$I_S = I_C \sin \varphi, \tag{1.2}$$

where I_c is the critical current and $\varphi = \varphi_1 - \varphi_2$ and represents the phase difference over the junction as shown in Fig. 1.2. The critical current refers to the maximum amount of current which can flow through the junction before the junction undergoes a 2π phase shift. When a junction undergoes a 2π phase shift, it generates and SFQ pulse as shown in Fig. 1.3. This 2π phase shift is typically referred to as the switching of a junction.



(a) (b)

Figure 1.3: (a) SFQ pulse generated by junction with (b) associated 2π junction phase shift. Figure adapted from [12].

1.2.3 RSFQ building blocks

RSFQ circuits utilise the transfer and storage of SFQ pulses to represent binary logic. RSFQ logic cells can be constructed using three basic RSFQ building blocks [19] shown in Fig. 1.4. Each block consists of inductor, JJ and bias current source elements.

- The transfer block transfers an SFQ pulse from one physical location to another. To achieve this, the value for the inductor is set as $L \sim \Phi_0/2I_c$ where I_c is the critical current of the JJ.
- The storage block stores an SFQ pulse within a junction-inductor loop. This is achieved through setting the inductor value as $L \sim \Phi_0/I_c$.
- The decision block is implemented through two JJs with different I_c values to control whether a SFQ pulse is transmitted or not. The typical relation between the critical currents of the two JJs is $I_{c2} = \sqrt{2}I_{c1} \approx 1.4I_{c1}$ [12].

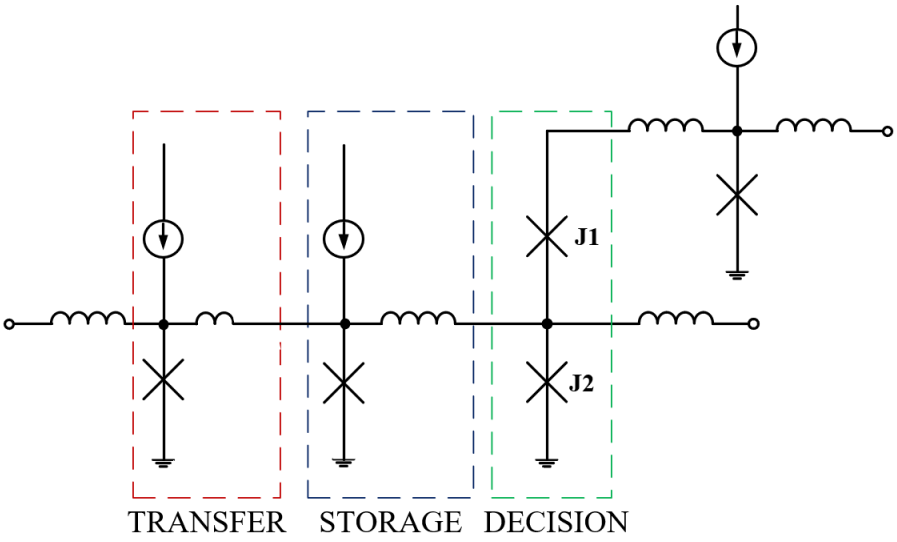


Figure 1.4: Schematic of different RSFQ building blocks.

1.2.4 Signal propagation

Josephson transmission lines (JTLs) or passive transmission lines (PTLs) are two methods used to propagate SFQ pulses between RSFQ circuits.

A JTL is the most basic cell in RSFQ logic [12]. JTLs are constructed by connecting several biased JJs with inductors as described in the transfer block in Chapter 1.2.3. JTLs provide pulse transmission without pulse reflections, but also increased power consumption. The probability of timing errors also increases with increased JTL length due to jitter [20]. JTLs also require a much larger routing space than PTLs.

PTLs for superconductor integrated circuits can be constructed using microstrip or stripline geometries. The cross-section for these PTL geometries are compared in Fig. 1.5. PTLs provide high-speed pulse propagation and very low power dissipation [21], but pulse reflections due to impedance mismatch can affect the operating margins of a circuit [22], [23]. For this research, PTLs implementing the stripline geometry is considered for SFQ pulse propagation.

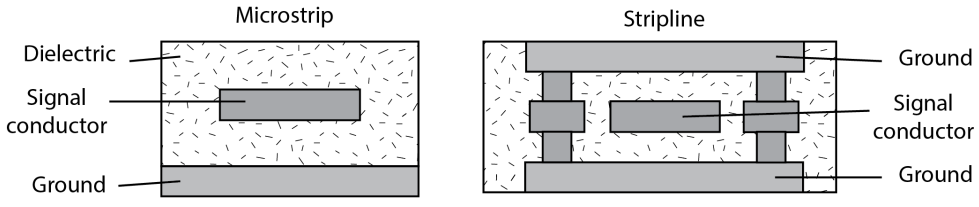


Figure 1.5: Cross-section of typical thin-film passive transmission line geometries in superconductor integrated circuits for microstrip and stripline. Figure from [24].

1.2.5 Basic RSFQ design flow

The basic design flow for RSFQ circuits up to impedance extraction using InductEx [25], [26] is described in Fig. 1.6.

The circuit schematic can be set up using both commercial and open source schematic capture software. Two open source tools which support the JJ as a native element are XIC [27] and the gEDA package [28]. Both of these tools can be used to extract the circuit netlist from the captured schematic. XIC also serves as a graphical interface for the WRspice circuit simulator [29]. Although XIC is not as intuitive to use as gEDA, it provides an all-in-one design environment for circuit designers. Cell layout can also be done in XIC. The layout can also be linked to the circuit schematic for ease of reference. A major setback is that XIC becomes exponentially slower the larger a circuit becomes.

For more experienced circuit designers, a circuit netlist is often set up directly from the core cell diagram. A Spice engine, such as JoSIM [30], JSIM [31] or PSCAN2 [32], is then used to simulate the circuit functionality. A major advantage of JoSIM is that it supports phase-based simulation as well as a speed increase when compared to JSIM [33].

Many margin analysis and optimiser techniques have been published over the years, but few lead to tools for wider use [34]. For this research, the JoSIM-tools library [35] is used for both the margin analysis and circuit optimiser as it is the in-house tool linked with JoSIM.

Popular cell layouts editors include open source projects such as XIC, KLayout [36], LASI [37] and commercial editors such as LayoutEditor [38], Cadence Virtuoso [39] and AutoCAD [40]. KLayout provides an integrated scripting tool for design rule checking (DRC) which was used for this research.

InductEx is used to verify that the inductances found in the cell layout correlates to the intended design value. Other tools are available, but InductEx is presently the most versatile inductance extraction tool [34]. If a cell layout has to be adjusted to correct impedance values, the layout once again undergoes DRC.

A final step in the design flow is layout-versus-schematic (LVS) verification. LVS is used to compare the physical layout of a cell with a circuit schematic. Cadence provides an LVS implementation, but as this is commercial software and no open-source LVS tools have been reported to date [34], LVS is omitted from the design flow in Fig. 1.6.

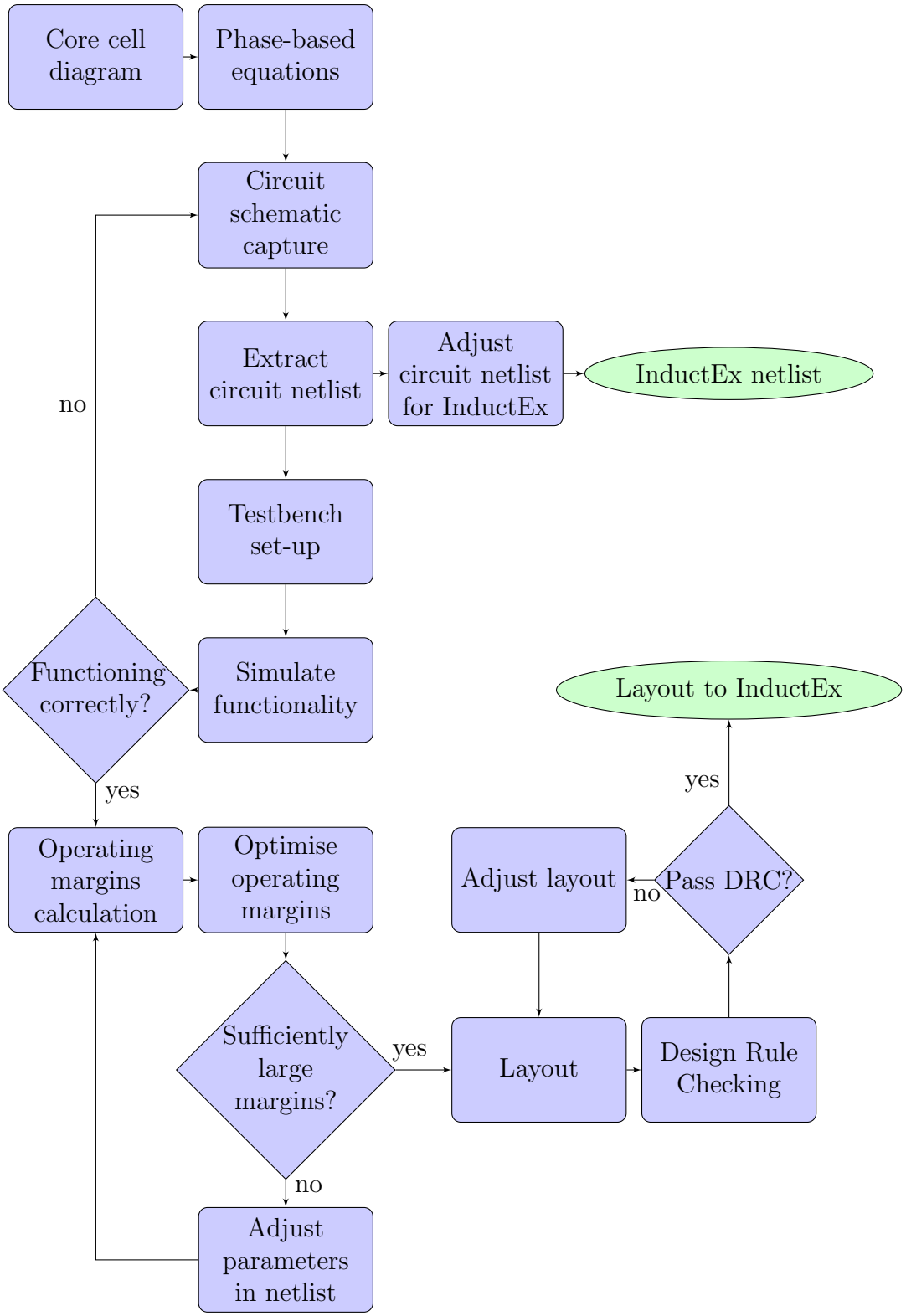


Figure 1.6: Flow diagram of RSFQ cell design up to InductEx extraction.

1.3 Objectives of Dissertation

1.3.1 Objectives

The lack of formalised RSFQ circuit design theory presents the opportunity to establish education quality RSFQ cell design procedures. The use of phase-based circuit equations presents a method to design complex RSFQ circuits from first principles. Although experienced RSFQ circuit designers intuitively consider phase when designing circuits, formalising the design theory provides inexperienced designers with the tools required to design RSFQ circuits which function as intended.

The viability of designing RSFQ cells using phase-based equations should also be evaluated. The design of an RSFQ cell library provides a comprehensive study on the application of phase-based equations for RSFQ cell design.

This dissertation reports on the objectives summarised as:

1. The investigation of how phase change within an RSFQ circuit affects the current distribution.
2. Analysing how the current distribution within an RSFQ circuit affects the operating margins.
3. Formalising education quality circuit design theory for RSFQ logic.
4. Implementing the formalised RSFQ design theory to construct a functional RSFQ cell library.
5. Investigate how SFQ pulse transmission using PTLs affect RSFQ circuits.
6. Fabricate and test the constructed RSFQ cell library to verify that the formalised RSFQ design theory is viable.

1.3.2 Document Layout

Chapter 2 presents the formalisation of RSFQ circuit design theory through the use of phase-based equations. The chapter also discusses how well-known techniques, such as Kirchhoff's voltage and current laws can be adapted for superconductor circuits. The analysis of current distribution within RSFQ circuits using these phase-based equations is also included. Techniques to adapt the phase-based circuit equations to improve operating margins are also presented. The chapter provides multiple RSFQ cell design examples to discuss the complete design flow for RSFQ cells up to physical cell layout.

Passive transmission lines and the influence of impedance mismatch caused by PTL connections are discussed in Chapter 3. SFQ pulse reflection is investigated along with methods to minimise these reflections.

Chapter 4 presents the development of an RSFQ cell library for layout synthesis. The use of a multilayer fabrication process for the layout of RSFQ cells is presented. A layout track block is also presented to establish a standardised layout template for a multilayer fabrication process.

Chapter 5 presents multiple chip designs submitted for fabrication. Some preliminary measured results are also included.

The research is concluded in Chapter 6.

Appendix A contains an unpublished journal article "*Cell Design Methodology and Circuit Theory of RSFQ Logic*" in which the formalisation of RSFQ cell design is presented. The article is a result of work done in Chapter 2.

Appendix B contains a published article "*Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells*" [24]. In this article, the effect of SFQ pulse reflections are investigated and possible solutions to improve impedance mismatching is presented.

Appendix C contains a published article "*Design and Characterisation of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process*" [41]. The article includes work presented in Chapter 4.

Appendix D contains a published conference article "*Standard Cell Layout Synthesis for Row-Based Placement and Routing of RSFQ and AQFP Logic Families*" [42] in which a layout synthesis tool is presented. The layout requirements for RSFQ and AFQP logic cells to implement standardised layouts for a multilayer fabrication process are discussed.

Appendix E contains a comprehensive study regarding the phase-based equations for the RSFQ cells designed in Chapter 2. The effect of phase change within multi-state cells is also investigated.

Appendix F provides comprehensive current distribution simulation results for the RSFQ cells designed in Chapter 2.

Appendix G contains the margin analysis results for the RSFQ cells designed in Chapter 2.

Appendix H contains the test manual for the SUMLL01-MRC chip. The test manual is used as a reference when testing the fabricated SUMLL01-MRC chip. The required measurements to verify circuit functionality is also presented within the test manual.

Appendix I contains the test manual for the SUMLL02-MRC chip. The test manual is used as a reference when testing the fabricated SUMLL02-MRC chip. The required measurements to verify circuit functionality is also presented within the test manual.

Appendix J contains the test manual for the SUMLL03 chip. The test manual is used as a reference when testing the fabricated SUMLL03 chip. The required measurements to verify circuit functionality is also presented within the test manual.

Appendix K presents the user manual for the RSFQ cell library presented in Chapter 4. The manual contains comprehensive information regarding the functionality, layout and power dissipation of the RSFQ cell library.

Chapter 2

RSFQ Circuit Design Through Phase-Based Equations

The theory and design methodology discussed within this chapter was presented as oral presentations during EUCAS 2019 [43] and ISS 2020 [44]. An article regarding this work was also submitted for publication [45] and is included in Appendix A.

2.1 Introduction

This chapter aims to formalise the theory and design methodology for RSFQ logic circuits. The design methodology for basic CMOS circuits is discussed and an equivalent technique for RSFQ logic is investigated. A generic RSFQ cell library is developed using this equivalent design methodology. The circuits within this chapter are not designed to be connected using PTLs in an aim to decrease the complexity of the design.

The techniques commonly used to design and analyse semiconductor circuits are discussed within Section 2.2. The adaptation of these design techniques for RSFQ circuits and the implementation of Newton's Method for RSFQ circuit analysis is discussed in Section 2.3. Section 2.4 introduces a generic RSFQ cell library designed using phase-based equations. The fundamental methodology for designing RSFQ circuits is demonstrated through the design of a JTL within Section 2.4.1. Section 2.4.2 introduces the concept of multiple branches within an RSFQ circuit. Designing circuits using a decision pair of Josephson junctions are discussed in Section 2.4.3. The implications of designing an RSFQ cell with two states are discussed in Section 2.4.4 through the design of a DFF. The simulation of multiple states using JoSIM and the importance of phase sources within a simulation engine is also introduced within the DFF design example. Section 2.4.5 introduces the OR2 cell as an example to analyse operating margins of RSFQ cells. Methods to improve operating margins are also investigated. The RSFQ XOR cell, in Section 2.4.6, is used as an example to discuss the design methodology for a cell with multiple set states. The concept of yield analysis and a yield roll-off curve is also introduced. The concept of digital simulation is introduced in Section 2.4.7 through the AND2 example cell. The NOT cell designed introduced in Section 2.4.8 shows a more complex design of an RSFQ cell. The complete design process to develop an RSFQ cell ready for layout is discussed in Section 2.4.9 through the design of an NDRO cell.

2.2 CMOS circuits

Complementary metal–oxide–semiconductor (CMOS) technology makes use of semiconducting components to construct analogue and digital circuits. Transistors can be used to design various logic elements such as the R-S flip-flop example shown in Fig. 2.1. Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) are two methods used to design and analyse circuits. Referring to Fig. 2.1, the following equations can be established using KCL and KVL:

$$i_a = i_b + i_c$$

and

$$V_{DD} = v_1 + v_2 + v_3$$

Similar equations can be constructed to find the current distribution through each element within the circuit.

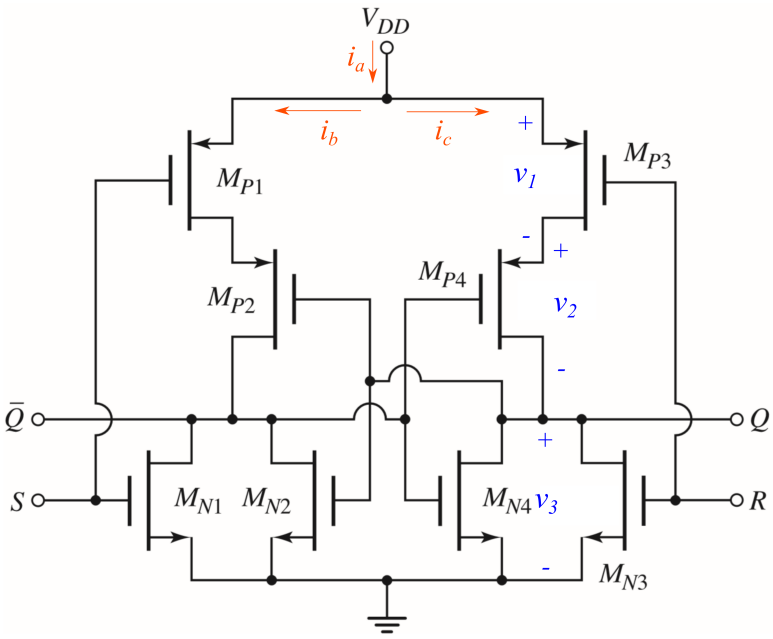


Figure 2.1: CMOS R-S flip-flop adapted from Figure 16.64 in [46].

2.3 RSFQ Circuit Design Methodology

The aim of this work is to develop a circuit analysis method for RSFQ circuits using either a KCL or KVL equivalent. For this, the circuit elements must be described in terms of the current flowing through the element or the voltage difference over the element. The basic RSFQ circuit elements are JJs, inductors and current sources. The influence of shunt resistors for DC analysis is negligible as current will always flow through a superconductor instead of a resistive material.

Once all the circuit elements are described in terms of the current through the element or the voltage over the element, KCL or KVL can be used to construct circuit equations. If the number of unknowns match the number of circuit equations, Newton's Method can be used to solve the values of the unknowns, also known as the root values. Newton's

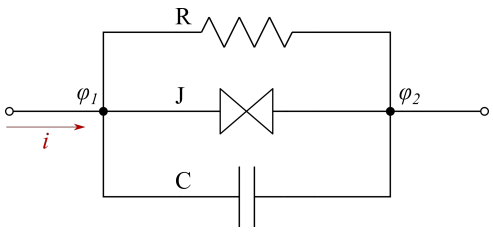


Figure 2.2: Current through RCSJ model adapted from [47].

Method is a mathematical algorithm used to iteratively approximate the root values of a function set. An initial guess is required for the root values. The next root value guess is then calculated through:

$$\mathbf{x_{n+1}} = \mathbf{x_n} - \mathbf{J}(\mathbf{x_n})^{-1}\mathbf{f}(\mathbf{x_n}) \tag{2.1}$$

where $\mathbf{x_n}$ is the initial or previous guess, $\mathbf{f}(\mathbf{x_n})$ is the function set, $\mathbf{J}(\mathbf{x_n})$ is the pseudo-inverse Jacobian of $\mathbf{f}(\mathbf{x_n})$ and n is the number of iterations completed. The restrictions and special cases of Newton's Method are widely available in literature. A script was developed by assuming that a non-singular and non-zero $\mathbf{J}(\mathbf{x_n})$ can be constructed through the circuit equations.

2.3.1 Phase-based Josephson junction model

Various models have been developed to model the Josephson junction (JJ). A popular model is the RCSJ model [47], shown in Fig. 2.2, which models the JJ as inductor in parallel with a capacitor and resistor. The RCSJ model is sufficient for modelling critically damped superconductor-insulator-superconductor (SIS) tunnel junctions used in various fabrication processes. The current through a Josephson junction, according to the RCSJ model, is described through [48]:

$$i = I_c \sin\varphi + \frac{v}{R} + C\frac{dv}{dt} \tag{2.2}$$

where I_c is the critical current of the junction, φ is the phase difference over the junction, $\varphi = \varphi_2 - \varphi_1$, and R and C the internal junction resistance and capacitance, respectively. The Josephson phase-voltage relation is defined through [12]:

$$v = \left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt} \tag{2.3}$$

We can combine (2.2) and (2.3) to describe the current through a JJ in terms of the phase:

$$i = I_c \sin\varphi + \left(\frac{1}{R}\right)\left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt} + C\left(\frac{\Phi_0}{2\pi}\right)\frac{d^2\varphi}{dt^2} \tag{2.4}$$

For a DC analysis, $d\varphi/dt = 0$ can be assumed. Therefore (2.4) can be reduced to represent the DC current through a JJ in terms of phase as:

$$i = I_c \sin\varphi \tag{2.5}$$

The switching of a JJ occurs when $i > I_c$. The current through the JJ, while switching occurs, is described through (2.4) and causes a 2π phase shift over the JJ, as shown in Fig. 2.3. Once the 2π phase shift has occurred, $d\varphi/dt = 0$ regains validity and the current through the JJ subsides back to (2.5). The following definitions are formalised, with reference to Fig. 2.3, for a phase shift observed during circuit analysis:

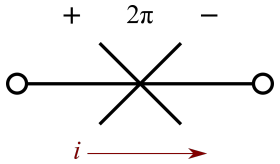


Figure 2.3: Definition of 2π phase shift for a switching JJ.

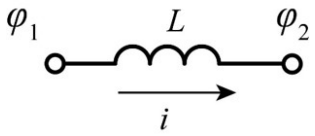


Figure 2.4: Current through inductor in terms of phase difference over inductor.

- If the current is taken in the positive i direction, a $+2\pi$ phase shift is observed.
- If the current is taken in the negative i direction, a -2π phase shift is observed.

2.3.2 Phase-based inductor model

The RCSJ model, shown in Fig. 2.2, considers the JJ as a junction shunted with a resistor and capacitor. In this model, the junction is described through an inductance [47]. Therefore the phase-voltage relation over an inductor for DC analysis can be also characterised through (2.3). The voltage over an inductor can be described through:

$$v = L\frac{di}{dt} \tag{2.6}$$

Combining (2.3) and (2.6), a relation between phase difference over an inductor and current through an inductor can be established:

$$\left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt} = L\frac{di}{dt} \tag{2.7}$$

Thus the current through an inductor in terms of phase, shown in Fig. 2.4, is derived as:

$$i = \varphi\left(\frac{\Phi_0}{2\pi L}\right) \tag{2.8}$$

where $\varphi = \varphi_2 - \varphi_1$. If $\varphi_1 \neq \varphi_2$, then current will flow through the inductor and no current will flow through the inductor if $\varphi_1 = \varphi_2$.

A summary of the phase-based component models are presented in Table 2.1.

Table 2.1: Summary of phase-based component models

Component	Phase-based model
Josephson junction	$\varphi = \arcsin\left(i/I_c\right)$
Inductor	$\varphi = iL\left(2\pi/\Phi_0\right)$

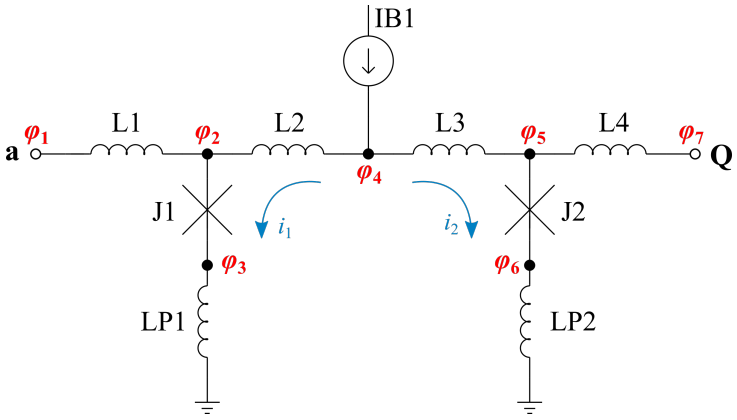


Figure 2.5: Schematic of RSFQ JTL.

2.4 Introduction to the generic cell library

A cell library is a collection of standard circuits performing either a logic or storage function. These circuits are characterised by design specifications of the process technology. This section discusses the design methodology for a generic RSFQ cell library based on circuits developed by Likharev and Semenov [12] and the ADP2 CONNECT library [49], [50]. The generic cell library discussed in this chapter includes the following core cells:

- Interconnects: JTL, SPLIT and MERGE.
- Buffers: DFF and NDRO.
- Logic cells: OR2, XOR, AND2 and NOT.

The '2' within OR2 and AND2 indicates that the cell has two signal input ports. JoSIM is used to simulate the current distribution within circuits along with circuit functionality. The JJs components are modelled for the MIT-LL SFQ5ee process during simulation, but the methods discussed can also be applied to other fabrication processes.

2.4.1 JTL

- This section introduces the fundamental idea for analysing an RSFQ circuit using phase-based equations.

The Josephson transmission line, JTL, is commonly used to propagate SFQ pulses within a larger circuit. The JTL can also be used to delay an SFQ pulse to adhere to timing constraints within a larger circuit. Commonly, two identical JJs are used to form the transmission line, but different configurations regarding amount of JJs and varying JJ sizes do exist.

The schematic for the JTL used in this analysis is shown in Fig. 2.5 with the input pin at φ_1 and the output pin at φ_7. The JJs are designed to be identical in size and the inductors L_1 to L_4 are designed to transmit the SFQ pulse. The design values for the RSFQ JTL is shown in Table 2.2.

The designed RSFQ JTL is load-dependent when designed to be connected directly to other cells. If the connecting loads are not balanced, current leakage can occur on L_1 and L_4. The effects of current leakage and the importance of load balancing is discussed in

Table 2.2: Parameter design values for RSFQ JTL cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	I_c
B_{CC}	Bias current coefficient	-
I_{B1}	Bias current source 1	$2I_cB_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(4I_c)$
$L3$	Inductor 3	$\Phi_0/(4I_c)$
$L4$	Inductor 4	$\Phi_0/(4I_c)$

Section 2.5. The derivation of phase-based equations assumes that the connecting loads are balanced. This infers that:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_5 is equal to the phase at φ_7 so that no current flows through L_4.

The load balancing assumption leads to the ability to analyse the JTL in isolation as no external currents are present within the circuit. Kirchhoff's current law (KCL) is now evaluated at φ_4:

$$I_{B1} = i_1 + i_2 \tag{2.9}$$

The bias current source value and all inductor and JJ values are known if I_c and B_{CC} are known. Thus the only unknown variables are i_1 and i_2. Consequently, two equations describing the current distribution within the JTL are required to solve the two unknown variables using Newton's Method. The phase at φ_4 evaluated:

$$\varphi_4 = \left(\frac{2\pi}{\Phi_0}\right) L_2 i_1 + \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right) L_{p1} i_1 \tag{2.10}$$

and

$$\varphi_4 = \left(\frac{2\pi}{\Phi_0}\right) L_3 i_2 + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right) L_{p2} i_2 \tag{2.11}$$

Combining (2.10) and (2.11), the phase loop through L_{p1}-J_1-L_2-L_3-J_2-L_{p2} can be expressed as the following function:

$$f(\boldsymbol{i}) = \left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1 - L_2 i_1 + L_3 i_2 + L_{p2} i_2) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \tag{2.12}$$

Rearranging (2.9), we derive the second function representing the current distribution within the JTL cell:

$$g(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.13}$$

The design values for this example is chosen as $I_c = 250\ u\text{A}$ and $B_{CC} = 0.7$. Newton's Method is implemented to solve the two unknown current values described in (2.12) and (2.13). The JTL is also simulated and the relevant current values extracted using

Table 2.3: Comparison between calculated and simulated values for the RSFQ JTL circuit.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	175.00	175.000000000009	−5.14E-12 %
i_2	175.00	174.999999999991	5.14E-12 %

JoSIM [30]. Table 2.3 shows the comparison between the calculated values of the current distribution and the applicable simulated values. It is seen that the difference between the calculated and simulated values are insignificant. The difference might not be as a result of an error but could also be caused by different means of rounding between theoretical values and the way that values are interpreted by the simulator. A difference smaller than 1E-6 (or 1E-4 %) can therefore be considered negligible going forward.

Circuit verification

The functionality of the designed RSFQ JTL must now be confirmed. The functionality of the JTL is evaluated by connecting a phase source at the input port **a**, φ_1 in Fig. 2.5. An additional junction with a bias current source set to $I_B = 0.7I_c$ is connected to **Q** to function as a load circuit. The amplitude of the phase source is increased with 2π to replicate the phase change when an SFQ pulse arrives at **a**. The simulation investigates the behaviour of the JTL when multiple pulses are received. The simulation results are shown in Fig. 2.6. The JTL is also run through TimEx to extract the time delay between the input and output of the JTL. This is also known as the $a \rightarrow q$ delay and is extracted as 3.5 ps for the designed RSFQ JTL. This delay is observed through the vertical dotted line in Fig. 2.6. The $a \rightarrow q$ delay can be reduced by increasing the bias current source value, decreasing the inductor values, decreasing the size of the JJs or a combination of the three adjustments. The $a \rightarrow q$ delay can also be increased if a larger delay is required.

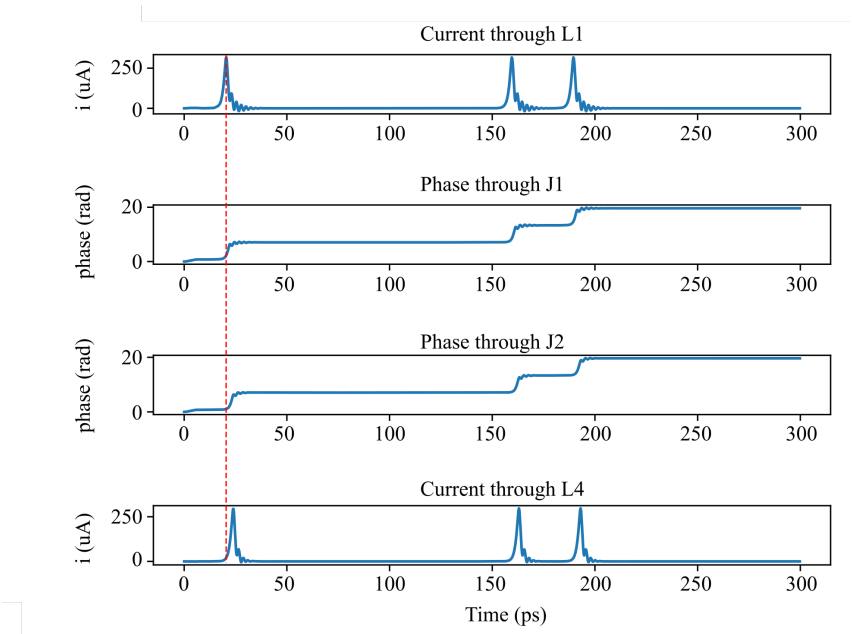


Figure 2.6: Simulation results showing the functionality of the designed RSFQ JTL.

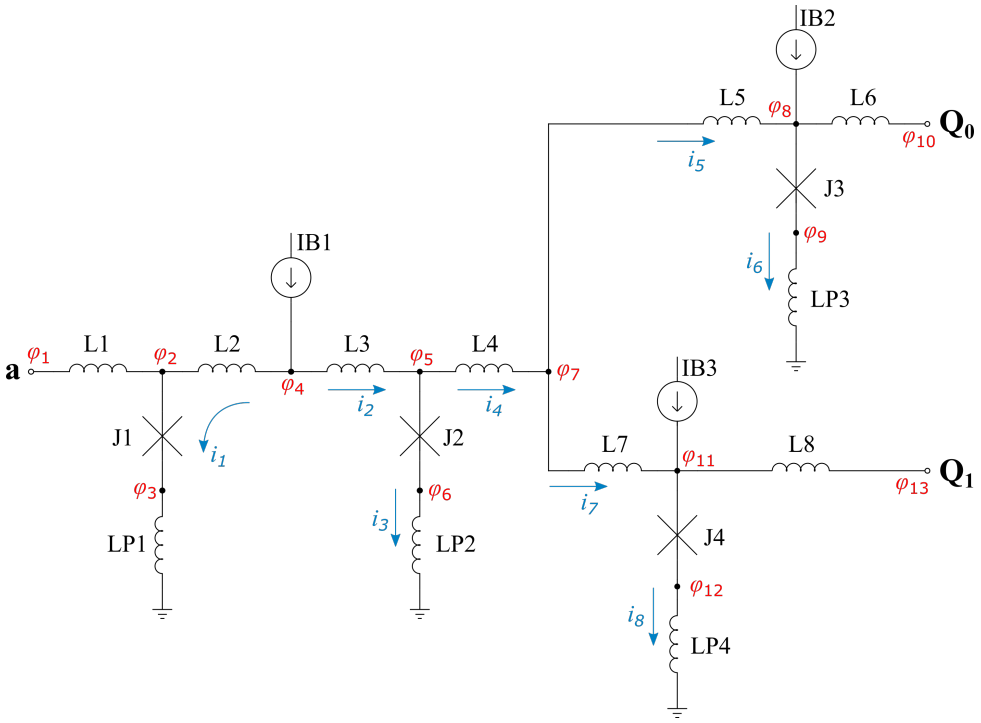


Figure 2.7: Schematic of the RSFQ SPLIT cell.

2.4.2 SPLIT

- This section introduces the concept of multiple branches within RSFQ circuits and how the phase-based equations are influenced by multiple branches.

The fan-out of a circuit refers to the number of load circuits the output of a single circuit can drive. RSFQ circuits are generally designed to be able to drive a single load circuit. If multiple load circuits must be driven by the output of a single circuit, the output line of that circuit must first be split. Splitter cells are often used to split a clock signal within the clocking framework of larger circuits. Experimental splitter cells with more than two output lines have been developed, but the operating margins decrease significantly as the fan-out increases [51].

The SPLIT cell discussed within this section is used to split a signal line into two duplicate output branches. Fig. 2.7 shows the schematic of the SPLIT used for this design example. The input port **a** is found at φ_1 and the output ports $\mathbf{Q_0}$ and $\mathbf{Q_1}$ at φ_{10} and φ_{13}. All inductors are designed to transmit an SFQ pulse. The two output branches are designed to be symmetrical. Thus $L_5 = L_7$, $L_6 = L_8$, $J_3 = J_4$ and $I_{B2} = I_{B3}$. The design values for the RSFQ SPLIT cell is shown in Table 2.4.

The circuit must be analysed in isolation in order to calculate the current distribution within the circuit. The following assumptions are therefore made in order to construct the phase-based equations for the SPLIT cell:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_8 is equal to the phase at φ_{10} so that no current flows through L_6.
3. The phase at φ_{11} is equal to the phase at φ_{13} so that no current flows through L_8.

Table 2.4: Parameter design values for RSFQ SPLIT cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	$1.4I_c$
I_{c3}	J3 critical current	I_c
B_{CC}	Bias current coefficient	-
I_{B1}	Bias current source 1	$B_{CC}(I_{c1} + I_{c2})$
I_{B2}	Bias current source 2	$I_c B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$(\Phi_0/(2I_c))(I_{c2}/(I_{c1} + I_{c2}))$
$L3$	Inductor 3	$(\Phi_0/(2I_c))(I_{c1}/(I_{c1} + I_{c2}))$
$L4$	Inductor 4	$\Phi_0/(4I_{c2})$
$L5$	Inductor 5	$\Phi_0/(4I_{c2})$
$L6$	Inductor 6	$\Phi_0/(4I_c)$

Thus it is assumed that no external currents are present within the SPLIT cell. To determine the current distribution within the SPLIT cell, eight unknown currents, i_1 to i_8, must be calculated. The following five equations are constructed using KCL:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.14}$$

$$g(\boldsymbol{i}) = i_2 - i_3 - i_4 \tag{2.15}$$

$$h(\boldsymbol{i}) = i_4 - i_5 - i_7 \tag{2.16}$$

$$k(\boldsymbol{i}) = I_{B2} + i_5 - i_6 \tag{2.17}$$

$$l(\boldsymbol{i}) = I_{B3} + i_7 - i_8 \tag{2.18}$$

The phase loop through loops L_{P1}-J_1-L_2-L_3-J_2-L_{P2}, L_P-J_3-L_5-L_7-J_4-L_{P4} and L_{P2}-J_2-L_4-L_7-J_4-L_{P4} is analysed to determine the remaining three functions required to implement Newton's Method.

$$m(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 - L_2 i_1 + L_3 i_2 + L_{p2} i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \tag{2.19}$$

$$n(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_6 - L_5 i_5 + L_7 i_7 + L_{p4} i_8\right) - \arcsin\left(\frac{i_6}{I_{c3}}\right) + \arcsin\left(\frac{i_8}{I_{c4}}\right) \tag{2.20}$$

$$o(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_4 i_4 + L_7 i_7 + L_{p4} i_8\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) + \arcsin\left(\frac{i_8}{I_{c4}}\right) \tag{2.21}$$

Table 2.5: Comparison between calculated and simulated values for current distribution for the SPLIT circuit.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	176.324580881	176.324580887	negligible
i_2	243.675419118	243.675419112	negligible
i_3	241.146881320	241.146881303	negligible
i_4	2.528537798	2.528537809	negligible
i_5	1.264268899	1.264268904	negligible
i_6	176.264268899	176.264268904	negligible
i_7	1.264268899	1.264268904	negligible
i_8	176.264268899	176.264268904	negligible

The design values for this example is chosen as $I_c = 250$ μA and $B_{CC} = 0.7$. Newton's Method is used to solve the unknown current variables i_1 to i_8 through (2.14)-(2.21). The current distribution is also simulated using JoSIM and the results are compared within Table 2.5. It is seen that the largest calculation error is ≈ 0.0000004 % for i_4, i_5 and i_7. The calculated current distribution for the SPLIT cell can thus be calculated with minimal error when compared to the simulated values.

Circuit verification

The functionality of the designed RSFQ SPLIT cell must now be confirmed. A phase source is connected to the input port **a** and the amplitude is increased with 2π to simulate an SFQ pulse arriving at **a**. The JTL designed in Section 2.4.1 is connected to **Q** to function as the load circuit. The circuit is simulated using JoSIM and the simulation results are shown in Fig. 2.8. The functionality of the SPLIT cell is also confirmed using TimEx. It is important to note that the output pulses must simultaneously arrive at $\mathbf{Q_0}$ and $\mathbf{Q_1}$ to validate the functionality of the SPLIT cell. TimEx confirms that both the $a \rightarrow Q_0$ and $a \rightarrow Q_1$ delays are identical. The $a \rightarrow q$ delay, extracted as 7.75 ps, is therefore valid for both output branches. The $a \rightarrow q$ delay is also marked by the dashed vertical line in Fig. 2.8. The minimum time delay between two input pulses to ensure a functional splitter circuit is also extracted as 7.031 ps. This minimum time delay alternatively known as the $a \rightarrow a$ critical timing.

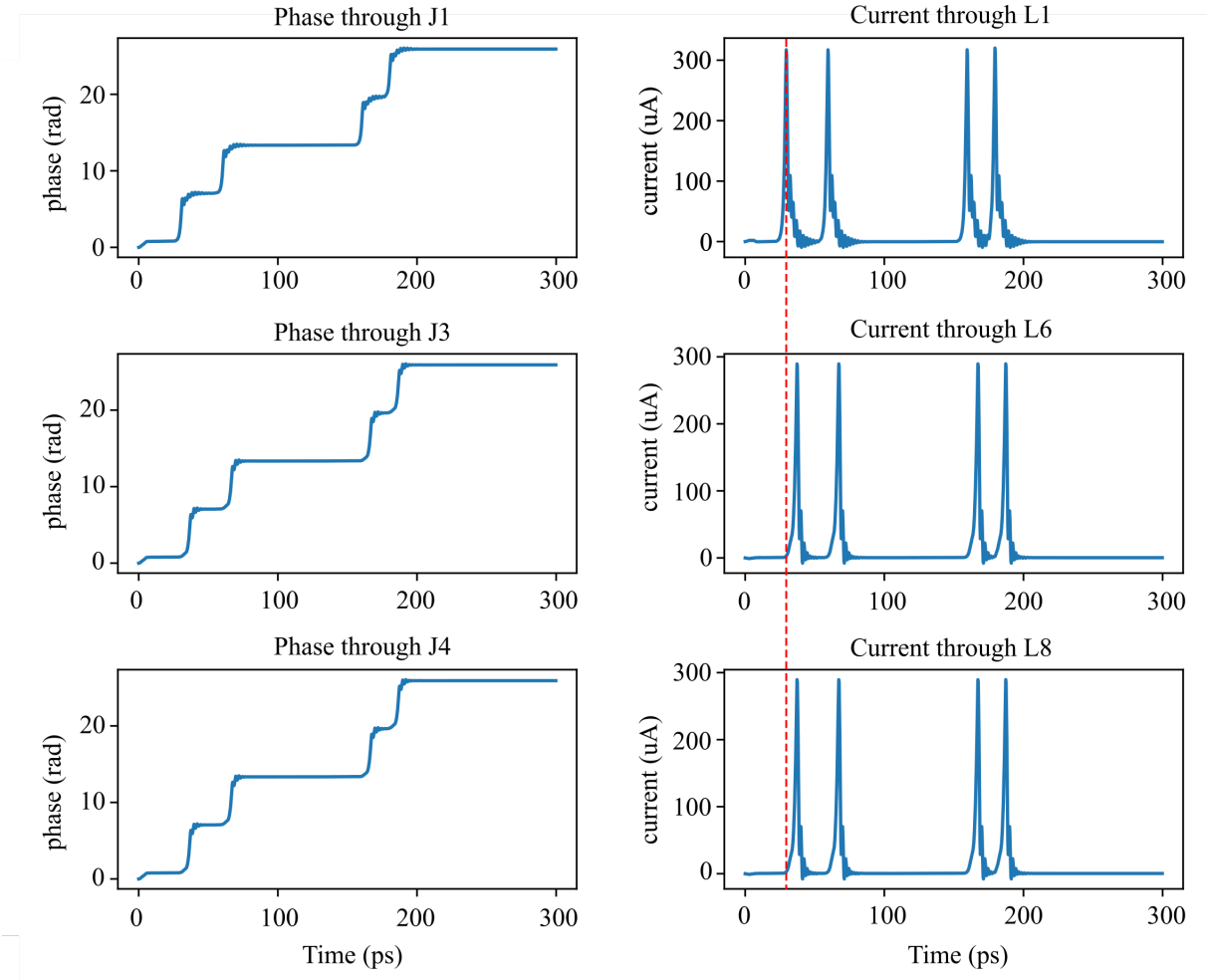


Figure 2.8: Simulation results showing the functionality of the designed RSFQ SPLIT cell.

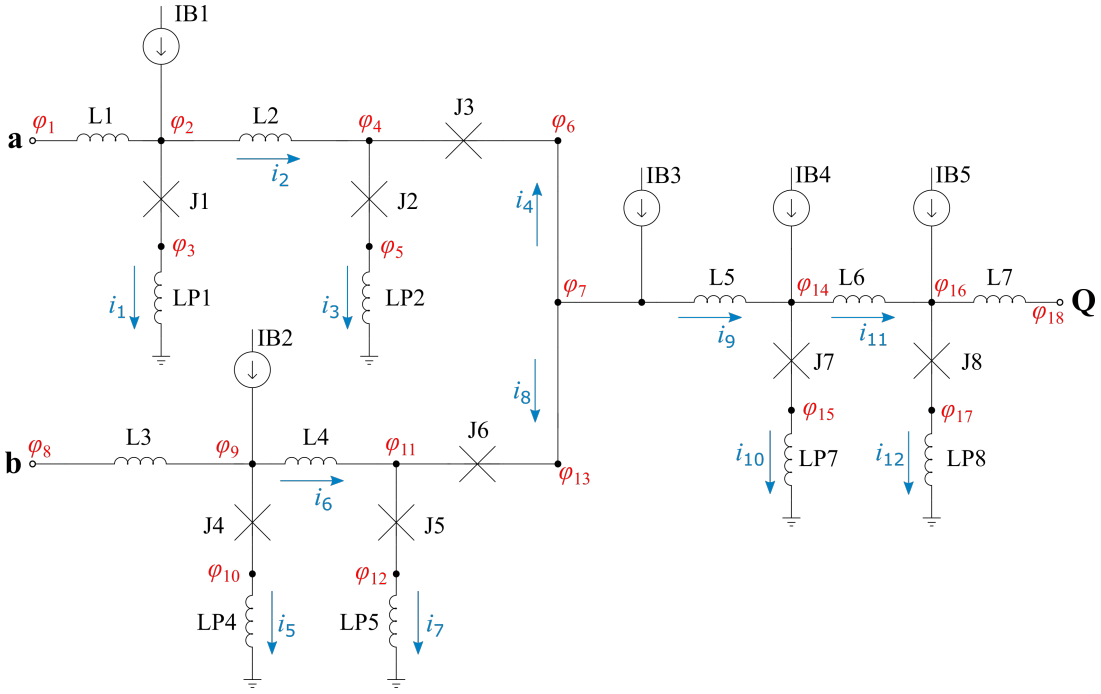


Figure 2.9: RSFQ MERGE Schematic.

2.4.3 MERGE

- This section introduces the concept of a decision pair of Josephson junctions within a circuit.

The merger joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the merger will generate a pulse on the output signal line. The schematic of the RSFQ MERGE cell is shown in Figure 2.9 with the two input ports **a** and **b** found at φ_1 and φ_8 respectively. The output port **Q** is found at φ_{18}. The junctions J_3 and J_6 act as buffers within the MERGE cell when an input signal has been received. If an input pulse arrives at **a**, junctions J_1, J_2, J_6, J_7 and J_8 will switch. Similarly, if an input pulse arrives at **b**, junctions J_4, J_5, J_3, J_7 and J_8 will switch. The two input branches are designed to be symmetrical. Therefore $L_1 = L_3$, $L_2 = L_4$, $J_1 = J_4$, $J_2 = J_5$, $J_3 = J_6$ and $I_{B1} = I_{B2}$. Inductors L_1 to L_7 are designed to transmit a SFQ pulse. The design values for the cell is listed in Table 2.6. The following assumptions are made to analyse the RSFQ MERGE cell in isolation:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_8 is equal to the phase at φ_9 so that no current flows through L_3.
3. The phase at φ_{16} is equal to the phase at φ_{18} so that no current flows through L_7.

Thus it is assumed that no external currents are present within the MERGE cell. The current distribution of the RSFQ MERGE cell can therefore be determined by solving the unknown current values i_1 to i_{12}. KCL is used to determine the first seven equations required to solve the unknown current values.

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.22}$$

Table 2.6: Parameter design values for RSFQ MERGE cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	I_c
I_{c3}	J3 critical current	$I_c/1.4$
I_{c7}	J7 critical current	I_c
I_{c8}	J8 critical current	I_c
B_{CC}	Bias current coefficient	-
I_{B1}	Bias current source 1	$I_{c1}B_{CC}$
I_{B3}	Bias current source 3	I_c
I_{B4}	Bias current source 4	$I_{c7}B_{CC}$
I_{B5}	Bias current source 5	$I_{c8}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L5$	Inductor 5	$\Phi_0/(2I_c)$
$L6$	Inductor 6	$\Phi_0/(2I_{c7})$
$L7$	Inductor 7	$\Phi_0/(4I_c)$

$$g(\boldsymbol{i}) = i_3 - i_2 - i_4 \tag{2.23}$$

$$h(\boldsymbol{i}) = I_{B2} - i_5 - i_6 \tag{2.24}$$

$$k(\boldsymbol{i}) = i_7 - i_6 - i_8 \tag{2.25}$$

$$l(\boldsymbol{i}) = I_{B3} - i_4 - i_8 - i_9 \tag{2.26}$$

$$m(\boldsymbol{i}) = I_{B4} + i_9 - i_{10} - i_{11} \tag{2.27}$$

$$n(\boldsymbol{i}) = I_{B5} + i_{11} - i_{12} \tag{2.28}$$

The phase loop through L_{P1}-J_1-L_2-J_2-L_{P2} is represented through:

$$o(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p2}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \tag{2.29}$$

Analysing the phase loop through L_{P4}-J_4-L_4-J_5-L_{P5} leads to:

$$p(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_5 + L_4 i_6 + L_{p5}i_7\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_7}{I_{c5}}\right) \tag{2.30}$$

Table 2.7: Comparison between calculated and simulated values for current distribution for the MERGE circuit.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	160.607647235	160.607647303	negligible
i_2	14.392352764	14.392352696	negligible
i_3	127.830995475	127.830995466	negligible
i_4	113.438642710	113.438642770	negligible
i_5	160.607647235	160.607647303	negligible
i_6	14.392352764	14.392352696	negligible
i_7	127.830995475	127.830995466	negligible
i_8	113.438642710	113.438642770	negligible
i_9	23.122714578	23.122714458	negligible
i_{10}	142.662763040	142.662762984	negligible
i_{11}	5.459951537	5.459951474	negligible
i_{12}	180.459951537	180.459951474	negligible

The L_{P2}-J_2-J_3-J_6-J_5-L_{P5} phase loop is described through:

$$q(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_{p5}i_7\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_8}{I_{c6}}\right) + \arcsin\left(\frac{i_7}{I_{c5}}\right) \tag{2.31}$$

The phase change through the L_{P2}-J_2-J_3-L_5-J_7-L_{P7} loop can be expressed as:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_5 i_9 + L_{p7}i_{10}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_{10}}{I_{c7}}\right) \tag{2.32}$$

The final equation required for Newton's Method is established by analysing the phase loop L_{P5}-J_5-J_6-L_5-L_6-J_8-L_{P8}:

$$s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_7 + L_5 i_9 + L_6 i_{11} + L_{p8}i_{12}\right) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - \arcsin\left(\frac{i_8}{I_{c6}}\right) + \arcsin\left(\frac{i_{12}}{I_{c8}}\right) \tag{2.33}$$

The MERGE is designed with $I_c = 250$ μA and $B_{CC} = 0.7$. Newton's Method is used to calculate the current distribution of the circuit by solving the unknown current values of i_1 to i_{12}. The comparison between the current values calculated using Newton's Method and the simulated values are listed within Table 2.7.

Circuit verification

Phase sources are connected to input ports **a** and **b** to simulate input SFQ pulses arriving at each port. The JTL designed in Section 2.4.1 is used as the load circuit. The functionality of the designed MERGE cell is shown in the simulation graphs in Fig. 2.10. The $a \rightarrow q$ delay is extracted as 10 ps for both input branches. The $a \rightarrow a$ critical timing, extracted as 7.03 ps, is valid for both input branches. There is also an additional critical timing which indicates the minimum time delay between two input pulses from different input branches to ensure a functional circuit. This is known as the $a \rightarrow b$ critical timing and is extracted as 3.05 ps for the designed RSFQ MERGE cell.

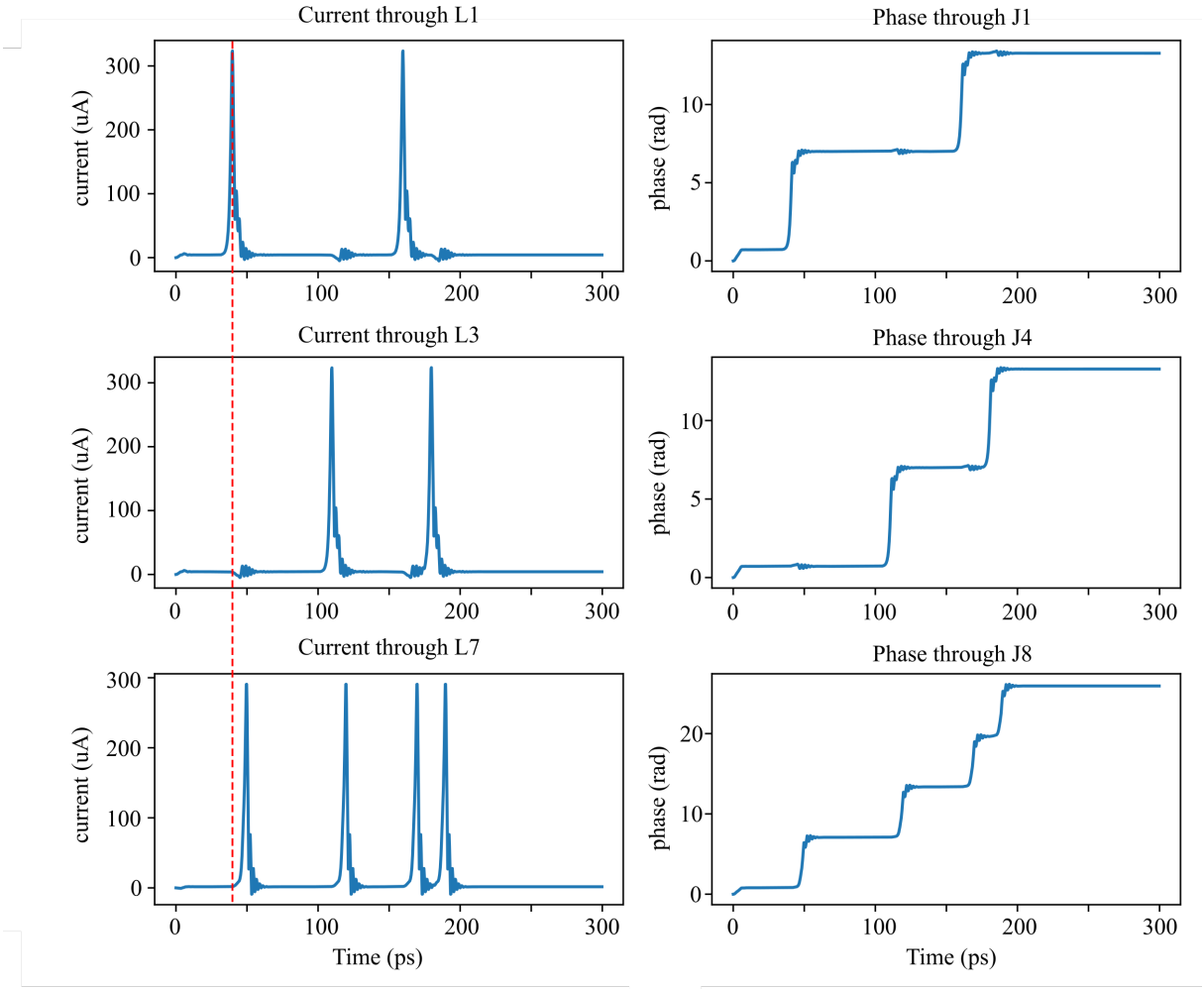


Figure 2.10: Simulation results showing the functionality of the designed RSFQ MERGE cell.

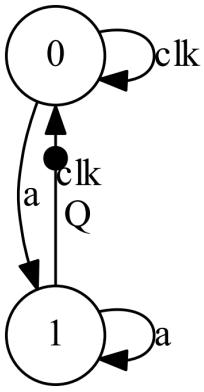


Figure 2.11: Mealy Finite State Machine diagram of DFF.

2.4.4 DFF

- This section introduces the concept of a cell with two states and how circuit analysis is expanded to investigate the cell behaviour in all states. Simulating two states using phase sources in JoSIM is also discussed.

The D flip-flop (DFF) is a multi-state device used to transmit an input set pulse synchronised with a reset (typically clock) signal. The Mealy Finite State Machine diagram showing the multi-state nature of the DFF is shown in Fig. 2.11. The two states of the DFF can be defined as:

1. A 'set' state where an input set signal has been received. It is indicated as state 1 in Fig. 2.11.

2. A 'reset' state where a input reset signal has been received. The reset state can also refer to the 'start-up' state of the DFF before any input signal has been received. It is indicated as state 0 in the state machine diagram.

Fig. 2.12 shows the schematic of an RSFQ DFF with matching JJs. The input port **a** is found at φ_1, the clock input port **clk** at φ_{12} and the output port **Q** is found at φ_{15}. A combination of transfer and storage loops are required to construct the storing functionality within the DFF. To realise this, the RSFQ DFF circuit consists of several transfer blocks along with a storage block at J_3-L_3 and a decision pair at J_4-J_5. The J_2 junction also forms a decision pair with J3 and acts as a buffer junction if more than one input pulse is received before a reset signal. The design values for the DFF is listed in Table 2.8. The current distribution within the RSFQ DFF changes depending on which state the DFF is in. The phase-based design equations should therefore be analysed in both the reset and set state of the DFF.

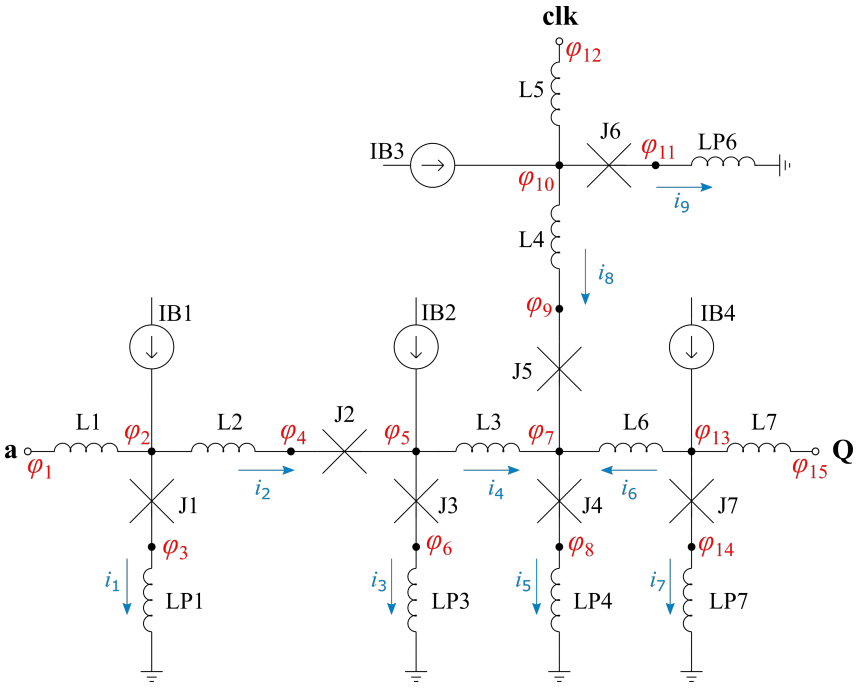


Figure 2.12: RSFQ DFF Schematic.

Table 2.8: Parameter design values for RSFQ DFF cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	$I_c/1.4$
I_{c3}	J3 critical current	I_c
I_{c4}	J4 critical current	I_c
I_{c5}	J5 critical current	$I_c/1.4$
I_{c6}	J6 critical current	I_c
I_{c7}	J7 critical current	I_c
B_{CC}	Bias current coefficient	-
I_{B1}	Bias current source 1	$I_{c1}B_{CC}$
I_{B2}	Bias current source 2	I_{c3}
I_{B3}	Bias current source 3	$I_{c6}B_{CC}$
I_{B4}	Bias current source 4	$I_{c7}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L3$	Inductor 3	Φ_0/I_{c3}
$L4$	Inductor 4	$\Phi_0/(2I_{c6})$
$L5$	Inductor 5	$\Phi_0/(4I_c)$
$L6$	Inductor 6	$\Phi_0/(2I_{c4})$
$L7$	Inductor 7	$\Phi_0/(4I_c)$

Reset State

The reset state indicates that a input reset signal was received by the DFF. Alternatively, it can also indicate that no input signals have been received and that the circuit is in a 'set-up' state. The DFF is analysed using the phase-based component models established in Table 2.1. The following assumptions are made to simplify circuit analysis:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_{12} is equal to the phase at φ_{10} so that no current flows through L_5.
3. The phase at φ_{13} is equal to the phase at φ_{15} so that no current flows through L_7.

Applying these assumptions, the phase change within the circuit is used to analyse the current flow at φ_2, φ_5, φ_7, φ_{10} and φ_{13}. The equations for the current distribution of the four bias current sources completes the nine equations needed for the nine unknown currents i_1 to i_9. Appendix E provides a comprehensive study on how the phase change loops for the DFF is chosen and analysed. KCL can be used to establish the first five equations for the current distribution in the RSFQ DFF circuit:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.34}$$

$$g(\boldsymbol{i}) = I_{B2} + i_2 - i_3 - i_4 \tag{2.35}$$

$$h(\boldsymbol{i}) = i_5 - i_4 - i_6 - i_8 \tag{2.36}$$

$$k(\boldsymbol{i}) = I_{B4} - i_6 - i_7 \tag{2.37}$$

$$l(\boldsymbol{i}) = I_{B3} - i_9 - i_8 \tag{2.38}$$

The phase change within loop L_{P1}-J_1-L_2-J_2-J_3-L_{P3} is described through:

$$\begin{aligned} m(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p3}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) \\ + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \arcsin\left(\frac{i_3}{I_{c3}}\right) \end{aligned} \tag{2.39}$$

The phase changes through the L_{P1}-J_1-L_2-J_2-L_3-J_4-L_{P4} and L_{P3}-J_3-L_3-L_6-J_7-L_{P7} loops are characterised as:

$$\begin{aligned} n(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_3 i_4 + L_{p4}i_5\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) \\ + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \arcsin\left(\frac{i_5}{I_{c4}}\right) \end{aligned} \tag{2.40}$$

and

$$o(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 - L_6 i_6 + L_{p7}i_7\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_7}{I_{c7}}\right) \tag{2.41}$$

The final equation represents the phase change through the L_{P6}-J_6-L_4-J_5-J_4-L_{P4} loop:

$$p(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p6}i_9 + L_4 i_8 + L_{p4}i_5\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \arcsin\left(\frac{i_5}{I_{c4}}\right) \tag{2.42}$$

The values chosen for this design is $I_c = 250$ μA and $B_{CC} = 0.7$. Newton's Method described in (2.1) is used to iteratively solve the values of i_1 to i_9. Table 2.9 shows the comparison between the calculated and simulated values for the current distribution in the DFF circuit for the reset state. It is seen that the differences are negligible.

Table 2.9: Comparison between calculated and simulated values for current distribution for the DFF circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	184.917554808	184.917554813	negligible
i_2	−9.917554808	−9.917554813	negligible
i_3	210.031168069	210.031168197	negligible
i_4	30.051277122	30.051276989	negligible
i_5	79.074657239	79.074657003	negligible
i_6	27.789145924	27.789145848	negligible
i_7	147.210854075	147.210854151	negligible
i_8	21.234234192	21.234234165	negligible
i_9	153.765765807	153.765765834	negligible

Set State

The set state indicates that a input set signal has been received by the DFF. When a single input set signal is received, junctions J_1 and J_3 switch and a flux quantum is stored within the J_3-L_3-J_4 loop. If another input set signal is received before a input reset signal, junction J_2 switches. The following assumptions are made in order to adapt (2.34)-(2.42) for the set state:

1. A phase increase of 2π is observed at φ_2 and φ_5 when the DFF enters the set state.
2. The phase at φ_1 equals the phase at φ_2 so that no current flows through L_1.
3. The phases at φ_7, φ_{10}, φ_{12}, φ_{13} and φ_{15} remain unchanged from the reset state.

Considering these assumptions, it is found that (2.34)-(2.39) and (2.42) still holds true for the set state. The extensive analysis for the DFF in the set state can be found in Appendix E. The 2π phase shift at φ_2 and φ_5 in the set state influences (2.40) and (2.41) as follows:

$$n(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_3 i_4 + L_{p4}i_5\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \arcsin\left(\frac{i_5}{I_{c4}}\right) - 2\pi \tag{2.43}$$

$$o(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 - L_6 i_6 + L_{p7} i_7\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_7}{I_{c7}}\right) - 2\pi \quad (2.44)$$

The values for this DFF design remains $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The current distribution for the DFF within the set state can be calculated through (2.34)-(2.39), (2.42) and (2.43)-(2.44). The current distribution of the DFF within the set state is simulated through a phase source in JoSIM. The phase source makes it possible to simulate the 2π phase shift at φ_1 without an external test circuit. To simulate the start-up state, the phase at φ_2 is measured and a phase source with an equivalent initial phase is connected to φ_1. To simulate the set state, a 2π phase increase is added to the initial phase of the phase source. Table 2.10 shows the comparison between the simulated and calculated current distribution values. It is seen that the calculation error is much larger for the set state than the reset state shown in Table 2.10. This is mainly attributed to the assumption that current does not flow through L_1, L_5 and L_7 during both the reset and set states. When the state of the DFF changes to the set state, the current distribution within the circuit changes, due to stored fluxons, and can affect the phases at the input and output ports. This can lead to current leakage which is not accounted for in the phase-based equations used to describe the current distribution within the DFF. As the possible current leakage is dependent on the source and load circuits, it is not viable to include these currents when establishing the phase-based equation calculations as simulation is required to determine the magnitude of current leakage.

Table 2.11 provides the comparison between the calculated and simulated values when the phase of the input phase source is tuned to ensure that the current through L_1 is less than 10 nA. The original simulated leakage current through L_1 for the DFF within the set state is 20.4 μA. The tuned phase source allows the circuit current distribution to be analysed with the DFF in relative isolation compared to the original set state simulation. Table 2.11 shows that tuning the amplitude of the phase source presents simulated results matching the calculated current distribution more consistently. It is possible to tune the amplitude of the phase source even more to reduce the current leakage through L_1.

A consistent methodology must be developed to test the set states for various RSFQ circuits. Firstly, the initial phase at the receiving junction for the reset state is simulated. For the case of the RSFQ DFF, the receiving junction is J_1 and the initial phase is measured at φ_2. A phase source is then connected to the input port; φ_1 for the case of the DFF. The phase for the reset state is set as the starting phase amplitude for the set state. Thus $\varphi_1 = \varphi_2$ for the case of the DFF. The 2π phase increase is then simulated by adding 2π to the initial amplitude of the phase source. The implementation of the phase source for the set state in JoSIM is shown in Listing 2.1.

```
.param pi = 3.141592654
* Simulated B1 phase for the reset state
.param reset_phase = 0.94873330391631
* 2pi phase increase to simulate set state
.param set_phase = 2*pi+B1_phase_reset
* Phase source definition
P_in a 0 pwl(0 0 5p reset_phase 20p reset_phase 23p set_phase)
* Call Device-Under-Test with relevant port connections
XDUT LSmitll_DFF a clk q
```

Listing 2.1: Phase source implementation for simulating set state of RSFQ DFF in JoSIM.

Table 2.10: Comparison between calculated and simulated values for current distribution for the DFF circuit set state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	149.400058780	165.614512800	−9.7905 %
i_2	25.599941219	29.788880321	−14.0621 %
i_3	57.229025689	60.839929404	−5.9351 %
i_4	218.370915530	218.948950917	−0.2640 %
i_5	201.615650207	201.958426960	−0.1697 %
i_6	−9.450996383	−9.583484697	−1.3825 %
i_7	184.450996383	184.583484697	−0.0718 %
i_8	−7.304268939	−7.407039259	−1.3875 %
i_9	182.304268939	182.407039259	−0.0563 %

Table 2.11: Comparison between calculated and simulated values for current distribution for the tuned DFF circuit within the set state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	149.400058780	149.422246756	−1.48E-2 %
i_2	25.599941219	25.605511553	−2.18E-2 %
i_3	57.229025689	57.233829641	−8.39E-3 %
i_4	218.370915530	218.371681911	−3.51E-4 %
i_5	201.615650207	201.616104965	−2.26E-4 %
i_6	−9.450996383	−9.451171876	−1.86E-3 %
i_7	184.450996383	184.451171876	negligible
i_8	−7.304268939	−7.304405070	−1.86E-3 %
i_9	182.304268939	182.304405070	negligible

Circuit verification

Fig. 2.13 shows the simulation results for the designed RSFQ DFF cell. The DFF is simulated with separate phase sources connected to the input port, **a**, and the clock port, **clk**. A JTL, as designed in Section 2.4.1, is connected to the output port, **Q**, as the load circuit. The current leakage can be observed in the graphs for the current through L_1 and L_5 for the set state. Current leakage through L_7 is visible for both the set and reset state. The simulation graphs for the current through L_5 and L_7 also indicate that there is a time delay between input clock signal and the resulting output pulse. TimEx is used to extract the $clk \rightarrow q$ time delay along with confirming the functionality of the designed DFF. Fig. 2.11 shows the state diagram, as extracted by TimEx. The $clk \rightarrow q$ delay is extracted as 6.0 ps. The $clk \rightarrow q$ delay is indicated in Fig. 2.13 through the dashed vertical line.

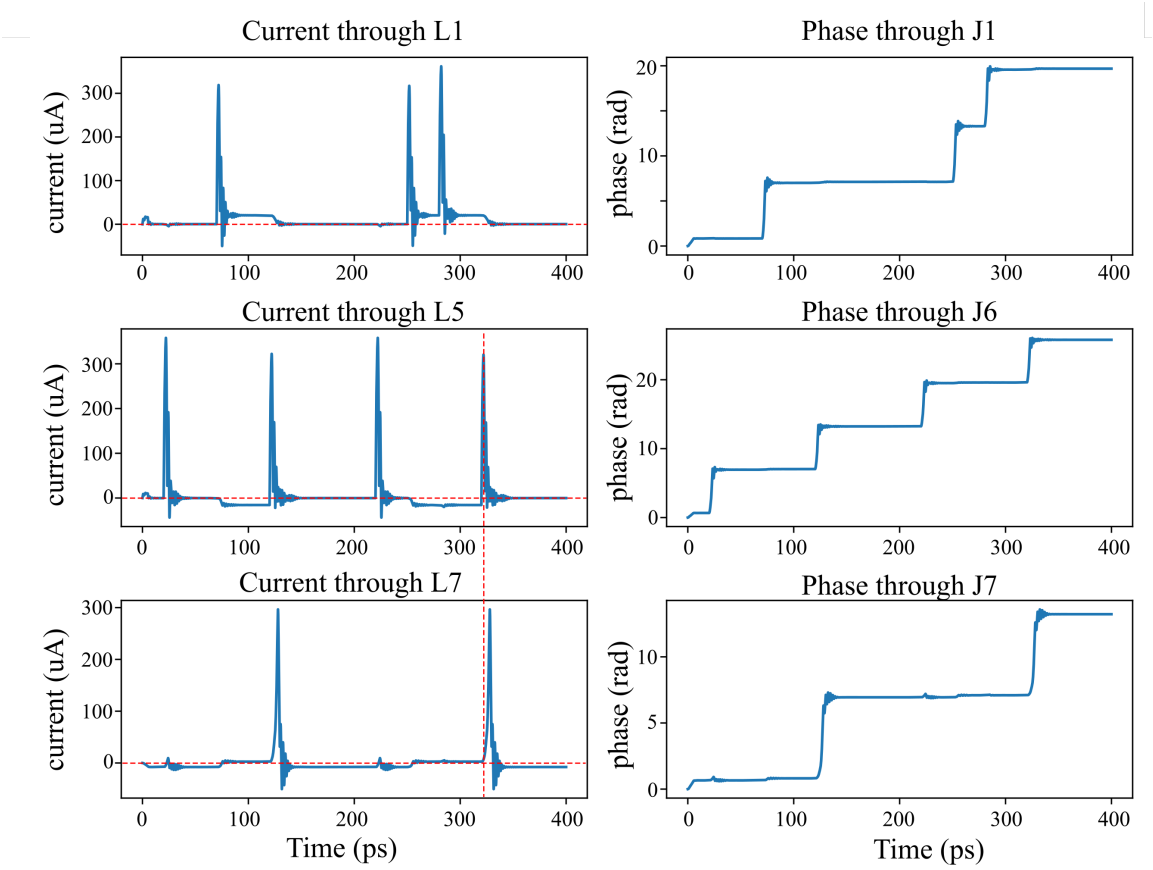


Figure 2.13: Simulation results showing the functionality of the designed RSFQ DFF cell.

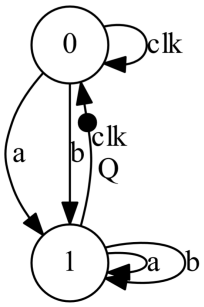


Figure 2.14: Mealy Finite State Machine diagram of the RSFQ OR2 cell.

2.4.5 OR2

- This section introduces the concept of operation margins and how the current distribution within a circuit can affect these margins.

The OR2 cell generates an output pulse if an input pulse from either input lines was received before the clock signal. The Mealy Finite State Machine diagram of the RSFQ OR2 cell is shown in Fig. 2.14. The two states of the OR2 cell can be defined as:

1. A 'reset' state where a clk signal has been received. This state can also indicate the 'start-up' state of the circuit. It is indicated as state 0 in Fig. 2.14.

2. A 'set' state where an input signal from either or both input branches, a and b, have been received. It is indicated as state 1 in Fig. 2.14.

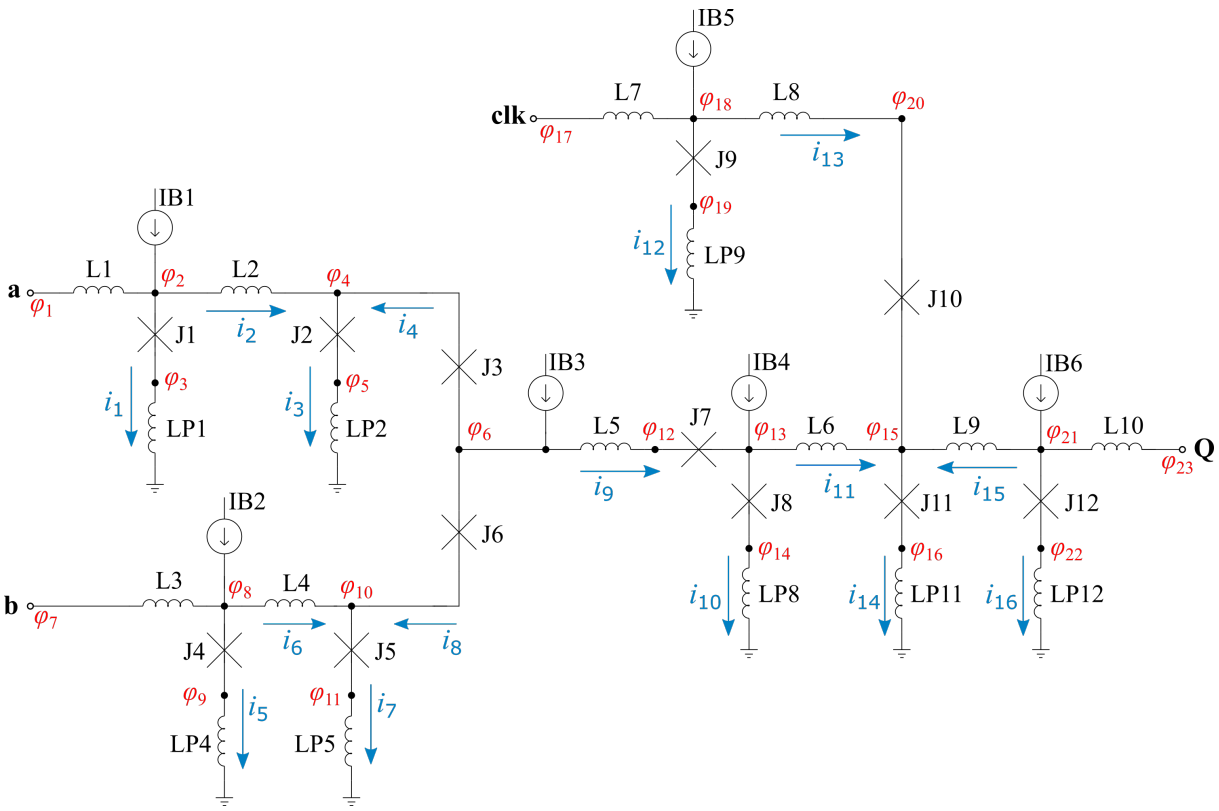


Figure 2.15: RSFQ OR2 Schematic.

Table 2.12: Parameter design values for RSFQ OR2 cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	I_c
I_{c3}	J3 critical current	$I_c/1.4$
I_{c7}	J7 critical current	$I_c/1.4$
I_{c8}	J8 critical current	I_c
I_{c9}	J9 critical current	I_c
I_{c10}	J10 critical current	$I_c/1.4$
I_{c11}	J11 critical current	I_c
I_{c12}	J12 critical current	I_c
Bcc	Bias current coefficient	-
I_{B1}	Bias current 1	$I_{c1}B_{CC}$
I_{B3}	Bias current 3	I_c
I_{B4}	Bias current 4	I_{c8}
I_{B5}	Bias current 5	$I_{c9}B_{CC}$
I_{B6}	Bias current 6	$I_{c12}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L5$	Inductor 5	$\Phi_0/(2I_c)$
$L6$	Inductor 6	Φ_0/I_{c8}
$L7$	Inductor 7	$\Phi_0/(4I_c)$
$L8$	Inductor 8	$\Phi_0/(2I_{c9})$
$L9$	Inductor 9	$\Phi_0/(2I_{c11})$
$L10$	Inductor 10	$\Phi_0/(4I_c)$

Fig. 2.15 shows the schematic of an RSFQ OR2 cell with matching JJs included within the circuit. The ports for the two input branches, **a** and **b**, are located at φ_1 and φ_7. The clock input port, **clk**, is located at φ_{17} and the output port, **Q**, is found at φ_{23}. The OR2 cell is constructed through a combination of the RSFQ MERGE and RSFQ DFF cells. The cell includes multiple transfer blocks and a storage loop through J_8-L_6-J_{11}. The two input branches are designed to be symmetrical, thus $J_1 = J_4$, $J_2 = J_5$, $J_3 = J_6$, $L_1 = L_3$, $L_2 = L_4$ and $I_{B1} = I_{B2}$. The design values for the OR2 cell are listed in Table 2.12. Coinciding with the design of the RSFQ DFF, the current distribution within the RSFQ OR2 cell varies depending on which state the circuit is in. The phase-based equations for the OR2 cell should thus be analysed for both the reset and set states.

Reset state

The reset state of the RSFQ OR2 cell describes the state of the circuit when a clock signal has been received and an output has been generated and the circuit returns to the 'start-up' state. The construction of the phase-based equations requires the circuit to be analysed in isolation. The following assumptions are thus made:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_7 is equal to the phase at φ_8 so that there is no current flowing through L_3.
3. The phase at φ_{17} is equal to the phase at φ_{18} so that the current through L_7 equals zero.
4. The phase at φ_{21} is equal to the phase at φ_{23} so that no current flows through L_{10}.

Considering these assumptions, 16 unknown current values, i_1 to i_{16}, must be solved to determine the current distribution within the OR2 cell. To implement Newton's Method to solve the unknown current values, 16 equations describing the circuit properties are needed. Kirchhoff's current law is used to construct the first nine equations of the current distribution:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.45}$$

$$g(\boldsymbol{i}) = i_3 - i_2 - i_4 \tag{2.46}$$

$$h(\boldsymbol{i}) = I_{B2} - i_5 - i_6 \tag{2.47}$$

$$k(\boldsymbol{i}) = i_7 - i_6 - i_8 \tag{2.48}$$

$$l(\boldsymbol{i}) = I_{B3} - i_4 - i_8 - i_9 \tag{2.49}$$

$$m(\boldsymbol{i}) = I_{B4} + i_9 - i_{10} - i_{11} \tag{2.50}$$

$$n(\boldsymbol{i}) = i_{14} - i_{11} - i_{13} - i_{15} \tag{2.51}$$

$$o(\boldsymbol{i}) = I_{B5} - i_{12} - i_{13} \tag{2.52}$$

$$p(\boldsymbol{i}) = I_{B6} - i_{15} - i_{16} \tag{2.53}$$

The phase change through the L_{P1}-J_1-L_2-J_2-L_{P2}, L_{P4}-J_4-L_4-J_5-L_{P5} and L_{P2}-J_2-J_3-J_6-J_5-L_{P5} loops are described through:

$$q(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p2}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \tag{2.54}$$

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_5 + L_4 i_6 + L_{p5}i_7\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_7}{I_{c5}}\right) \tag{2.55}$$

$$s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_{p5}i_7\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_8}{I_{c6}}\right) + \arcsin\left(\frac{i_7}{I_{c5}}\right) \tag{2.56}$$

Analysing the phase change through L_{P2}-J_2-J_3-L_5-J_7-J_8-L_{P8}:

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_5 i_9 + L_{p8}i_{10}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{10}}{I_{c8}}\right) \tag{2.57}$$

The phase change through the L_{P5}-J_5-J_6-L_5-J_7-L_6-J_{11}-L_{P11} loop is expressed as:

$$u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_7 + L_5 i_9 + L_6 i_{11} + L_{p11}i_{14}\right) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - \arcsin\left(\frac{i_8}{I_{c6}}\right) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) \tag{2.58}$$

The final two equations characterise the phase change through the L_{P9}-J_9-L_8-J_{10}-J_{11}-L_{P11} and L_{P8}-J_8-L_6-L_9-J_{12}-L_{P12} loops:

$$v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p9}i_{12} + L_8 i_{13} + L_{p11}i_{14}\right) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) \tag{2.59}$$

$$w(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p8}i_{10} + L_6 i_{11} - L_9 i_{15} + L_{p12}i_{16}\right) - \arcsin\left(\frac{i_{10}}{I_{c8}}\right) + \arcsin\left(\frac{i_{16}}{I_{c12}}\right) \tag{2.60}$$

The design values for the nominal critical current and bias coefficient are chosen as $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The current values i_1 to i_{16} are calculated by using Newton's Method to solve (2.45)-(2.60). The current distribution within the OR2 cell is also simulated using JoSIM. The comparison between the calculated and simulated values are listed in Table 2.13. It is seen that the calculated values corresponds to the simulated values.

Set state

The RSFQ OR2 cell goes into the set state under three conditions:

1. An input pulse at **A** is received without an input pulse at **CLK**,
2. An input pulse at **B** is received without an input pulse at **CLK**, or
3. Input pulses at both **A** and **B** are received without an input pulse at **CLK**.

These conditions cause a fluxon to get trapped in the L_{P8}-J_8-L_6-J_{11}-L_{P11} loop due to the switching of J_8 and the storing inductor L_6. This trapped fluxon leads to the current distribution within the cell to changing when compared to the reset state. Comprehensive

Table 2.13: Comparison between calculated and simulated values for current distribution for the OR2 circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	162.297039984	162.297040043	negligible
i_2	12.702960015	12.702959956	negligible
i_3	133.698895706	133.698895694	negligible
i_4	120.995935691	120.995935738	negligible
i_5	162.297039984	162.297040043	negligible
i_6	12.702960015	12.702959956	negligible
i_7	133.698895706	133.698895694	negligible
i_8	120.995935691	120.995935738	negligible
i_9	8.008128617	8.008128523	negligible
i_{10}	223.758313866	223.758313944	negligible
i_{11}	34.249814750	34.249814578	negligible
i_{12}	154.343955496	154.343955517	negligible
i_{13}	20.656044503	20.656044482	negligible
i_{14}	81.933056360	81.933056102	negligible
i_{15}	27.027197106	27.027197040	negligible
i_{16}	147.972802893	147.972802959	negligible

phase-based equations for all conditions of the OR2 cell in the set state can be found in Appendix E.

The KCL analysis for the current distribution of the OR2 cell stays consistent regardless of which state the circuit is in. Therefore (2.45) to (2.53) still holds true for the OR2 cell within the set state. The phase change for the set state within the loops described through (2.54)-(2.57) and (2.59) also remains unchanged from the reset state. The functions $u(\boldsymbol{i})$ and $w(\boldsymbol{i})$ described in (2.58) and (2.60) are adapted for the set state as follows:

$$u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_7 + L_5 i_9 + L_6 i_{11} + L_{p11} i_{14}\right) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - \arcsin\left(\frac{i_8}{I_{c6}}\right) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) - 2\pi \tag{2.61}$$

$$w(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p8}i_{10} + L_6 i_{11} - L_9 i_{15} + L_{p12} i_{16}\right) - \arcsin\left(\frac{i_{10}}{I_{c8}}\right) + \arcsin\left(\frac{i_{16}}{I_{c12}}\right) - 2\pi \tag{2.62}$$

The set state of the OR2 cell is simulated using two phase sources connected to **a** and **b**. The value of the phase sources connected to **a** and **b** are initially set to equal the value at φ_2 and φ_8 to mimic the reset state of the circuit. Therefore no current flows through L_1 and L_3. To simulate the set state of the OR2 cell, the amplitude of the phase source connected to **a** is increased with 2π. The circuit set state is also analysed through

Table 2.14: Calculation error comparison for current distribution for both conditions which brings about the set state of the RSFQ OR2 cell.

		% Calculation Error		
	Calculated (μA)	Set A	Set B	Average
i_1	158.1276506	−1.0824 %	−0.0153 %	−0.5489 %
i_2	16.8723493	−3.5056 %	0.1439 %	−1.6808 %
i_3	119.0860058	−0.3758 %	−0.0723 %	−0.2241 %
i_4	102.2136564	0.1605 %	−0.1080 %	0.0263 %
i_5	158.1276506	−0.0153 %	−1.0824 %	−0.5489 %
i_6	16.8723493	0.1439 %	−3.5056 %	−1.6808 %
i_7	119.0860058	−0.0723 %	−0.3758 %	−0.2241 %
i_8	102.2136564	−0.1080 %	0.1605 %	0.0263 %
i_9	45.5726870	−0.1169 %	−0.1169 %	−0.1169 %
i_{10}	74.4313924	−0.0616 %	−0.0616 %	−0.0616 %
i_{11}	221.1412945	−0.0034 %	−0.0034 %	−0.0034 %
i_{12}	182.7983895	−0.0007 %	−0.0007 %	−0.0007 %
i_{13}	−7.7983895	−0.0171 %	−0.0171 %	0.0171 %
i_{14}	203.2550365	−0.0022 %	−0.0022 %	−0.0022 %
i_{15}	−10.0878684	−0.0170 %	−0.0170 %	0.0170 %
i_{16}	185.0878684	−0.0009 %	−0.0009 %	−0.0009 %

applying a 2π phase increase to the phase source connected to **b** to simulate an input at **b**. The resulting calculation errors for both conditions are summarised in Table 2.14. The comprehensive simulation results are listed in Appendix F. It is seen that the largest calculation error for set A is ≈ 3.5 % and for set B is ≈ 3.5 %. The only calculation errors larger than 1 % are found on i_1 and i_2 for set A and i_5 and i_6 for set B. These errors are due to the assumption that no external current enters the OR2 cell during the set state.

Circuit verification

The functionality of the RSFQ OR2 cell is now verified through simulation using JoSIM. Phase sources are connected to ports **a**, **b** and **clk** to simulate SFQ pulses at the relevant ports. A JTL, as designed in Section 2.4.1, is connected to the output port **Q** as the load circuit. The simulation results are shown in Fig. 2.16. The cell functionality is also confirmed through TimEx. The extracted state machine diagram is shown in Fig. 2.14. The $clk \rightarrow q$ time delay is also extracted as 10.8 ps while the $clk \rightarrow clk$ critical timing is extracted as 6.8 ps.

Operation margins

Operating margins of a circuit describes the tolerance of the circuit towards fabrication deviations. It is therefore important to analyse whether a circuit is robust enough to still function as intended once fabricated. The critical operating margin of a circuit indicates which component is the most sensitive to value deviation. Generally, a circuit with a

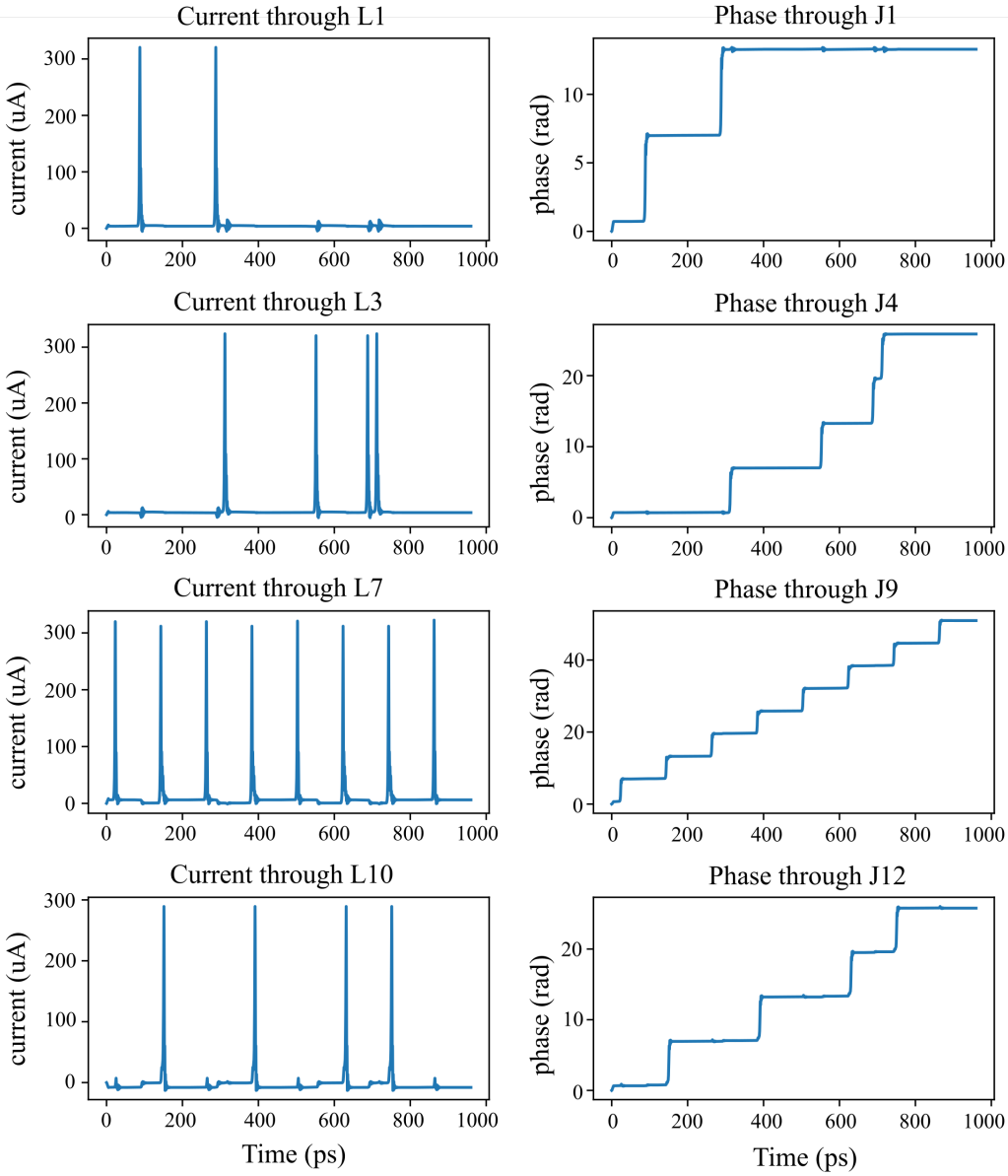


Figure 2.16: Simulation results showing the functionality of the designed RSFQ OR2 cell.

critical margins between ±20 % and ±30 % is considered adequately robust to undergo fabrication.

The majority of the junctions within the RSFQ OR2 cell are designed with 'n bias current equal to 70 % of the junction's critical current as shown in Table 2.12. Biasing the junctions with $I_c/\sqrt{2} \approx 0.7I_c$ provides the largest operating margin for the junction [12], [52]. The additional inductors and junctions connected to the bias current source draws current from the source which is not accounted for in the original OR2 design. Table 2.13 shows that the biasing current of J_1, J_2, J_4, J_5, J_8, J_9, J_{11} and J_{12} are lower than 70 % of the junction's critical current. This skewed current distribution within the circuit is expected to influence the operating margins. The operating margin analysis of the designed RSFQ OR2 cell is shown in Fig. 2.17. It is seen that the critical operating margins are found on J_2 and J_{11} and is 20.8 %.

A method to improve operating margins involves adjusting the bias current sources to ensure that junctions are biased to 70 % of their designed critical current. It is important

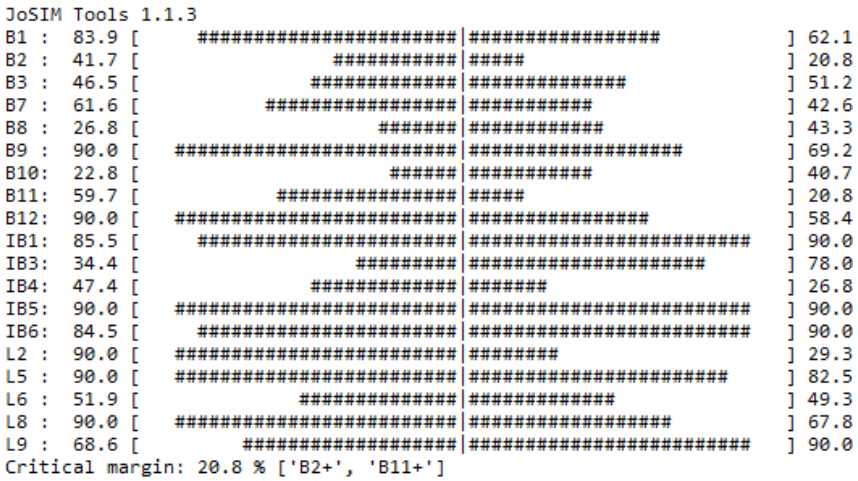


Figure 2.17: Original margins of designed RSFQ OR2 cell.

to note that, for this example, the bias current source I_{B3} which provides current to J_2 and J_5 also biases J_3 and J_6. As J_3 and J_6 are designed to have a critical current of $0.7I_C$, the current flowing through these junctions limits the amount of biasing current is available to J_2 and J_5. Increasing I_{B3} can cause J_3 and J_6 to switch unpredictably. For this example, we will only constrain the current through J_1, J_4, J_9 and J_{12} to $0.7I_c$. The unknowns for the functions (2.45) to (2.60) are adjusted for the new constraints on i_1, i_5, i_{12} and i_{16}. The current sources I_{B1}, I_{B2}, I_{B5} and I_{B6} are set as unknown variables in (2.45) to (2.60). The bias current source values to satisfy the new constraints are calculated using Newton's Method on the adapted functions within (2.45) to (2.60). The resulting bias current values are listed in Table 2.15. We will refer to these newly calculated bias current source values as the tuned values. The resulting margin analysis for this tuned OR2 cell is shown in Fig. 2.18. It is seen that the operation margins of the OR2 cell increased slightly with a critical margin of 23.6 % on J_8.

Constraining the DC current through the matching junctions can lead to better load balancing as the phase over the input/output junctions can be restricted. The concept of load balancing is expanded upon in Section 2.5.

The operation margins of the OR2 cell can be further improved through optimisation algorithms. One such algorithm is the Distance-to-Failure-Maximisation Optimisation Algorithm developed in [53]. The algorithm is implemented within JoSIM Tools [35] to identify an optimised operation point within a multidimensional space. JoSIM Tools is used to optimise the designed RSFQ OR2 cell. The resulting margin analysis is shown in Fig. 2.19. It is seen that the margins have once again improved significantly and that the critical margin for the cell is now 45.8 %.

The margin analysis for all the designed RSFQ cell can be found in Appendix G. The maximum variation of I_c before circuit functionality is compromised is also shown within each cell's margin analysis. The designed cells all have a ± 90 % operating margin for I_c.

Table 2.15: Tuned Parameter design values for RSFQ OR2 cell.

Parameter	Definition	Description
I_{B1}	Bias current 1	$0.777I_{c1}$
I_{B2}	Bias current 2	$0.777I_{c4}$
I_{B5}	Bias current 5	$0.806I_{c9}$
I_{B6}	Bias current 6	$0.854I_{c12}$

Figure 2.18: Margins of RSFQ OR2 cell with tuned junction biasing.

Figure 2.19: Operating margins of optimised RSFQ OR2 cell.

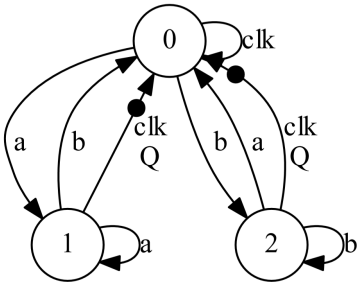


Figure 2.20: Mealy Finite State Machine diagram of the RSFQ XOR cell.

2.4.6 XOR

- This section introduces the concept of cells with multiple set states and how the phase-based equations can be constructed for each of these states. The concept of a yield analysis is also introduced within this section.

The XOR cell generates an output pulse exclusively if a pulse from a single input branch was received before the clock signal. If signals from both input branches are received before a clock signal, the circuit does not generate an output signal. The Mealy Finite State Machine diagram of the RSFQ XOR cell is shown in Fig. 2.20. The three states of the XOR cell can be defined as:

1. A 'reset' state where a clock signal has been received after a single input branch activation. If both input branches are activated, the cell also returns to the reset state. This state can also indicate the 'start-up' state of the circuit. It is indicated as state 0 in Fig. 2.20.

2. A 'set A' state where an input signal from branch **a** has been received. It is indicated as state 1.

3. A 'set B' state where an input signal from branch **b** has been received. It is indicated as state 2.

Fig. 2.21 shows the schematic of an RSFQ XOR cell with matching JJs included within the circuit. The ports for the two input branches, **a** and **b**, are located at φ_1 and φ_8. The clock input port, **clk**, is located at φ_{16} and the output port, **Q**, is found at φ_{22}. The XOR cell is constructed through modifying the RSFQ OR2 cell. The cell includes multiple transfer blocks and storage loops through J_2-J_3-L_3-J_7-J_{10} and J_5-J_6-L_6-J_7-J_{10}. The two input branches are designed to be symmetrical, thus $J_1 = J_4$, $J_2 = J_5$, $J_3 = J_6$, $L_1 = L_4$, $L_2 = L_5$, $L_3 = L_6$, $I_{B1} = I_{B3}$ and $I_{B2} = I_{B4}$. The design values for the XOR cell are listed in Table 2.16. The storage loops within the XOR cell lead to different current distributions within the circuit for different states. The phase-based equations are evaluated for the reset state as well as both set states – set a and set b.

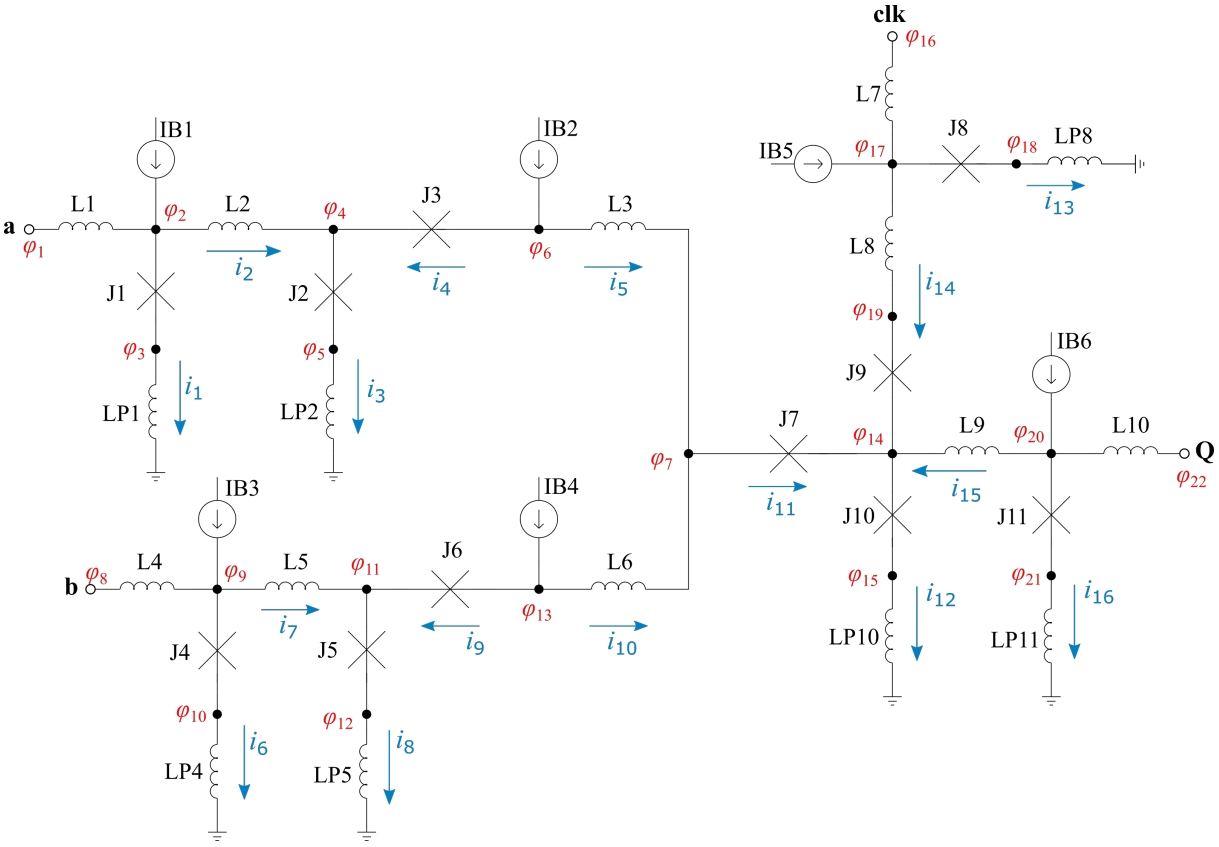


Figure 2.21: RSFQ XOR Schematic.

Reset state

The reset state of the RSFQ XOR cell describes the state of the circuit when either a clock signal has been received and an output has been generated or when both input branches have been activated and the circuit returns to the 'start-up' state. The construction of the phase-based equations requires the circuit to be analysed in isolation. The following assumptions are thus made:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_8 is equal to the phase at φ_9 so that there is no current flowing through L_4.
3. The phase at φ_{16} is equal to the phase at φ_{17} so that the current through L_7 equals zero.
4. The phase at φ_{20} is equal to the phase at φ_{21} so that no current flows through L_{10}.

Implementing these assumptions, 16 unknown current values describe the current distribution within the XOR cell. Thus 16 equations describing the circuit is required to solve for the 16 unknowns. The first ten equations can be derived using KCL:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.63}$$

$$g(\boldsymbol{i}) = i_3 - i_2 - i_4 \tag{2.64}$$

Table 2.16: Parameter design values for RSFQ XOR cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	I_c
I_{c3}	J3 critical current	I_c
I_{c7}	J7 critical current	$I_c/1.4$
I_{c8}	J8 critical current	I_c
I_{c9}	J9 critical current	$I_c/1.4$
I_{c10}	J10 critical current	I_c
I_{c11}	J11 critical current	I_c
Bcc	Bias current coefficient	-
I_{B1}	Bias current 1	$I_{c1}B_{CC}$
I_{B2}	Bias current 2	$I_{c2}B_{CC}$
I_{B5}	Bias current 5	$I_{c8}B_{CC}$
I_{B6}	Bias current 6	$I_{c11}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L3$	Inductor 3	Φ_0/I_{c2}
$L7$	Inductor 7	$\Phi_0/(4I_c)$
$L8$	Inductor 8	$\Phi_0/(2I_{c8})$
$L9$	Inductor 9	$\Phi_0/(2I_{c10})$
$L10$	Inductor 10	$\Phi_0/(4I_c)$

$$h(\boldsymbol{i}) = I_{B2} - i_4 - i_5 \tag{2.65}$$

$$k(\boldsymbol{i}) = I_{B3} - i_6 - i_7 \tag{2.66}$$

$$l(\boldsymbol{i}) = i_8 - i_7 - i_9 \tag{2.67}$$

$$m(\boldsymbol{i}) = I_{B4} - i_9 - i_{10} \tag{2.68}$$

$$n(\boldsymbol{i}) = i_{11} - i_{10} - i_5 \tag{2.69}$$

$$o(\boldsymbol{i}) = I_{B5} - i_{13} - i_{14} \tag{2.70}$$

$$p(\boldsymbol{i}) = i_{12} - i_{11} - i_{14} - i_{15} \tag{2.71}$$

$$q(\boldsymbol{i}) = I_{B6} - i_{15} - i_{16} \tag{2.72}$$

The phase change through the L_{P1}-J_1-L_2-J_2-L_{P2}, L_{P4}-J_4-L_5-J_5-L_{P5} and L_{P2}-J_2-J_3-L_3-L_6-J_6-J_5-L_{P5} loops are described through:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p2}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \tag{2.73}$$

$$s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_6 + L_5 i_7 + L_{p5}i_8\right) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) \tag{2.74}$$

and

$$\begin{aligned} t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_3 i_5 - L_6 i_{10} + L_{p5}i_8\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) \\ + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) \end{aligned} \tag{2.75}$$

The phase change through the L_{P2}-J_2-J_3-L_3-J_7-J_{10}-L_{P10} and L_{P5}-J_5-J_6-L_6-J_7-L_9-J_{11}-L_{P11} loops are described through:

$$\begin{aligned} u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_3 i_5 + L_{p10}i_{12}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) \end{aligned} \tag{2.76}$$

and

$$\begin{aligned} v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_8 + L_6 i_{10} - L_9 i_{15} + L_{p11}i_{16}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right). \end{aligned} \tag{2.77}$$

One more function is required to implement Newton's Method so solve i_1 to i_{16}. To construct the final function, the phase change through loop L_{P8}-J_8-L_8-J_9-J_{10}-L_{P10} is analysed:

$$\begin{aligned} w(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p8}i_{13} + L_8 i_{14} + L_{p10}i_{12}\right) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) \end{aligned} \tag{2.78}$$

To compare the calculated current distribution with the simulated values, the design values for the nominal critical current and bias coefficient are chosen as $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The comparison and calculation error per unknown is listed in Table 2.17. The difference between the calculated ans simulated values for the reset state are thus negligible.

Table 2.17: Comparison between calculated and simulated values for current distribution for the XOR circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	167.267893713	167.267893766	negligible
i_2	7.732106286	7.732106233	negligible
i_3	150.496590263	150.496590314	negligible
i_4	142.764483977	142.764484081	negligible
i_5	32.235516022	32.235515918	negligible
i_6	167.267893713	167.267893791	negligible
i_7	7.732106286	7.732106241	negligible
i_8	150.496590263	150.496590321	negligible
i_9	142.764483977	142.764484079	negligible
i_{10}	32.235516022	32.235515920	negligible
i_{11}	64.471032045	64.471031839	negligible
i_{12}	102.416622318	102.416622068	negligible
i_{13}	158.548748440	158.548748446	negligible
i_{14}	16.451251559	16.451251553	negligible
i_{15}	21.494338713	21.494338675	negligible
i_{16}	153.505661286	153.505661324	negligible

Set A state

The set A state indicates that an SFQ pulse has been received at the **a** branch input, at φ_1 in Fig. 2.21. As a result, J_1 and J_2 undergoes a 2π phase shift and the XOR cell moves from from state 0 to state 1 in Fig. 2.20. The equations describing KCL, (2.63) to (2.72), remains unchanged regardless of the state the XOR cell is in. Appendix E provides a comprehensive study on how the 2π phase shifts affect the current distribution defined through (2.73) to (2.78). Analysing the 2π phase shifts within the XOR cell, it is found that (2.73), (2.74) and (2.77) to (2.78) remain unchanged for the set A state. The $t(\boldsymbol{i})$ function in (2.75) is adapted as follows:

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_3 i_5 - L_6 i_{10} + L_{p5} i_8\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) - 2\pi \tag{2.79}$$

The $u(\boldsymbol{i})$ function in (2.76) also requires adaption for the set A state:

$$u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_3 i_5 + L_{p10} i_{12}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) - 2\pi \tag{2.80}$$

The XOR within the set A state is simulated using phase sources in JoSIM. Table 2.18 shows the comparison between the calculated and simulated current distribution within the XOR during the set A state. It is seen that the largest calculation errors are on i_{14} and i_{15} with approximately 11.5 % calculation error. But these simulated current values have amplitudes of less than half a micro-ampere, so a small variation in the calculated value results in a large percentage calculation error. The largest calculation error is on i_1 with a -12.5 μA error. It is expected that the largest calculation errors will be on the unknowns closest to input port **a**.

Table 2.18: Comparison between calculated and simulated values for current distribution for the XOR circuit set A state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	137.288904647	149.815162894	-8.36 %
i_2	37.711095352	41.802674455	-9.79 %
i_3	41.264461615	44.995677121	-8.29 %
i_4	3.553366262	3.193002666	11.29 %
i_5	171.446633737	171.806997333	-0.21 %
i_6	174.701999503	174.730943777	-0.02 %
i_7	0.298000496	0.269056222	10.76 %
i_8	174.097074554	174.184930388	-0.05 %
i_9	173.799074057	173.915874166	0.07 %
i_{10}	1.200925942	1.084125833	10.77 %
i_{11}	172.647559679	172.891123166	-0.14 %
i_{12}	173.514379846	173.668363098	-0.09 %
i_{13}	174.622871927	174.661842464	-0.02 %
i_{14}	0.377128072	0.338157535	11.52 %
i_{15}	0.489692094	0.439082395	11.53 %
i_{16}	174.510307905	174.560917604	-0.03 %

Set B state

The set B state indicates that an SFQ pulse has been received at the **b** input port. This pulse causes J_4 and J_5 to switch and undergo a 2π phase shift. Similar to the set A state, the KCL equations for the reset state, (2.63)-(2.72), remain valid for the set B state. A comprehensive study regarding the construction of the phase-based equations for the XOR cell in the set B state can be found in Appendix E. The functions described in (2.73), (2.74), (2.76) and (2.78) remain unchanged for the set B state. The functions describing the phase change through the L_{P2}-J_2-L_3-L_6-J_6-J_5-L_{P5} and L_{P5}-J_5-J_6-L_6-J_7-L_9-J_{11}-L_{P11}

loops are adapted as follows:

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 + L_3 i_5 - L_6 i_{10} + L_{p5}i_8\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + 2\pi \tag{2.81}$$

and

$$v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_8 + L_6 i_{10} - L_9 i_{15} + L_{p11}i_{16}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) - 2\pi \tag{2.82}$$

The designed XOR cell within the set B state is now simulated using JoSIM. The simulated current distribution is compared with the calculated values within Table 2.19. It is seen that similar calculation errors are present as discussed for the XOR cell within the set A state. As expected, the largest calculation error is on i_5 with a -12.5 μA error.

Table 2.19: Comparison between calculated and simulated values for current distribution for the XOR circuit set B state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	174.701999503	174.730943777	-0.02 %
i_2	0.298000496	0.269056222	10.76 %
i_3	174.097074554	174.184930388	-0.05 %
i_4	173.799074057	173.915874166	-0.07 %
i_5	1.200925942	1.084125833	10.77 %
i_6	137.288904647	149.815162894	-8.36 %
i_7	37.711095352	41.802674455	-9.79 %
i_8	41.264461615	44.995677121	-8.29 %
i_9	3.553366262	3.193002666	11.29 %
i_{10}	171.446633737	171.806997333	-0.21 %
i_{11}	172.647559679	172.891123167	-0.14 %
i_{12}	173.514379846	173.668363098	-0.09 %
i_{13}	174.622871927	174.661842464	-0.02 %
i_{14}	0.377128072	0.338157535	11.52 %
i_{15}	0.489692094	0.439082395	11.53 %
i_{16}	174.510307905	174.560917604	-0.03 %

Circuit verification

The functionality of the designed RSFQ XOR cell is now verified through simulation. The resulting simulation graphs is shown in Fig. 2.22. The cell functionality is also confirmed through TimEx. The state machine diagram extracted using TimEx is shown in Fig. 2.20. The $clk \rightarrow q$ time delay is extracted as 10.3 ps for both the set A and set B states. The usage of the extracted time delay and critical timing values are discussed in Section 2.4.7.

Operation margins

The operating margins for the designed XOR cell is shown in Fig. 2.23. It is seen that the critical margin is 7.3 % on junction J_9. Referring to Table 2.17, it is seen that current through the matching junctions, i_1, i_6, i_{13} and i_{16}, are lower than the designed $0.7I_c$ due to unexpected current distribution within the circuit. Adapting (2.63) to (2.78) to constrain i_1, i_6, i_{13} and i_{16} to the designed values, the current distribution within the matching junctions can be fixed for the reset state. The bias current sources I_{B1}, I_{B3}, I_{B5} and I_{B6} are set as variables in (2.63) to (2.78) while i_1, i_6, i_{13} and i_{16} are defined as constant values. The resulting operating margins are shown in Fig. 2.24. It is seen that the critical margin has increased to 10.1 %. The critical margin is caused by junction J_2 and, due to cell symmetry, J_5. The operating margins in Fig. 2.24 also show that I_{B2} and, by extension, I_{B4} have a critical margin of 14.5 %. The current distribution constraints are now extended to include constraints on i_3 and i_8. The bias current sources I_{B2} and I_{B4} are converted to variables within (2.63) to (2.78). The resulting operating margins of these constraints are shown in Fig. 2.25. It is seen that the critical margin for the cell has one again increased to 13.1 % on junction J_2. The critical margin of the designed RSFQ XOR cell can therefore almost be doubled through constraining the current distribution within the cell. Although the method of constraining the current distribution within a circuit does not optimise the operating margins to the same extent as a conventional optimisation tool, it is also not as time consuming and memory intensive as these optimisation tools.

For the sake of completeness, the tuned RSFQ XOR cell is optimised using JoSIM-tools. The size of the matching junctions and the current through these junctions are constraint during the optimisation process to minimise potential current leakage when connected the XOR cell to other cells.

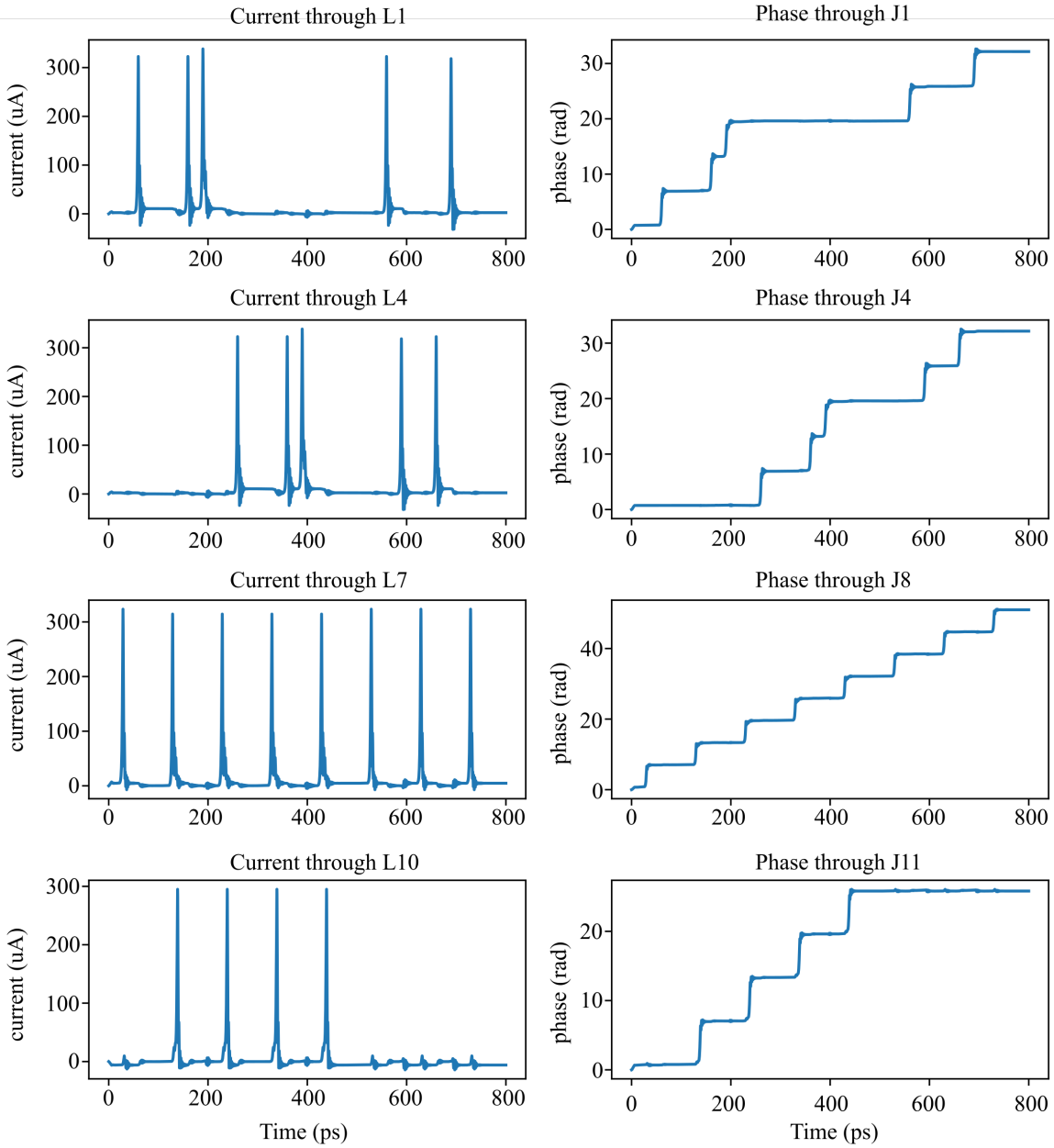


Figure 2.22: Simulation results showing the functionality of the designed RSFQ XOR cell.

```
JoSIM Tools 1.1.3
B1 :  47.4 [              ##############|##############             ] 51.4
B2 :  18.0 [                    ######|##                           ]  9.2
B3 :  35.4 [                  #########|###                         ] 14.0
B7 :  30.7 [                   ########|###########                 ] 42.5
B8 :  90.0 [  ########################|####################        ] 69.3
B9 :   7.3 [                       ##|######                       ] 24.3
B10:  50.7 [              ##############|##                         ]  7.5
B11:  89.0 [   ########################|##########                 ] 38.2
IB1:  53.3 [              ##############|####################        ] 69.9
IB2:  13.1 [                       ###|###############              ] 51.9
IB5:  90.0 [  ########################|########################### ] 90.0
IB6:  36.8 [                  #########|########################### ] 90.0
L2 :  72.5 [        ####################|###                        ] 10.8
L3 :  46.8 [              ##############|########                   ] 31.4
L8 :  51.4 [              ##############|###########                ] 40.9
L9 :  32.6 [                  #########|########################### ] 90.0
Critical margin:  7.3 % ['B9-']
```

Figure 2.23: Operation margins of the designed RSFQ XOR cell.

```
JoSIM Tools 1.1.3
B1 :  43.9 [                ############|###############             ] 54.8
B2 :  16.8 [                        ####|##                          ] 10.1
B3 :  35.2 [                    #########|####                        ] 14.3
B7 :  31.6 [                     ########|###########                 ] 41.9
B8 :  90.0 [   ########################|######################      ] 78.3
B9 :  10.6 [                          ##|#######                     ] 25.0
B10:  46.7 [               #############|###                         ] 10.8
B11:  69.7 [         ###################|###############             ] 55.5
IB1:  56.3 [             ###############|#################           ] 61.8
IB2:  14.5 [                        ####|##############              ] 51.9
IB5:  90.0 [   ########################|######################      ] 78.0
IB6:  44.7 [                ############|####################        ] 74.1
L2 :  75.8 [       ####################|###                         ] 11.9
L3 :  48.3 [               #############|#############               ] 51.2
L8 :  90.0 [   ########################|###########                 ] 42.5
L9 :  53.5 [                ############|########################    ] 90.0
Critical margin: 10.1 % ['B2+']
```

Figure 2.24: Operation margins of the tuned RSFQ XOR cell with current distribution constraints on matching junctions.

```
JoSIM Tools 1.1.3
B1 :  38.1 [                   ##########|###############             ] 55.6
B2 :  13.1 [                         ###|######                      ] 22.6
B3 :  22.8 [                      #######|#####                       ] 18.9
B7 :  23.6 [                      #######|#############               ] 47.5
B8 :  90.0 [   ########################|######################      ] 78.3
B9 :  14.7 [                        ####|######                      ] 22.9
B10:  40.3 [                ############|####                        ] 15.4
B11:  64.1 [           #################|###################         ] 73.2
IB1:  79.4 [       ####################|###############             ] 54.9
IB2:  26.6 [                     ########|#######                    ] 28.4
IB5:  90.0 [   ########################|######################      ] 79.5
IB6:  67.9 [          ###################|###################         ] 72.7
L2 :  86.0 [     ######################|########                    ] 30.8
L3 :  36.3 [                   ##########|###################         ] 73.4
L8 :  90.0 [   ########################|###########                 ] 39.6
L9 :  68.6 [          ###################|########################    ] 90.0
Critical margin: 13.1 % ['B2-']
```

Figure 2.25: Operation margins of the tuned RSFQ XOR cell with current distribution constraints.

```
JoSIM Tools 1.1.3
B1 :  56.2 [              ###############|########                    ] 29.8
B2 :  35.8 [                   ##########|##########                ] 37.9
B3 :  34.4 [                    #########|########                  ] 30.0
B7 :  34.4 [                    #########|#########                 ] 33.0
B8 :  55.1 [              ###############|###################         ] 74.6
B9 :  31.0 [                     ########|#########                 ] 33.3
B10:  46.1 [                  ###########|###########               ] 41.2
B11:  51.4 [                ##############|###################         ] 75.0
IB1:  39.1 [                   ##########|####################        ] 78.5
IB2:  50.7 [                ##############|##############              ] 50.5
IB5:  90.0 [   ########################|##################          ] 66.4
IB6:  90.0 [   ########################|################            ] 59.5
L2 :  43.5 [                ############|############                ] 44.4
L3 :  57.2 [              ###############|####################        ] 75.8
L8 :  90.0 [   ########################|########################    ] 90.0
L9 :  90.0 [   ########################|########################    ] 90.0
Critical margin: 29.8 % ['B1+']
```

Figure 2.26: Operation margins of the optimised RSFQ XOR cell.

Yield analysis

Process variations cause fabricated circuits to differ slightly from the designed values. Yield analysis is a method used to estimate the probability of the fabricated circuit functioning correctly. Monte Carlo analysis is generally used to calculate the yield of a circuit [54]. Yield analysis is often used in conjunction with margin analysis to determine the fabrication tolerance of a circuit. Yield analysis is a probabilistic approach which analyses multiple sample points within a Gaussian distribution to determine the yield percentage of functional circuits given a certain parameter standard deviation, σ. Yield analysis is therefore an expensive operation to perform in comparison to margin analysis [53]. Circuit optimisation is typically done through analysing the operating margins. The yield analysis is performed after operating margin optimisation to confirm the robustness of a circuit.

As the process variations alter the fabricated resistors, inductors and junction values, three global parameters are added to each circuit netlist: I_{global}, B_{global} and L_{global}. The process variations altering the resistors affect I_{global} as the bias current sources are constructed using bias resistors connected to a constant DC voltage. B_{global} represents the variations on junction sizes and L_{global} describes the variations of the inductors. A variance value is also assigned to each of the global parameters within a JoSIM-tools set-up file. The set-up file for yield analysis using JoSIM-tools (version 1.1.3) is listed in Listing 2.2. An arbitrary variance of $\sigma^2 = 0.1$ and number of samples equal to 10 000 is chosen for the listing.

```
mode = ``yield"

[parameters]
Btotal  = {nominal = 1, variance = 0.1}
Ltotal  = {nominal = 1, variance = 0.1}
Itotal  = {nominal = 1, variance = 0.1}

[yield]
num_samples = 10000

[verify]
method = ``spec_file"
file = ``LSmitll_XOR.sp"
circuit = ``LSmitll_XOR.cir"
threshold = 0.35
```

Listing 2.2: Yield analysis set-up file for JoSIM-tools.

The yield analysis of a circuit is generally visualised through a yield roll-off curve. This curve displays the yield at varying values of standard deviation, variance or parameter spread. The comparative yield roll-off curves for the designed, tuned and optimised RSFQ XOR cell are shown in Fig. 2.27. A circuit is generally considered robust when it has a 100 % yield at 0.2 parameter spread. All three versions of the RSFQ XOR cell can therefore be considered robust enough to have the correct functionality after fabrication. The optimised XOR cell has a 100 % yield at 0.25 standard deviation and a 99.7 % yield at 0.3 deviation.

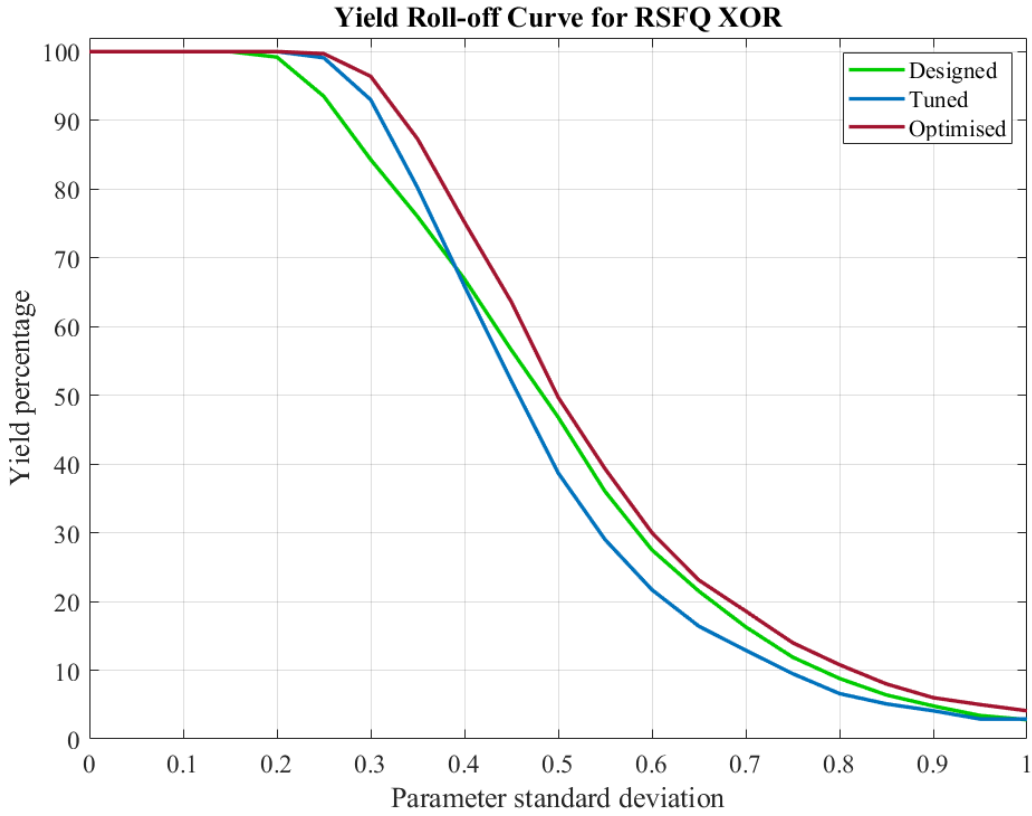


Figure 2.27: Yield roll-off curve for the designed, tuned and optimised RSFQ XOR cell.

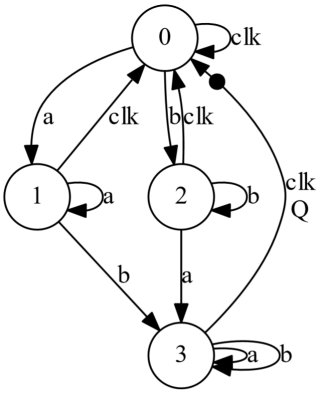


Figure 2.28: Mealy Finite State Machine diagram of the RSFQ AND2 cell.

2.4.7 AND2

- This section discusses how an RSFQ cell with four states is designed. The concept of a digital circuit model and simulation is also introduced within this section.

The RSFQ AND2 cell is a cell which performs logical conjunction of two input branches. The AND2 cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The Mealy Finite State Machine diagram for the RSFQ AND2 cell is shown in Fig. 2.28. The four states of the AND2 cell illustrated in Fig. 2.28 are defined as:

1. A 'reset' state where the circuit received a clock input signal. This state can also indicate the 'start-up' state of the circuit and is labelled as state 0.

2. A 'set A' state where an input signal from branch **a** has been received. It is indicated as state 1 in Fig. 2.28.

3. A 'set B' state where an input signal from branch **b** has been received. It is indicated as state 2 within the state diagram.

4. A 'set AB' state where input signals from both **a** and **b** branches have been received before a clock signal. It is labelled as state 3.

The schematic for the RSFQ AND2 cell with matching JJs is shown in Fig. 2.29. The input ports are indicated through **a** and **b** and are found at φ_1 and φ_{13}. The clock input port is marked as **clk** at φ_{22} and the output port is indicated as **Q** at φ_{29}. The constraints of a physical layout is introduced within the circuit design for the AND2 cell. In an ideal schematic for the AND2 cell, inductors L_4, L_9, L_{13} and L_{14} from Fig. 2.29 could be excluded, as shown in [12]. Modern fabrication processes such as the MIT-LL SFQ5ee process present constraints for minimum distance between specific metal elements. These constraints are discussed in detail in Chapter 4. For this design example, we assume that the physical layout constraints are satisfied when $L_4 = L_9 = L_{13} = L_{14} = 1$ pH. Input branches **a** and **b** are designed to be identical along with $J_4 = J_{10}$, $J_5 = J_{11}$, $L_5 = L_{10}$ and $J_6 = J_{12}$.

Input SFQ pulses are stored through the J_3-L_3-J_5 and J_9-L_8-J_{11} storage loops for the set **a** and set **b** states respectively. If a clock pulse is received when both the J_3-L_3-J_5 and J_9-L_8-J_{11} storage loops contain a fluxon, junctions J_5 and J_{11} will switch simultaneously

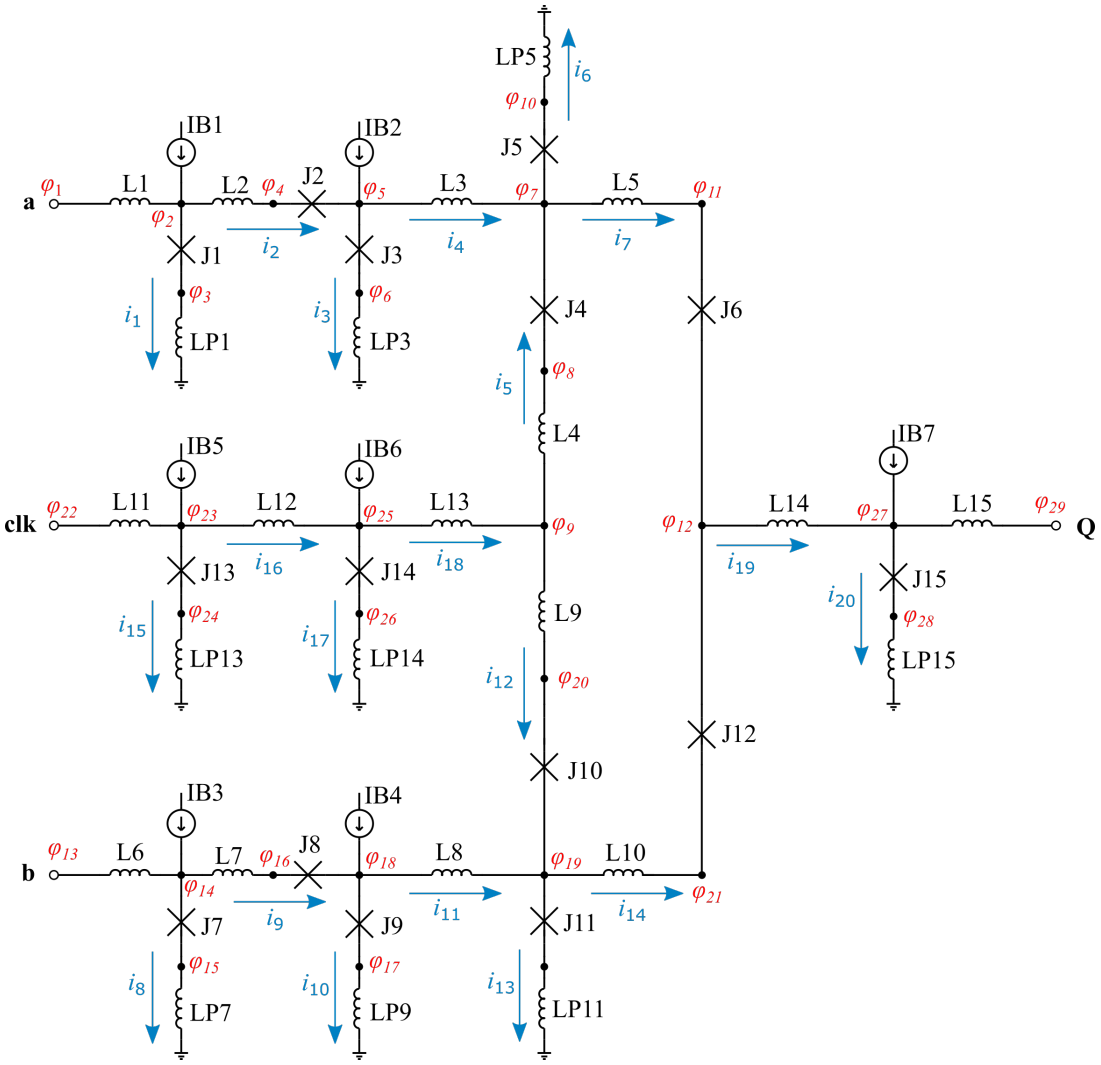


Figure 2.29: RSFQ AND2 schematic.

and generate an output pulse through L_{14}. The design values for the AND2 cell are listed in Table 2.20.

Reset state

The RSFQ AND2 cell returns to the reset state when a clock input signal is received. The reset state can also refer to the 'start-up' state of the circuit and is indicated as state 0 in Fig. 2.28. No fluxons are stored within the AND2 cell for the reset state.

The following assumptions are made to analyse the cell in isolation:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_{13} is equal to the phase at φ_{14} so that there is no current flowing through L_6.
3. The phase at φ_{22} is equal to the phase at φ_{23} so that the current through L_{11} equals zero.
4. The phase at φ_{27} is equal to the phase at φ_{29} so that no current flows through L_{15}.

Table 2.20: Parameter design values for RSFQ AND2 cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	$I_c/1.4$
I_{c3}	J3 critical current	I_c
I_{c4}	J4 critical current	$I_c/1.4$
I_{c5}	J5 critical current	I_c
I_{c6}	J6 critical current	$I_c/1.4$
I_{c13}	J13 critical current	I_c
I_{c14}	J14 critical current	I_c
I_{c15}	J15 critical current	I_c
Bcc	Bias current coefficient	-
I_{B1}	Bias current 1	$I_{c1}B_{CC}$
I_{B2}	Bias current 2	$I_{c3}B_{CC}$
I_{B5}	Bias current 5	$I_{c13}B_{CC}$
I_{B6}	Bias current 6	$I_{c14}B_{CC}$
I_{B7}	Bias current 7	$I_{c15}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L3$	Inductor 3	Φ_0/I_{c3}
$L5$	Inductor 5	$\Phi_0/(2I_{c5})$
$L11$	Inductor 11	$\Phi_0/(4I_c)$
$L12$	Inductor 12	$\Phi_0/(2I_{c13})$
$L15$	Inductor 15	$\Phi_0/(4I_c)$

Analysing the AND2 cell in isolation, the current distribution can be described through 20 unknown currents. Therefore 20 equations are required to solve the 20 unknowns using Newton's Method. KCL is used to construct the first 11 equations:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.83}$$

$$g(\boldsymbol{i}) = I_{B2} + i_2 - i_3 - i_4 \tag{2.84}$$

$$h(\boldsymbol{i}) = i_4 + i_5 - i_6 - i_7 \tag{2.85}$$

$$k(\boldsymbol{i}) = I_{B3} - i_8 - i_9 \tag{2.86}$$

$$l(\boldsymbol{i}) = I_{B4} + i_9 - i_{10} - i_{11} \tag{2.87}$$

$$m(\boldsymbol{i}) = i_{11} + i_{12} - i_{13} - i_{14} \tag{2.88}$$

$$n(\boldsymbol{i}) = I_{B5} - i_{15} - i_{16} \tag{2.89}$$

$$o(\boldsymbol{i}) = I_{B6} + i_{16} - i_{17} - i_{18} \tag{2.90}$$

$$p(\boldsymbol{i}) = i_{18} - i_5 - i_{12} \tag{2.91}$$

$$q(\boldsymbol{i}) = i_{19} - i_7 - i_{14} \tag{2.92}$$

$$r(\boldsymbol{i}) = I_{B7} + i_{19} - i_{20} \tag{2.93}$$

The phase changes through the L_{P1}-J_1-L_2-J_2-J_3-L_{P3} and L_{P3}-J_3-L_4-J_5-L_{P5} loops are described by:

$$\begin{aligned} s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p3}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \\ + \arcsin\left(\frac{i_3}{I_{c3}}\right) \end{aligned} \tag{2.94}$$

and

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 + L_{p5}i_6\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right). \tag{2.95}$$

The phase change through the L_{P5}-J_5-L_5-J_6-$J_1$2-L_{10}-J_{11}-L_{P11} loop is expressed as:

$$\begin{aligned} u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_6 + L_5 i_7 - L_{10}i_{14} + L_{p11}i_{13}\right) - \arcsin\left(\frac{i_6}{I_{c5}}\right) + \arcsin\left(\frac{i_7}{I_{c6}}\right) \\ - \arcsin\left(\frac{i_{14}}{I_{c12}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) \end{aligned} \tag{2.96}$$

The following three equations present the phase change through the L_{P7}-J_7-L_7-J_8-J_9-L_{P9}, L_{P9}-J_9-L_8-J_{11}-L_{P11} and L_{P5}-J_5-J_4-L_4-L_9-J_{10}-J_{11}-L_{P11} loops:

$$v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p7}i_8 + L_7 i_9 + L_{p9}i_{10}\right) - \arcsin\left(\frac{i_8}{I_{c7}}\right) + \arcsin\left(\frac{i_9}{I_{c8}}\right) + \arcsin\left(\frac{i_{10}}{I_{c9}}\right) \tag{2.97}$$

$$w(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p9}i_{10} + L_8 i_{11} + L_{p11}i_{13}\right) - \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) \tag{2.98}$$

$$x(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p5}i_6 - L_4 i_5 + L_9 i_{12} + L_{p11}i_{13}\right) - \arcsin\left(\frac{i_6}{I_{c5}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) \tag{2.99}$$

The phase change loop through the clock input branch is described through:

$$y(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p13}i_{15} + L_{12}i_{16} + L_{13}i_{18} + L_4 i_5 + L_{p5}i_6\right) - \arcsin\left(\frac{i_{15}}{I_{c13}}\right) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right) \tag{2.100}$$

The final two equations present the phase change through the L_{P14}-J_{14}-L_{13}-L_9-J_{10}-J_{11}-L_{P11} and L_{P11}-J_{11}-L_{10}-J_{12}-L_{14}-J_{15}-L_{P15} loops:

$$z(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p14}i_{17} + L_{13}i_{18} + L_9 i_{12} + L_{p11}i_{13}\right) - \arcsin\left(\frac{i_{17}}{I_{c14}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) \tag{2.101}$$

$$fa(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p11}i_{13} + L_{10}i_{14} + L_{14}i_{19} + L_{p15}i_{20}\right) - \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \arcsin\left(\frac{i_{14}}{I_{c12}}\right) + \arcsin\left(\frac{i_{20}}{I_{c15}}\right) \tag{2.102}$$

The values for the nominal critical current and bias coefficient are chosen as $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The AND2 cell is simulated using JoSIM and the current distribution is extracted and compared to the values calculated through solving (2.83)-(2.102). The calculated and simulated current distribution values for the AND2 cell within the reset state are listed in Table 2.21. As the differences are negligible, the calculated values can be used to represent the current distribution within the AND2 cell for the reset state.

Table 2.21: Comparison between calculated and simulated values for current distribution for the RSFQ AND2 circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	171.074529352	171.074529382	negligible
i_2	3.925470647	3.925470617	negligible
i_3	159.062413967	159.062414033	negligible
i_4	19.863056679	19.863056584	negligible
i_5	25.291038378	25.291038337	negligible
i_6	61.743351937	61.743351765	negligible
i_7	−16.589256879	−16.589256842	negligible
i_8	171.074529352	171.074529382	negligible
i_9	3.925470647	3.925470617	negligible
i_{10}	159.062413967	159.062414033	negligible
i_{11}	19.863056679	19.863056584	negligible
i_{12}	25.291038378	25.291038337	negligible
i_{13}	61.743351937	61.743351765	negligible
i_{14}	−16.589256879	−16.589256842	negligible
i_{15}	163.067709095	163.067709159	negligible
i_{16}	11.932290904	11.932290840	negligible
i_{17}	136.350214147	136.350214164	negligible
i_{18}	−33.178513759	−33.178513685	negligible
i_{19}	50.582076756	50.582076675	negligible
i_{20}	141.821486240	141.821486314	negligible

Set A state

If the RSFQ AND2 cell receives an SFQ pulse from the input **a** branch, J_1 and J_3 will switch and undergo a 2π phase shift. A fluxon is stored within the L_{P3}-J_3-L_3-J_5-L_{P5} loop. If another input pulse from branch **a** is received while the cell is in the set A state, J_1 and J_2 will switch and undergo a 2π phase shift. The switching of J_2 ensures that J_3 will not switch under this condition. The J_2 junction thus acts as a buffer between the input port and the logic circuitry.

Appendix E provides a comprehensive study of how the current distribution within the AND2 cell changes when input pulses are received from each input branch. The current distribution for the cell within the set A state can be described through (2.83)-(2.94) and (2.96)-(2.102). The only function which has to be adapted for the set A state is function $t(\boldsymbol{i})$. Therefore (2.95) is adapted as follows:

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 + L_{p5}i_6\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right) - 2\pi \tag{2.103}$$

The comparison between the calculated and simulated values for the current distribution of the RSFQ AND2 cell in the set A state is found in Appendix F.

Set B state

Similar to the set A state, if an input SFQ pulse is present in the **b** branch, J_7 and J_9 will switch and undergo a 2π phase shift. A fluxon is then stored in the L_{p9}-J_9-L_8-J_{11}-L_{p11} loop. The J_8 junction has the same functionality as J_2.

The current distribution for the AND2 cell within the set B state can partially be described through the same functions as the reset state. The functions described through (2.83)-(2.97) and (2.99)-(2.102) remain unchanged for the set B state. However, the function $w(\boldsymbol{i})$ has to be adapted to accommodate the change in current distribution. The function in (2.98) is therefore adjusted for state set B to:

$$w(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p9}i_{10} + L_8 i_{11} + L_{p11}i_{13}\right) - \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) - 2\pi \tag{2.104}$$

Appendix F also lists the comparison between the calculated and simulated values for the current distribution of the RSFQ AND2 cell in the set B state.

Set AB state

The set AB state of the AND2 cell occurs when input pulses are received at both the **a** and **b** input branches. The current distribution within the AND2 cell for the set AB state can therefore be described through combining the resulting phase changes from the set A and set B states. The current distribution can thus be described through (2.83)-(2.94), (2.96), (2.97) and (2.99)-(2.104).

The values for the nominal critical current and bias coefficient are chosen as $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The calculated and simulated current distribution values for the AND2 cell within the reset state are listed in Table 2.22.

Table 2.22: Comparison between calculated and simulated values for current distribution for the RSFQ AND2 circuit set AB state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	138.646988075	152.786005924	−9.2541 %
i_2	36.353011924	39.862245282	−8.8034 %
i_3	2.232997350	5.274547511	−57.6647 %
i_4	209.120014574	209.587697770	−0.2231 %
i_5	−6.435979014	−6.528536174	−1.4177 %
i_6	198.461667847	198.776058231	−0.1582 %
i_7	4.222367712	4.283103364	−1.4180 %
i_8	138.646988075	152.786005924	−9.2541 %
i_9	36.353011924	39.862245282	−8.8034 %
i_{10}	2.232997350	5.274547511	−57.6647 %
i_{11}	209.120014574	209.587697770	−0.2231 %
i_{12}	−6.435979014	−6.528536174	−1.4177 %
i_{13}	198.461667847	198.776058231	−0.1582 %
i_{14}	4.222367712	4.283103364	−1.4180 %
i_{15}	178.253498776	178.301138997	−0.0267 %
i_{16}	−3.253498776	−3.301138997	−1.4431 %
i_{17}	184.618459251	184.755933352	−0.0744 %
i_{18}	−12.871958028	−13.057072349	−1.4177 %
i_{19}	8.444735424	8.566206728	−1.4180 %
i_{20}	183.444735424	183.566206728	−0.0662 %

Circuit verification

The designed RSFQ AND2 cell is simulated using JoSIM. Phase sources are connected to the **a**, **b** and **clk** ports to replicate the phase change when SFQ pulses are received by the circuit. A JTL, as designed in Section 2.4.1 is connected to the output port **q** as the load circuit. The functionality of the cell for the reset, set A, set B and set AB states are tested. The resulting simulation graphs are shown in Fig. 2.30.

The functionality of the AND2 cell is also verified through TimEx. The extracted state diagram is shown in Fig. 2.28. The $clk \rightarrow q$ time delay is extracted as 8.5 ps.

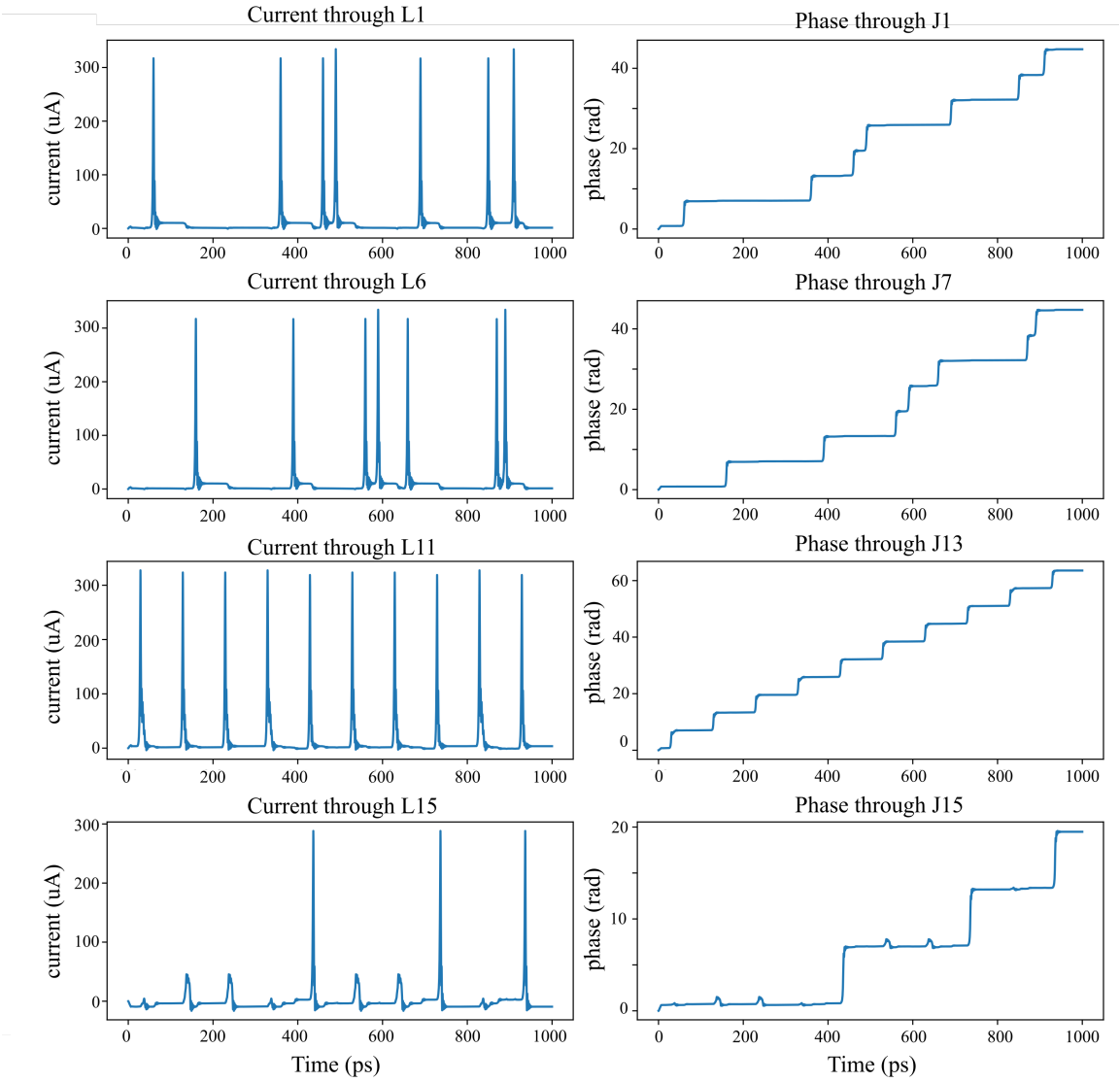


Figure 2.30: Simulation results showing the functionality of the designed RSFQ AND2 cell.

Digital model and simulation

The circuit simulation using JoSIM is known as analogue simulation. During analogue simulation, the voltages and currents within a circuit are calculated using KCL and KVL. Analogue simulation is used to simulate the electrical behaviour of a circuit while preserving the electrical elements and characteristics of a circuit.

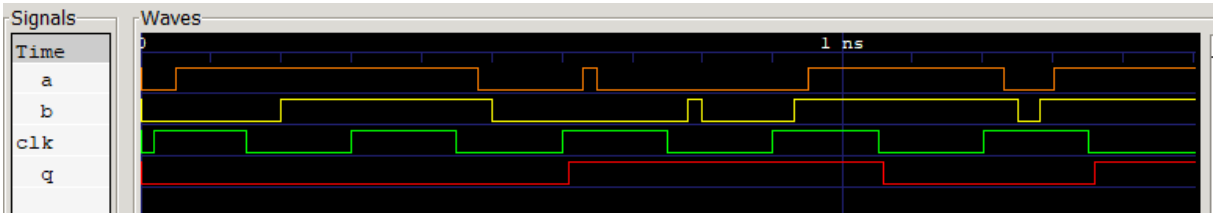


Figure 2.31: Digital simulation of designed RSFQ AND2 cell.

Digital simulation simulates the high-level behaviour of a discrete system. During digital simulation, voltage levels are used to describe the functionality of the elements within a circuit. This is also known as using logic levels to represent a digital signal. Digital simulation is often used to verify the functionality of large circuits due to the increased simulation speed. Verilog is often used to describe the digital model of a circuit.

In addition to analogue circuit verification and timing extraction, TimEx also constructs a Verilog model of the circuit. This digital model of the circuit includes the discrete circuit functionality along with time delays and critical timing parameters. The extracted digital model for the designed AND2 cell is listed in Listing 2.3. This digital model serves as an example for how the extracted time delays and critical timing parameters, extracted through TimEx, is used to analyse circuit functionality.

The digital model is simulated using a Verilog test bench circuit with the same test pattern as the analogue simulation seen in Fig. 2.30. For this example, the digital simulation is done through Icarus Verilog [55] and the results are viewed using GTKWave [56]. The resulting voltage level waves are shown in Fig. 2.31. Each change in voltage level represents the presence of an SFQ pulse at the relevant input or output port. It is seen that results of the digital simulation corresponds with the results of the analogue simulation.

Listing 2.3: RSFQ AND2 verilog model.

```
// ------------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2020 Stellenbosch University
// ------------------------------------------------------------------------------
`timescale 1ps/100fs
module AND2 (a, b, clk, q);

input
  a, b, clk;

output
  q;

reg
  q;

real
  delay_state3_clk_q = 8.5,
  ct_state0_clk_a = 5.3,
  ct_state0_clk_b = 5.3,
  ct_state1_clk_a = 6.0,
  ct_state1_clk_b = 3.9,
  ct_state2_clk_a = 3.9,
  ct_state2_clk_b = 6.0,
  ct_state3_clk_a = 4.0,
  ct_state3_clk_b = 4.0;

reg
```

```
    errorsignal_a,
    errorsignal_b,
    errorsignal_clk;

integer
    outfile,
    cell_state; // internal state of the cell

initial
    begin
        errorsignal_a = 0;
        errorsignal_b = 0;
        errorsignal_clk = 0;
        cell_state = 0; // Startup state
        q = 0; // All outputs start at 0
    end

always @(posedge a or negedge a) // execute at positive and negative edges of input
  begin
      if ($time>4) // arbitrary steady-state time)
          begin
              if (errorsignal_a == 1'b1)  // A critical timing is active for this input
                  begin
                      outfile = $fopen("errors.txt", "a");
                      $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\
                          ↪ n", $stime);
                      $fclose(outfile);
                      q <= 1'bX;  // Set all outputs to unknown
                  end
              if (errorsignal_a == 0)
                  begin
                      case (cell_state)
                          0: begin
                                cell_state = 1;  // Blocking statement -- immediately
                             end
                          1: begin
                             end
                          2: begin
                                cell_state = 3;  // Blocking statement -- immediately
                             end
                          3: begin
                             end
                      endcase
                  end
          end
  end

always @(posedge b or negedge b) // execute at positive and negative edges of input
  begin
      if ($time>4) // arbitrary steady-state time)
          begin
              if (errorsignal_b == 1'b1)  // A critical timing is active for this input
                  begin
                    outfile = $fopen("errors.txt", "a");
                    $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
                        ↪ , $stime);
                    $fclose(outfile);
                    q <= 1'bX;  // Set all outputs to unknown
                  end
              if (errorsignal_b == 0)
                  begin
                      case (cell_state)
                        0: begin
                             cell_state = 2;  // Blocking statement -- immediately
                           end
                        1: begin
                             cell_state = 3;  // Blocking statement -- immediately
                           end
                        2: begin
                           end
                        3: begin
                           end
                      endcase
```

```
            end
        end
    end

always @(posedge clk or negedge clk) // execute at positive and negative edges of input
    begin
        if ($time>4) // arbitrary steady-state time)
            begin
                if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
                begin
                    outfile = $fopen("errors.txt", "a");
                    $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
                        ↪ , $stime);
                    $fclose(outfile);
                    q <= 1'bX;  // Set all outputs to unknown
                end
                if (errorsignal_clk == 0)
                begin
                    case (cell_state)
                        0: begin
                            errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_a <= #(ct_state0_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
                            errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_b <= #(ct_state0_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
                        end
                        1: begin
                            cell_state = 0;  // Blocking statement -- immediately
                            errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_a <= #(ct_state1_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
                            errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_b <= #(ct_state1_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
                        end
                        2: begin
                            cell_state = 0;  // Blocking statement -- immediately
                            errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_a <= #(ct_state2_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
                            errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_b <= #(ct_state2_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
                        end
                        3: begin
                            q <= #(delay_state3_clk_q) !q;
                            cell_state = 0;  // Blocking statement -- immediately
                            errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_a <= #(ct_state3_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
                            errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
                            errorsignal_b <= #(ct_state3_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
                        end
                    endcase
                end
            end
    end
endmodule
```

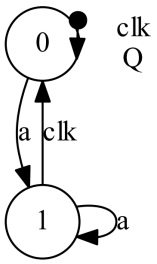


Figure 2.32: Mealy Finite State Machine diagram of the RSFQ NOT cell.

2.4.8 NOT

- This section analyses a more complex RSFQ circuit.

The NOT cell is a signal inverting cell driven by a clock pulse signal line. The NOT cell generates an output pulse if a clock pulse is received without the presence of an input signal pulse. If an input signal pulse arrives before a clock pulse, the NOT cell will not generate an output pulse. The Mealy Finite State Machine diagram for the RSFQ NOT cell is shown in Fig. 2.32. The two states illustrated in Fig. 2.32 are defined as:

1. A 'reset' state where the circuit received an input pulse at **clk**. . This state can also indicate the 'start-up' state of the circuit and is labelled as state 0.

2. A 'set A' state where an input signal from branch **a** has been received. It is indicated as state 1.

The schematic for the RSFQ NOT cell with matching JJs is shown in Fig. 2.33. The signal input port is indicated through **a** at φ_1 and the clock input port **clk** is found at φ_9. The output port **Q** is located at φ_{22}. Inductors L_4, L_6 and L_{11} are included in the schematic to comply with physical layout constraints of the circuit. These inductors can be excluded for an ideal schematic, as shown in [12]. For this example, we assume that the layout constraints are satisfied when $L_4 = L_6 = L_{11} = 0.5$ pH.

The NOT cell contains a splitter at the clock input branch, a storage loop through J_6-L_{10}-L_{11}-J_7-J_8 and two decision pairs – J_7-J_8 and J_5-J_8. Inductors L_7 and L_8, along with the resistor R_1, provides a time delay for the splitter branch leading to junction J_6. This time delay is required as the J_5 junction must switch before junction J_6 resets the circuit to the reset state. The circuit dynamics are extended upon in the relative 'Set state' and 'Reset state' subsections. For this example, we assume that the correct time delay is produced through $L_8 = 2$ pH, $L_9 = 1$ pH and $R_1 = 4\ \Omega$. The design values for the remaining components in the RSFQ NOT cell is listed in Table 2.23.

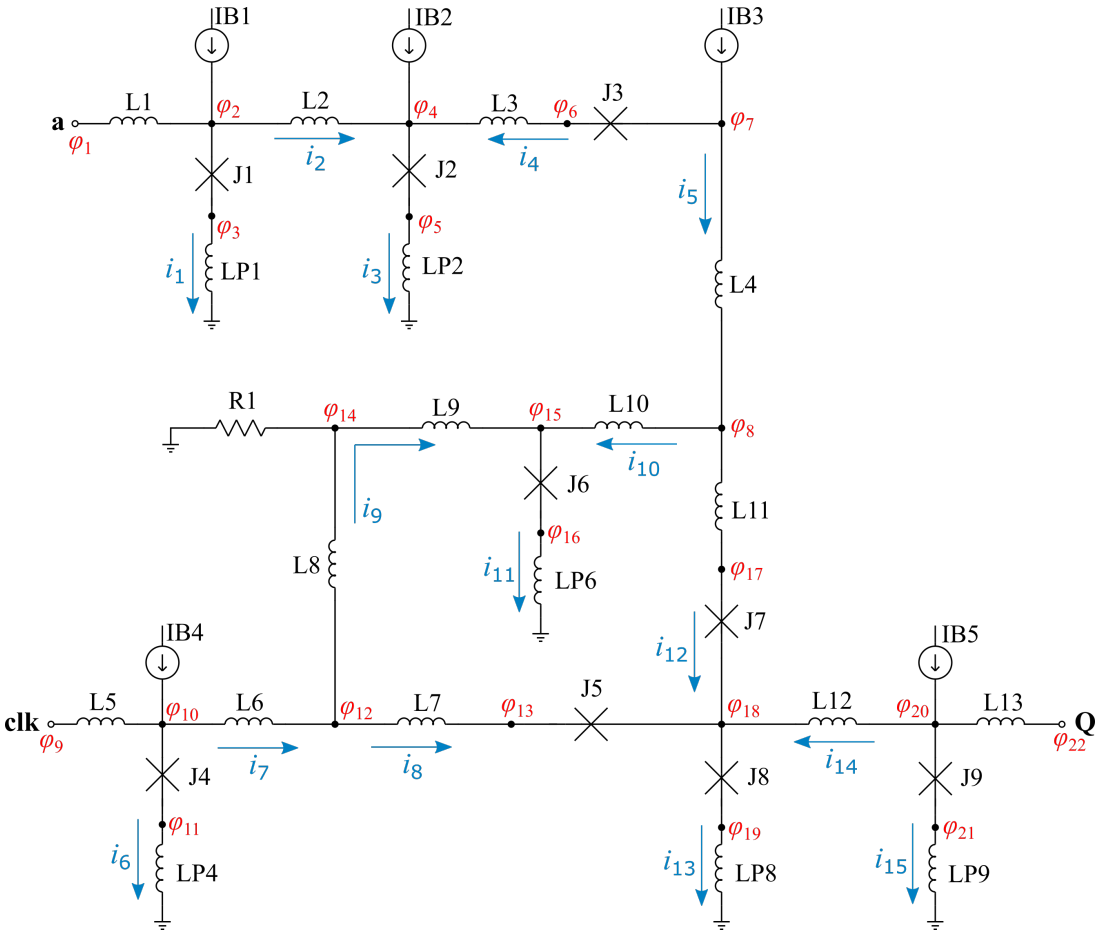


Figure 2.33: RSFQ NOT schematic.

Table 2.23: Parameter design values for RSFQ NOT cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	I_c
I_{c3}	J3 critical current	$I_c/1.4$
I_{c4}	J4 critical current	I_c
I_{c5}	J5 critical current	$I_c/1.4$
I_{c6}	J6 critical current	I_c
I_{c7}	J7 critical current	$I_c/1.4$
I_{c8}	J8 critical current	I_c
I_{c9}	J9 critical current	I_c
Bcc	Bias current coefficient	-
I_{B1}	Bias current 1	$I_{c1}B_{CC}$
I_{B2}	Bias current 2	$0.5I_{c3}$
I_{B3}	Bias current 3	$I_{c6}B_{CC}$
I_{B4}	Bias current 4	$I_{c4}B_{CC}$
I_{B5}	Bias current 5	$I_{c9}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L3$	Inductor 3	$\Phi_0/(2I_{c2})$
$L5$	Inductor 5	$\Phi_0/(4I_c)$
$L7$	Inductor 7	$\Phi_0/(2I_{c4})$
$L10$	Inductor 10	Φ_0/I_{c6}
$L12$	Inductor 12	$\Phi_0/(2I_{c8})$
$L13$	Inductor 13	$\Phi_0/(4I_c)$

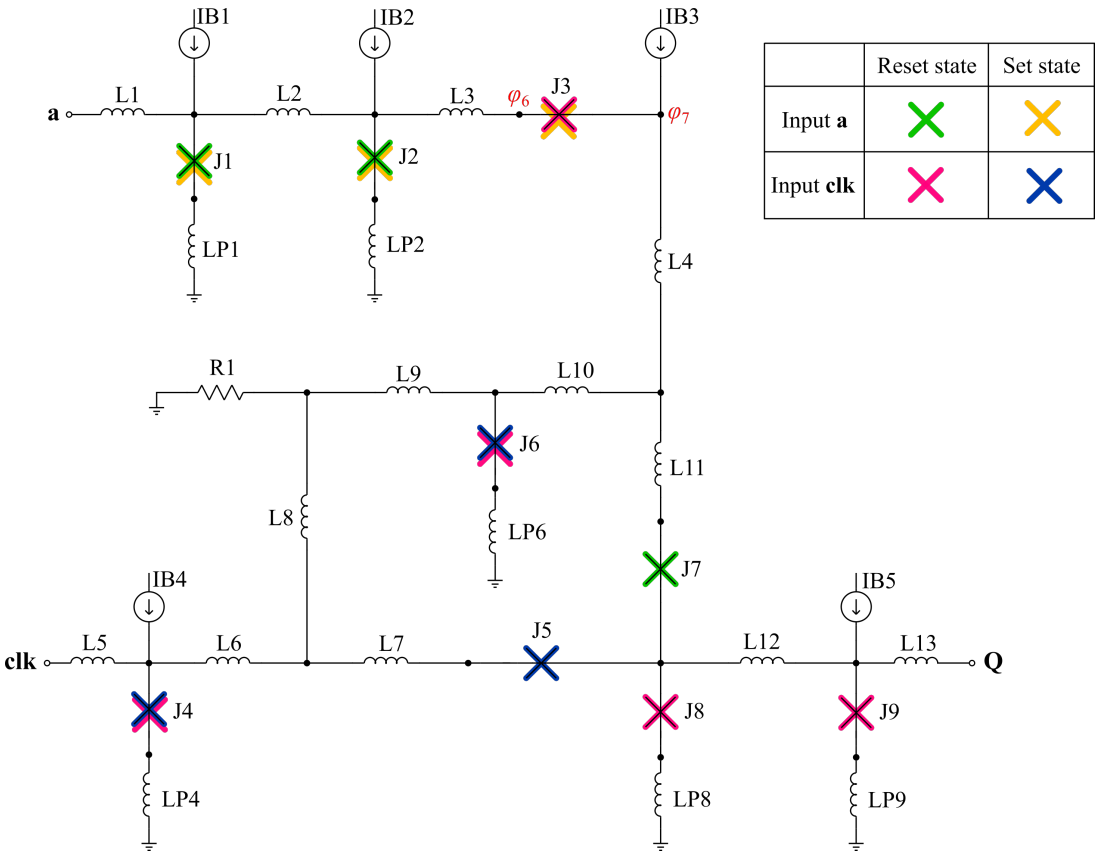


Figure 2.34: RSFQ NOT schematic indicating under which circumstances each junction will switch.

The circuit dynamics for the RSFQ NOT cell is shown in Fig. 2.34. The circumstances, regarding the state of the cell and input, under which each junction will switch is indicated within the schematic. It is important to note that if the cell is within the reset state and an input pulse is received at **clk**, the 2π phase shift over J_3 will be positive on the side of φ_7. If the NOT cell is in the set state and an input pulse is received at **a**, the 2π phase shift over J_3 will be positive on the side of φ_6.

Start-up state

The dynamics of the RSFQ NOT cell is more complex than the cells discussed in Sections 2.4.1 through 2.4.7. For this reason, the phase-based circuit equations for the NOT cell will be investigated in three states – the start-up state, the set state and the reset state. The phase-based equations will remain identical for both the start-up and reset state. The subsections are only separated to aid with the explanation of the circuit dynamics. We assume that no junctions switch when the NOT cell is in the start-up state.

The RSFQ NOT cell, illustrated in Fig. 2.33, is analysed in isolation through the following assumptions:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_9 is equal to the phase at φ_{10} so that there is no current flowing through L_5.
3. The phase at φ_{22} is equal to the phase at φ_{23} so that the current through L_{11} equals zero.

As the phase-based equations analyse the current distribution at DC, no current flows through the resistor R_1. The current through L_8 and L_9 is therefore equal for the DC analysis. The current distribution within the RSFQ NOT cell can thus be described through 15 unknowns, i_1 to i_{15}, when analysing the cell in isolation. In order to solve the 15 unknown variables using Newton's Method, 15 equations describing the current within the circuit is required. KCL is used to construct the first nine equations:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.105}$$

$$g(\boldsymbol{i}) = I_{B2} + i_2 - i_3 + i_4 \tag{2.106}$$

$$h(\boldsymbol{i}) = I_{B3} - i_4 - i_5 \tag{2.107}$$

$$k(\boldsymbol{i}) = i_5 - i_{10} - i_{12} \tag{2.108}$$

$$l(\boldsymbol{i}) = I_{B4} - i_6 - i_7 \tag{2.109}$$

$$m(\boldsymbol{i}) = i_7 - i_8 - i_9 \tag{2.110}$$

$$n(\boldsymbol{i}) = -i_9 + i_{11} - i_{10} \tag{2.111}$$

$$o(\boldsymbol{i}) = i_8 + i_{12} - i_{13} + i_{14} \tag{2.112}$$

$$p(\boldsymbol{i}) = I_{B5} - i_{14} - i_{15} \tag{2.113}$$

The phase changes through the L_{P1}-J_1-L_2-L_3-J_3-L_4-L_{11}-J_7-J_8-L_{P8} loop is described through:

$$\begin{aligned} q(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 - L_3 i_4 + L_4 i_5 + L_{11} i_{12} + L_{p8} i_{13}\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) \\ - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) \end{aligned} \tag{2.114}$$

The following equation describes the phase change through the L_{P2}-J_2-L_3-J_3-L_4-L_{10}-J_6-L_{P6} loop:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 - L_3i_4 + L_4i_5 + L_{10}i_{10} + L_{p6}i_{11}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) \tag{2.115}$$

The phase changes through the L_{P4}-J_4-L_6-L_7-J_5-L_{12}-J_9-L_{P9} and L_{P4}-J_4-L_6-L_8-L_9-J_6-L_{P6} loops are described through:

$$s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_6 + L_6i_7 + L_7i_8 - L_{12}i_{14} + L_{p9}i_{15}\right) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \arcsin\left(\frac{i_{15}}{I_{c9}}\right) \tag{2.116}$$

and

$$t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_6 + L_6i_7 + L_8i_9 + L_9i_9 + L_{p6}i_{11}\right) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) \tag{2.117}$$

The phase change through the L_8-L_9-L_{10}-L_{11}-J_7-J_5-L_7 loop is represented through:

$$u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_8i_9 + L_9i_9 - L_{10}i_{10} + L_{11}i_{12} - L_7i_8\right) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) \tag{2.118}$$

Finally, analysing the phase change in the L_{P6}-J_6-L_{10}-L_{11}-J_7-J_8-L_{P8} loop leads to:

$$v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p6}i_{11} - L_{10}i_{10} + L_{11}i_{12} + L_{p8}i_{13}\right) - \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) \tag{2.119}$$

To verify the phase-based equations in (2.105)-(2.119), the following values are chosen for the nominal critical current and the bias current coefficient: $I_c = 250\ \mu$A and $B_{CC} = 0.7$. The NOT cell is simulated in isolation using JoSIM and the resulting current distribution within the circuit is extracted. Table 2.24 lists the comparison between the calculated current values when solving (2.105)-(2.119) and the simulated current distribution values.

Table 2.24: Comparison between calculated and simulated values for current distribution for the RSFQ NOT circuit start-up state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	171.979710483	171.979710497	negligible
i_2	3.020289516	3.020289502	negligible
i_3	165.687882073	165.687882071	negligible
i_4	37.667592557	37.667592569	negligible
i_5	137.332407442	137.332407430	negligible
i_6	139.671541273	139.671541364	negligible
i_7	35.328458726	35.328458635	negligible
i_8	3.129314140	3.129314128	negligible
i_9	32.199144586	32.199144506	negligible
i_{10}	38.671467536	38.671467379	negligible
i_{11}	70.870612122	70.870611886	negligible
i_{12}	98.660939906	98.660940050	negligible
i_{13}	118.755513931	118.755513969	negligible
i_{14}	16.965259885	16.965259790	negligible
i_{15}	158.034740114	158.034740209	negligible

Set state

The NOT cell enters the set state when an SFQ pulse arrives at **a**. This causes the J_1, J_2 and J_7 junctions to switch and a fluxon is stored within the J_8-J_7-L_{11}-L_{10}-J_6 loop. The switching of a junction causes a 2π phase change over that junction. This 2π phase change over junctions J_1, J_2 and J_7 influences (2.115), (2.118) and (2.119). The equations describing the KCL, (2.105)-(2.113), along with (2.114), (2.116) and (2.117) remain unchanged from the start-up state.

The function $r(\boldsymbol{i})$ is altered as follows:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p2}i_3 - L_3 i_4 + L_4 i_5 + L_{10}i_{10} + L_{p6}i_{11}\right) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) - 2\pi \tag{2.120}$$

The phase change through the L_8-L_9-L_{10}-L_{11}-J_7-J_5-L_7 loop for the set state is represented through:

$$u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_8 i_9 + L_9 i_9 - L_{10}i_{10} + L_{11}i_{12} - L_7 i_8\right) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) + 2\pi \tag{2.121}$$

The function $v(\boldsymbol{i})$ is adjusted to:

$$v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p6}i_{11} - L_{10}i_{10} + L_{11}i_{12} + L_{p8}i_{13}\right) - \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + 2\pi \tag{2.122}$$

The RSFQ NOT cell within the set state is simulated using a phase source in JoSIM. The initial phase at φ_2 is simulated and the initial amplitude of the phase source is set to this value. To simulate an SFQ pulse at **a**, a 2π phase increase is then added to the amplitude of the phase source. The comparison between the calculated and simulated values for current distribution for the RSFQ NOT circuit within the set state is shown in Table. 2.25. The largest calculation error, 10.5 % on i_2, is due to the assumption that no current flows through inductor L_1 for both the reset and set states.

Table 2.25: Comparison between calculated and simulated values for current distribution for the RSFQ NOT circuit set state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	159.929240928	165.039873741	−3.0966 %
i_2	15.070759071	16.839099229	−10.5014 %
i_3	125.453824448	126.939163313	−1.1701 %
i_4	−14.616934623	−14.899935916	−1.8993 %
i_5	189.616934623	189.899935916	−0.1490 %
i_6	163.859760845	163.896633553	−0.0225 %
i_7	11.140239154	11.103366446	0.3321 %
i_8	32.174536358	32.151356953	0.0721 %
i_9	−21.034297203	−21.047990506	−0.0651 %
i_{10}	212.561597252	212.633621231	−0.0339 %
i_{11}	191.527300049	191.585630724	−0.0304 %
i_{12}	−22.944662629	−22.733685315	0.9280 %
i_{13}	45.770068138	45.919098781	−0.3246 %
i_{14}	36.540194409	36.501427143	0.1062 %
i_{15}	138.459805590	138.498572856	−0.0280 %

Reset state

The NOT cell enters the reset state when it receives an SFQ pulse at the clock input, **clk**, while in the set state. When the pulse at **clk** is received, junction J_4 switches and undergoes a 2π phase shift. The pulse then propagates through L_6 and splits into L_7 and L_8. The inductors L_8 and L_9, along with resistor R_1, cause a time delay so that J_5 switches before J_6. If the cell is in the set state, the stored fluxon will cause the current from I_{B3} to mainly bias J_6. Junction J_5 will therefore switch instead of J_8 as J_5 has a smaller critical current than J_8 and J_8 only has a small biasing current. One can refer to current i_{13} in Table 2.25 to evaluate the bias current of J_8 during the set state. After junction J_5 switches, J_6 switches and resets the current distribution within the cell to the start-up state. If junction J_6 switches before J_5, the cell will reset to the start-up state and the pulse through the L_7 branch will switch J_8 instead of J_5 causing the circuit to malfunction and generate an output pulse at **Q**.

If the NOT cell receives an input pulse at **clk** when in the reset state, junctions J_3, J_4, J_6, J_8 and J_9 will switch and undergo a 2π phase shift. It should be noted that the 2π phase shift over J_3 will be positive on the φ_7 side with reference to Fig. 2.32. A comprehensive study of the current distribution within the RSFQ NOT cell for all states is found in Appendix E.

Referring to the switching of junctions shown in Fig. 2.34 and the comprehensive analysis in Appendix E, it is confirmed that the phase-based equations for the NOT cell within the reset state is identical to the equations for the start-up state described through (2.105) to (2.119).

Circuit verification

The circuit functionality of the designed RSFQ NOT cell is simulated using JoSIM. Phase sources are connected to the **a** and **clk** ports to replicate the phase change when SFQ pulses are received by the circuit. A JTL, as designed in Section 2.4.1, is connected to the output port **Q** as the load circuit. The functionality of the NOT cell within the reset and set states is tested. The resulting simulation graphs are shown in Fig 2.35.

The functionality of the NOT cell is also verified through TimEx. The state diagram, extracted using TimEx, is shown in Fig. 2.32. The $clk \rightarrow q$ delay is extracted as 15.5 ps and the $clk \rightarrow clk$ critical timing for the reset state is 14.3 ps. The maximum clock frequency at which the designed NOT cell will still function correctly is approximately 70 GHz.

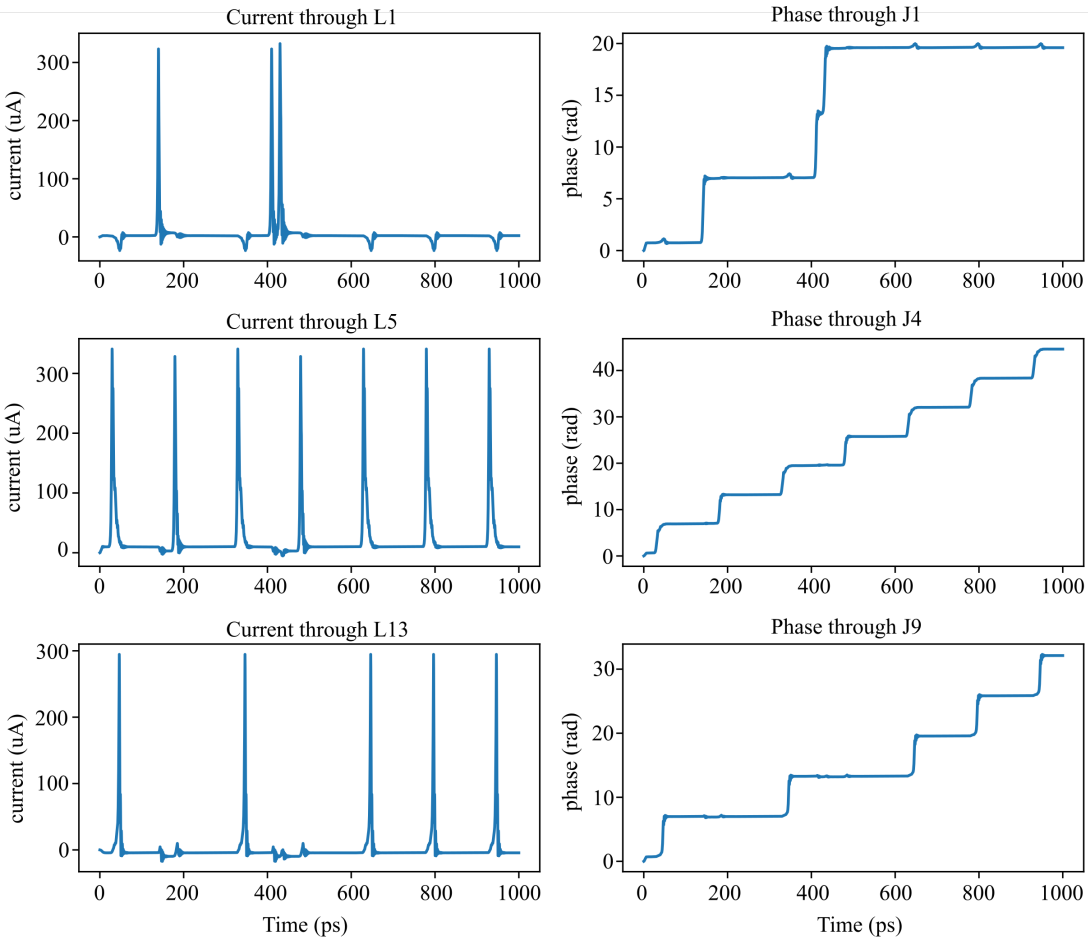


Figure 2.35: Simulation results showing the functionality of the designed RSFQ NOT cell.

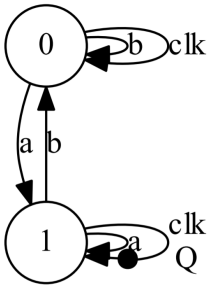


Figure 2.36: Mealy Finite State Machine diagram of the RSFQ NDRO cell.

2.4.9 NDRO

- This section introduces how an RSFQ circuit with a memory element is achieved. The section also serves as an example of the complete RSFQ cell design methodology to prepare the cell for layout.

The non-destructive readout (NDRO) cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDRO will generate an output pulse after each clock signal until an input reset signal is received. The Mealy Finite State Machine diagram of the RSFQ NDRO cell is shown in Fig. 2.36 with **a** representing the set signal, **b** the reset signal, **clk** the clock input signal and **Q** representing an output pulse. The two states illustrated in Fig. 2.36 are defined as:

1. A 'reset' state where there circuit has received a reset signal pulse from **b**. This state is marked as state 0 and also represents the start-up state where no input pulses have been received.

2. A 'set' state where an input signal pulse has been received at **a**. The cell generates an output pulse at **Q** after each input pulse received at **clk**. The state is marked as state 1 in Fig. 2.36.

The schematic for the RSFQ NDRO with matching JJs is shown in Fig. 2.37. The set signal input port **a** is located at φ_1 and the reset signal input port **b** is found at φ_7. The clock input port **clk** is located at φ_{16} while the output port **Q** is found at φ_{24}. Inductors L_7 and L_8 are included within the schematic to comply with physical layout constraints. For this example, we assume that the layout constraints are satisfied when $L_7 = L_8 = 1$ pH. The design values for the designed RSFQ NDRO is listed in Table 2.26.

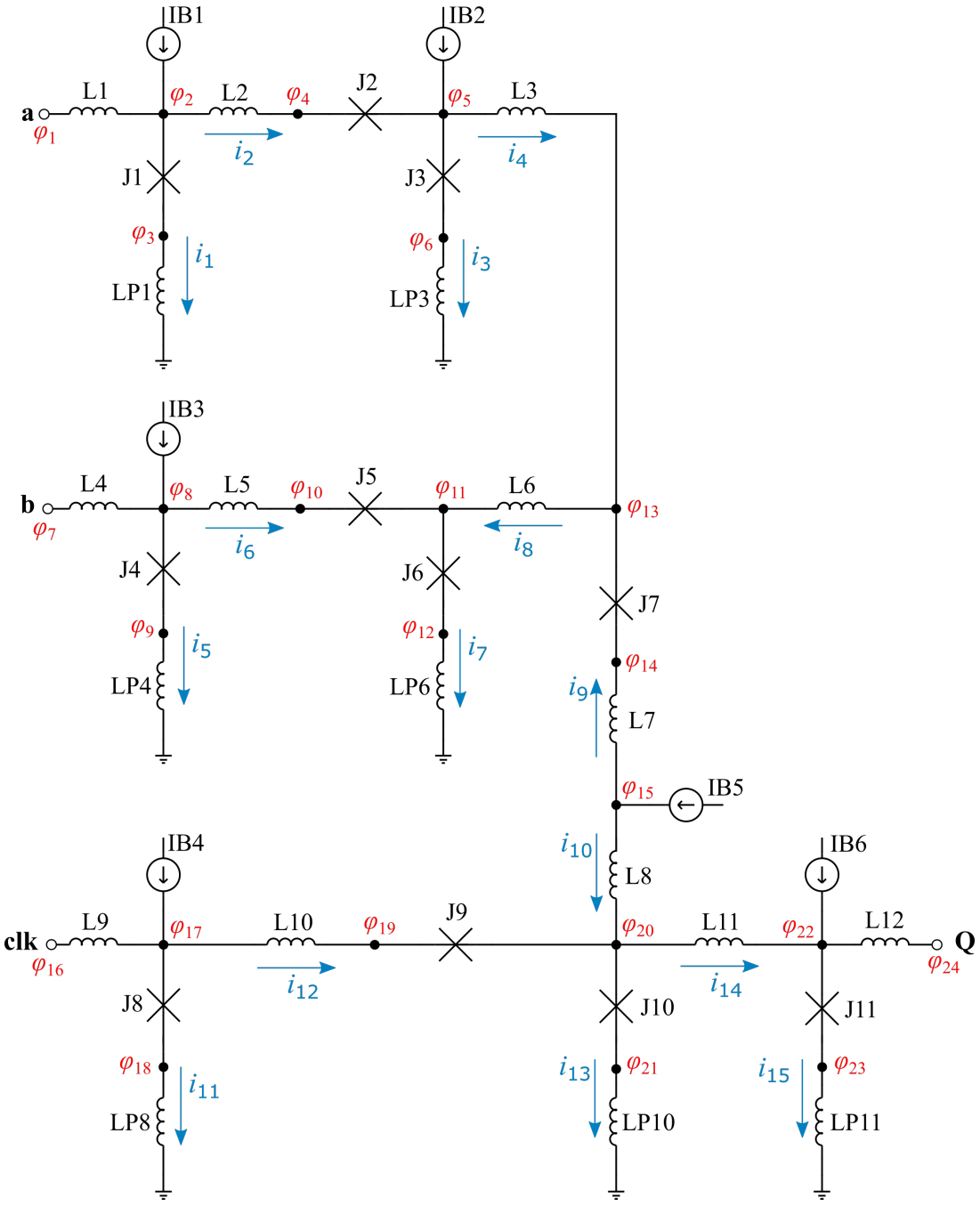


Figure 2.37: RSFQ NDRO schematic.

Table 2.26: Parameter design values for RSFQ NDRO cell.

Parameter	Definition	Description
I_c	Nominal critical current	-
I_{c1}	J1 critical current	I_c
I_{c2}	J2 critical current	$I_c/1.4$
I_{c3}	J3 critical current	I_c
I_{c4}	J4 critical current	I_c
I_{c5}	J5 critical current	$I_c/1.4$
I_{c6}	J6 critical current	I_c
I_{c7}	J7 critical current	$I_c/3$
I_{c8}	J8 critical current	I_c
I_{c9}	J9 critical current	$I_c/1.4$
I_{c10}	J10 critical current	I_c
I_{c11}	J11 critical current	I_c
Bcc	Bias current coefficient	-
I_{B1}	Bias current 1	$I_{c1}B_{CC}$
I_{B2}	Bias current 2	I_{c3}
I_{B3}	Bias current 3	$I_{c4}B_{CC}$
I_{B4}	Bias current 4	$I_{c8}B_{CC}$
I_{B5}	Bias current 5	$I_{c10}B_{CC}$
I_{B6}	Bias current 6	$I_{c11}B_{CC}$
$L1$	Inductor 1	$\Phi_0/(4I_c)$
$L2$	Inductor 2	$\Phi_0/(2I_{c1})$
$L3$	Inductor 3	$\Phi_0/(2I_{c3})$
$L4$	Inductor 4	$\Phi_0/(4I_c)$
$L5$	Inductor 5	$\Phi_0/(2I_{c4})$
$L6$	Inductor 6	$\Phi_0/(2I_{c6})$
$L9$	Inductor 9	$\Phi_0/(4I_c)$
$L10$	Inductor 10	$\Phi_0/(2I_{c8})$
$L11$	Inductor 11	$\Phi_0/(2I_{c10})$
$L12$	Inductor 12	$\Phi_0/(4I_c)$

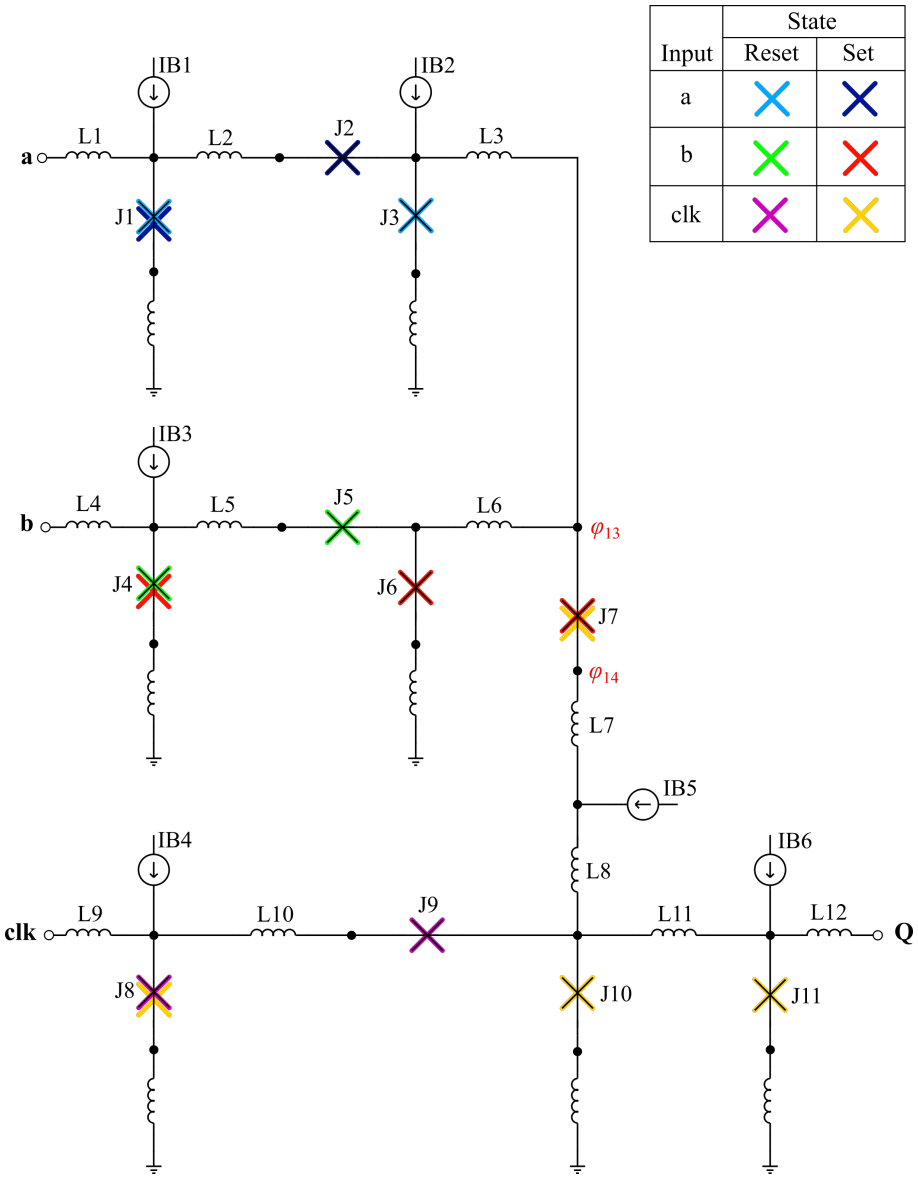


Figure 2.38: RSFQ NDRO schematic indicating under which circumstances each junction will switch.

The RSFQ NDRO contains a storage loop through J_3-L_3-L_6-J_6 which stores a fluxon when the cell is within the set state. Three decision pairs are formed through J_2-J_3, J_5-J_6 and J_9-J_{10}. Junction J_7 and J_{10} also form a decision pair when the cell is in the set state and an input pulse is received at **b**. But J_7 also acts as a buffer junction when the NDRO is in the set state and an input at **clk** is received. In this case, both J_7 and J_{10} will switch and undergo a 2π phase shift. The circuit dynamics for the NDRO is shown in Fig. 2.38. The figure also indicates the conditions under which each junction will switch. It is important to note that if the cell is within the set state and an input pulse is observed at **b**, the 2π phase shift for J_7 will be positive on the side of φ_{13}. If a clock input pulse is received when the cell is in the set state, the 2π phase shift for J_7 will be positive on the φ_{14} side.

Reset state

The reset state for the RSFQ NDRO indicates that the cell contains no stored fluxons. This condition can either occur during the start-up state when junctions have switched or when the cell was in the set state and an input signal was received at **b** prompting the switch from the set state to the reset state. Appendix E provides a comprehensive study on how the current distribution within the designed NDRO is affected when an input pulse is received at any input port in both states.

In order to analyse the current distribution within the NDRO, the cell must be analysed in isolation. The following assumptions are therefore made:

1. The phase at φ_1 is equal to the phase at φ_2 so that no current flows through L_1.
2. The phase at φ_7 is equal to the phase at φ_8 so that there is no current flowing through L_4
3. The phase at φ_{16} is equal to the phase at φ_{17} so that the current through L_9 is equal to zero.
4. The phase at φ_{22} is equal to the phase at φ_{24} so that no current flows through L_{12}.

The current distribution within the isolated NDRO can now be described through 15 unknown current values, i_1 to i_{15}. Therefore 15 functions are required to implement Newton's Method to solve the current distribution. The first nine functions are established using KCL:

$$f(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \tag{2.123}$$

$$g(\boldsymbol{i}) = I_{B2} + i_2 - i_3 - i_4 \tag{2.124}$$

$$h(\boldsymbol{i}) = i_4 - i_8 + i_9 \tag{2.125}$$

$$k(\boldsymbol{i}) = I_{B3} - i_5 - i_6 \tag{2.126}$$

$$l(\boldsymbol{i}) = i_6 - i_7 + i_8 \tag{2.127}$$

$$m(\boldsymbol{i}) = I_{B5} - i_9 - i_{10} \tag{2.128}$$

$$n(\boldsymbol{i}) = I_{B4} - i_{11} - i_{12} \tag{2.129}$$

$$o(\boldsymbol{i}) = i_{10} + i_{12} - i_{13} - i_{14} \tag{2.130}$$

$$p(\boldsymbol{i}) = I_{B6} + i_{14} - i_{15} \tag{2.131}$$

The phase change through the L_{p1}-J_1-L_2-J_2-J_3-L_{P3} loop is now evaluated to construct the function:

$$\begin{aligned} q(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p1}i_1 + L_2 i_2 + L_{p3}i_3\right) - \arcsin\left(\frac{i_1}{I_{c1}}\right) \\ + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \arcsin\left(\frac{i_3}{I_{c3}}\right) \end{aligned} \tag{2.132}$$

The functions describing the phase change through the L_{p3}-J_3-L_3-L_6-J_6-L_{p6} and L_{p4}-J_4-L_5-J_5-L_6-J_7-L_7-L_8-J_{10}-L_{p10} loops are represented through:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3i_4 + L_6i_8 + L_{p6}i_7\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_7}{I_{c6}}\right) \tag{2.133}$$

and

$$\begin{aligned} s(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p4}i_5 + L_5i_6 - L_6i_8 - L_7i_9 + L_8i_{10} + L_{p10}i_{13}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) \\ + \arcsin\left(\frac{i_6}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) \end{aligned} \tag{2.134}$$

The phase change through the L_{p8}-J_8-L_{10}-J_9-J_{10}-L_{p10} loop is described through:

$$\begin{aligned} t(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p8}i_{11} + L_{10}i_{12} + L_{p10}i_{13}\right) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) \end{aligned} \tag{2.135}$$

The last two functions required for Newton's Method describes the phase change through the L_{p6}-J_6-L_6-J_7-L_7-L_8-J_9-L_{10}-J_8-L_{p8} and L_{p3}-J_3-L_3-J_7-L_7-L_8-L_{11}-J_{11}-L_{p11} loops:

$$\begin{aligned} u(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p6}i_7 - L_6i_8 - L_7i_9 + L_8i_{10} - L_{10}i_{12} + L_{p8}i_{11}\right) - \arcsin\left(\frac{i_7}{I_{c6}}\right) \\ - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \arcsin\left(\frac{i_{11}}{I_{c8}}\right) \end{aligned} \tag{2.136}$$

$$\begin{aligned} v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3i_4 - L_7i_9 + L_8i_{10} + L_{11}i_{14} + L_{p11}i_{15}\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) \\ - \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right) \end{aligned} \tag{2.137}$$

The critical current is chosen as $I_C = 250\ \mu$A and the bias current coefficient as $B_{CC} = 0.7$. Newton's Method is now used to solve the unknown currents i_1 to i_{15} in (2.123) to (2.137). The resulting calculated values are compared to the simulated values for the reset state in Table 2.27. It is seen that the differences for the reset state are negligible.

Table 2.27: Comparison between calculated and simulated values for current distribution for the RSFQ NDRO circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	186.884569992	186.884570008	negligible
i_2	−11.884569992	−11.884570008	negligible
i_3	215.934768809	215.934768978	negligible
i_4	22.180661197	22.180661013	negligible
i_5	151.729256020	151.729256068	negligible
i_6	23.270743979	23.270743931	negligible
i_7	68.937987703	68.937987528	negligible
i_8	45.667243724	45.667243596	negligible
i_9	23.486582526	23.486582582	negligible
i_{10}	151.513417473	151.513417417	negligible
i_{11}	171.302981405	171.302981404	negligible
i_{12}	3.697018594	3.697018595	negligible
i_{13}	160.017609116	160.017609056	negligible
i_{14}	−4.807173048	−4.807173043	negligible
i_{15}	170.192826951	170.192826956	negligible

Set state

The RSFQ NDRO cell enters the set state when an input pulse at **a** is received. This input pulses causes J_1 and J_2 to switch and undergo a 2π phase shift. The functions described through (2.123) to (2.131) are constructed using KCL and remain unchanged regardless of which state the NDRO is in. Appendix E provides a comprehensive study on how the switching of J_1 and J_2 affect the functions described through (2.132) to (2.137). It is found that (2.132) and (2.134)-(2.136) remain unchanged when the NDRO enters the set state. The function $r(\boldsymbol{i})$ in (2.133) is adapted as follows:

$$r(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 + L_6 i_8 + L_{p6} i_7\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \arcsin\left(\frac{i_7}{I_{c6}}\right) - 2\pi \quad (2.138)$$

The $v(\boldsymbol{i})$ function in (2.137) requires the following adaption to account for the 2π phase shifts:

$$\begin{aligned} v(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(-L_{p3}i_3 + L_3 i_4 - L_7 i_9 + L_8 i_{10} + L_{11} i_{14} + L_{p11} i_{15}\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) \\ - \arcsin\left(\frac{i_9}{I_{c7}}\right) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right) - 2\pi \end{aligned} \quad (2.139)$$

Newton's method is used to solve the unknown current values for the set state described through (2.123)-(2.132), (2.134)-(2.136), (2.138) and (2.139). The resulting current distribution is compared to the simulated values within Table 2.28. It is seen that the largest calculation errors are found on i_1 to i_3. It is expected that the largest calculation errors will be on the current values near port **a** as the current leakage through L_1 for the set state is not taken into account within the phase-based equations.

Table 2.28: Comparison between calculated and simulated values for current distribution for the RSFQ NDRO circuit set state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	143.473263383	162.969717562	−11.9632 %
i_2	31.526736616	36.519366122	−13.6712 %
i_3	27.035778910	31.228708249	−13.4265 %
i_4	254.490957705	255.290657872	−0.3133 %
i_5	176.507751509	176.618318670	−0.0626 %
i_6	−1.507751509	−1.618318670	−6.8322 %
i_7	180.836787650	181.258207070	−0.2325 %
i_8	182.344539160	182.876525740	−0.2909 %
i_9	−72.146418545	−72.414132132	−0.3697 %
i_{10}	247.146418545	247.414132132	−0.1082 %
i_{11}	187.659224423	187.711693684	−0.0280 %
i_{12}	−12.659224423	−12.711693684	−0.4128 %
i_{13}	218.153106987	218.301126464	−0.0678 %
i_{14}	16.334087133	16.401311983	−0.4099 %
i_{15}	191.334087133	191.401311983	−0.0351 %

Circuit verification

The functionality of the designed RSFQ NDRO cell is now verified through a JoSIM simulation. The resulting simulation plots are shown in Fig. 2.39. The functionality is also verified through TimEx. The extracted state machine diagram is shown in Fig. 2.36. The $clk \rightarrow q$ delay for the NDRO in the set state is extracted as 6.5 ps and the $clk \rightarrow clk$ critical timing is extracted as 10.3 ps.

Operating margins

The operating margins for the designed RSFQ NDRO cell is shown in Fig. 2.40. The critical margin for the cell is set at 10.1 % on junction J_3. The current distribution within the matching junctions B_1, B_4, B_8 and B_{11} is now constrained to $0.7I_c$. The bias current sources I_{B1}, I_{B3}, I_{B4} and I_{B6} are converted to variables within (2.123) to (2.137). The tuned bias current source values are calculated as $I_{B1} = 0.639I_c$, $I_{B3} = 0.818I_c$, $I_{B4} = 0.717I_c$ and $I_{B6} = 0.725I_c$. The resulting operating margins for the NDRO with tuned bias current sources are shown in Fig. 2.41. It is seen that the critical margin for the circuit only increases slightly to 11.7 % on B_{10}.

The NDRO is now run through JoSIM-tools to optimise the circuit. Constraints are put on the size of the matching junctions as well as the current sources which bias the matching junctions. This is done to keep the phases of the input and output ports constant to minimise current leakage when connecting the NDRO to the other designed RSFQ cells. The resulting operating margins for the optimised NDRO is shown in Fig. 2.42. The critical margin of the cell increased significantly with circuit optimisation. The critical margin is now 29.6 % for junction B_6.

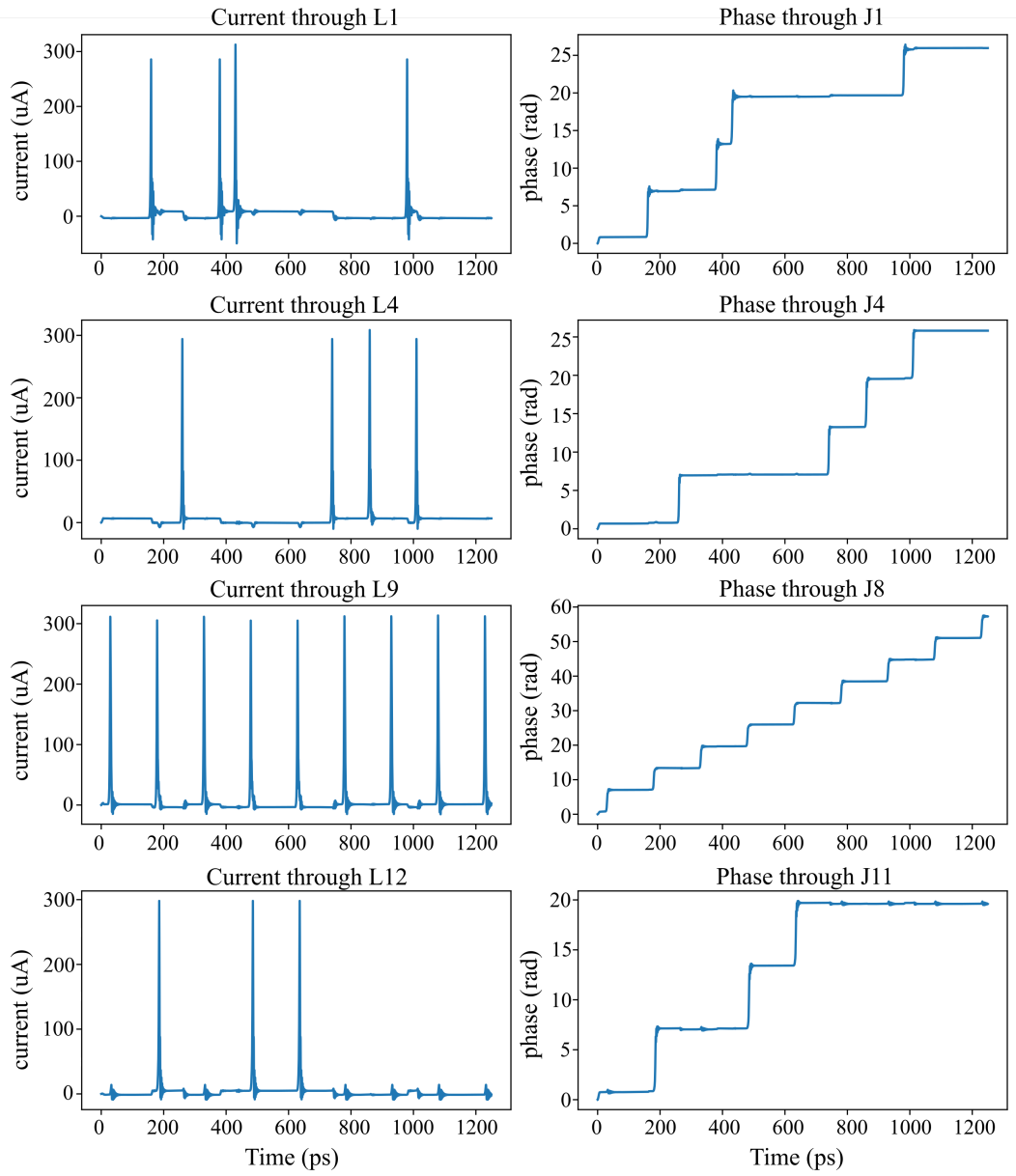


Figure 2.39: Simulation results showing the functionality of the designed RSFQ NDRO cell.

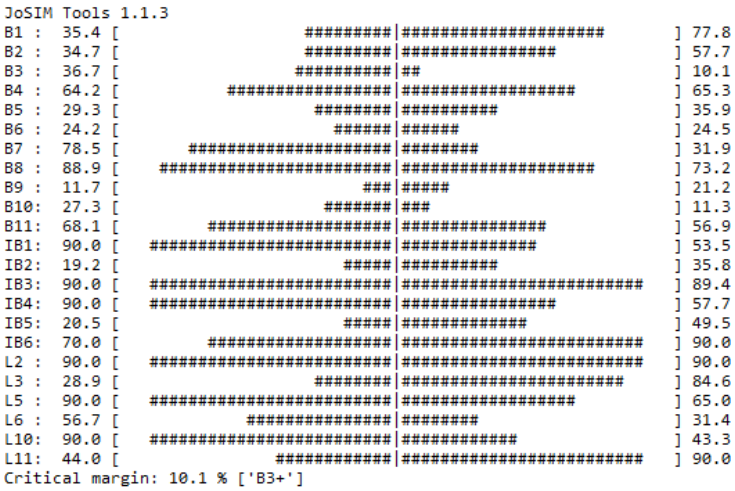


Figure 2.40: Operating margins of the designed RSFQ NDRO cell.

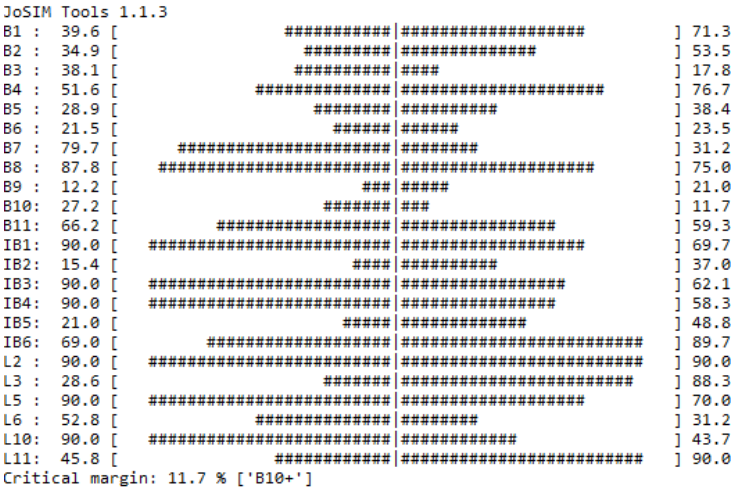


Figure 2.41: Operating margins of the RSFQ NDRO cell with tuned bias current source values.

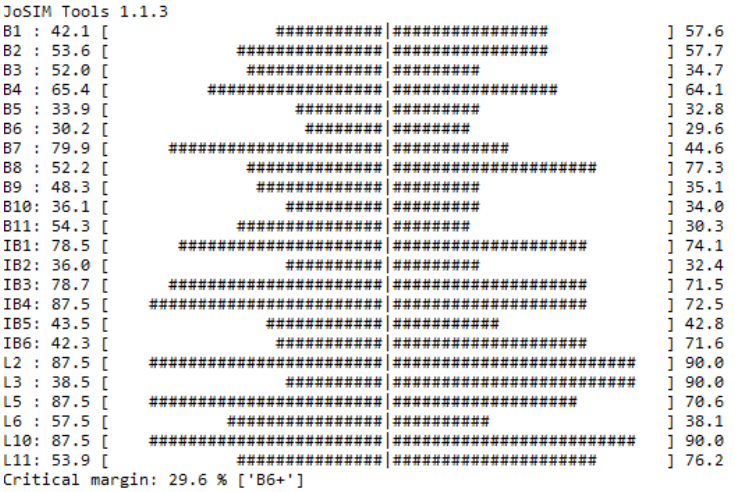


Figure 2.42: Operating margins of the optimised RSFQ NDRO cell.

Yield analysis

The comparative yield roll-off curves for the original designed, tuned and optimised RSFQ NDRO cell are shown in Fig. 2.43. The optimised NDRO cells has a 100 % yield at 0.2 parameter standard deviation. Both the original designed and the tuned versions have a 99.9 % yield at 0.2 standard deviation. The optimised NDRO cell has a yield of 99.6 % at 0.25 standard deviation. The optimised RSFQ NDRO cell can therefore be considered the circuit which will be the most robust towards fabrication tolerances.

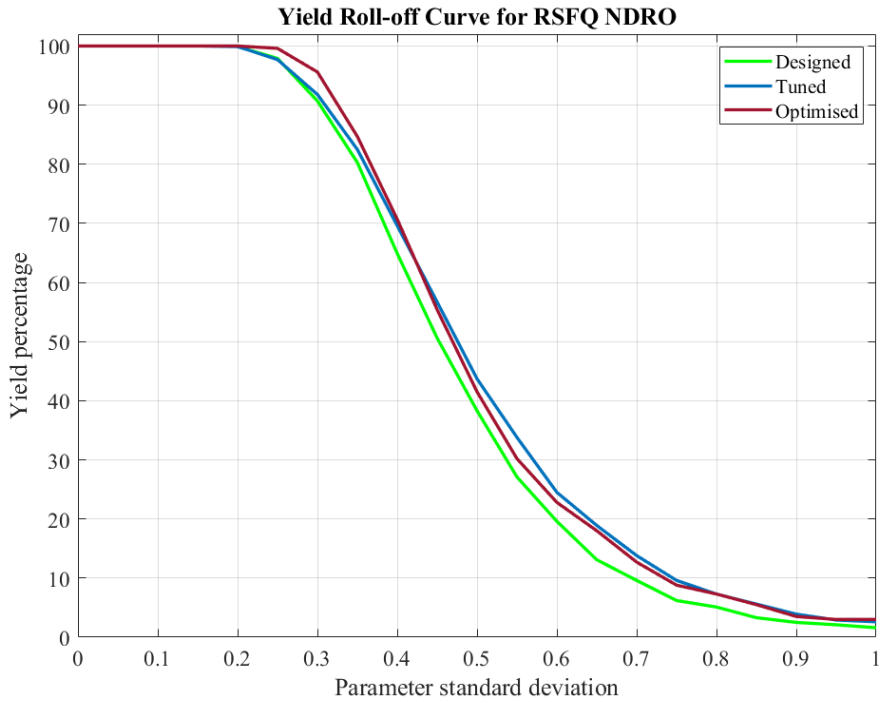


Figure 2.43: Yield roll-off curve for the designed, tuned and optimised RSFQ NDRO cell.

Digital model and simulation

The digital model of the designed RSFQ NDRO is extracted using TimEx and is found in Listing 2.4. The test bench for the digital simulation is set up to display a similar input pattern as the analogue simulation in Fig. 2.39. The resulting voltage level waves are shown in Fig. 2.44. It is seen that the digital model has similar behaviour as the analogue model specified in the circuit netlist.

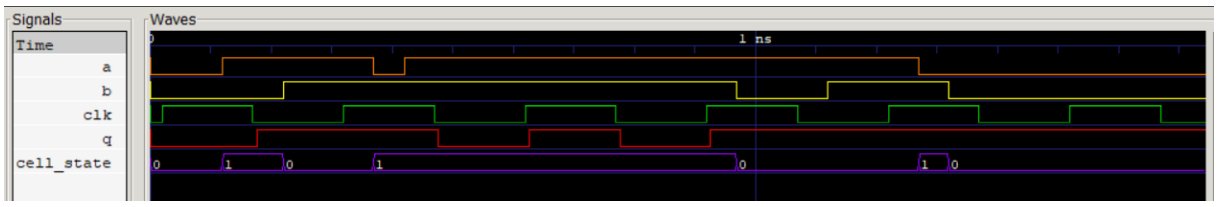


Figure 2.44: Digital simulation of designed RSFQ NDRO cell

Listing 2.4: RSFQ NDRO verilog model.

```
// ------------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2020 Stellenbosch University
// ------------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_NDRO (a, b, clk, q);

input
  a, b, clk;

output
  q;

reg
  q;

real
  delay_state1_clk_q = 6.5,
  ct_state0_b_a = 0.3,
  ct_state1_b_a = 2.3,
  ct_state1_clk_b = 0.3,
  ct_state1_clk_clk = 10.3;

reg
   errorsignal_a,
   errorsignal_b,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\
                     ↪ n", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                        end
                     1: begin
                        end
                  endcase
               end
         end
   end

always @(posedge b or negedge b) // execute at positive and negative edges of input
   begin
```

```
        if ($time>4) // arbitrary steady-state time)
            begin
                if (errorsignal_b == 1'b1)  // A critical timing is active for this input
                begin
                    outfile = $fopen("errors.txt", "a");
                    $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\
                        ↪ n", $stime);
                    $fclose(outfile);
                    q <= 1'bX;  // Set all outputs to unknown
                end
                if (errorsignal_b == 0)
                begin
                    case (cell_state)
                        0: begin
                                errorsignal_a = 1;  // Critical timing on this input; assign
                                    ↪ immediately
                                errorsignal_a <= #(ct_state0_b_a) 0;  // Clear error signal
                                    ↪ after critical timing expires
                            end
                        1: begin
                                cell_state = 0;  // Blocking statement -- immediately
                                errorsignal_a = 1;  // Critical timing on this input; assign
                                    ↪ immediately
                                errorsignal_a <= #(ct_state1_b_a) 0;  // Clear error signal
                                    ↪ after critical timing expires
                            end
                    endcase
                end
            end
    end

always @(posedge clk or negedge clk) // execute at positive and negative edges of input
    begin
        if ($time>4) // arbitrary steady-state time)
            begin
                if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
                begin
                    outfile = $fopen("errors.txt", "a");
                    $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\
                        ↪ n", $stime);
                    $fclose(outfile);
                    q <= 1'bX;  // Set all outputs to unknown
                end
                if (errorsignal_clk == 0)
                begin
                    case (cell_state)
                        0: begin
                            end
                        1: begin
                                q <= #(delay_state1_clk_q) !q;
                                errorsignal_b = 1;  // Critical timing on this input; assign
                                    ↪ immediately
                                errorsignal_b <= #(ct_state1_clk_b) 0;  // Clear error signal
                                    ↪ after critical timing expires
                                errorsignal_clk = 1;  // Critical timing on this input; assign
                                    ↪  immediately
                                errorsignal_clk <= #(ct_state1_clk_clk) 0;  // Clear error
                                    ↪ signal after critical timing expires
                            end
                    endcase
                end
            end
    end

endmodule
```

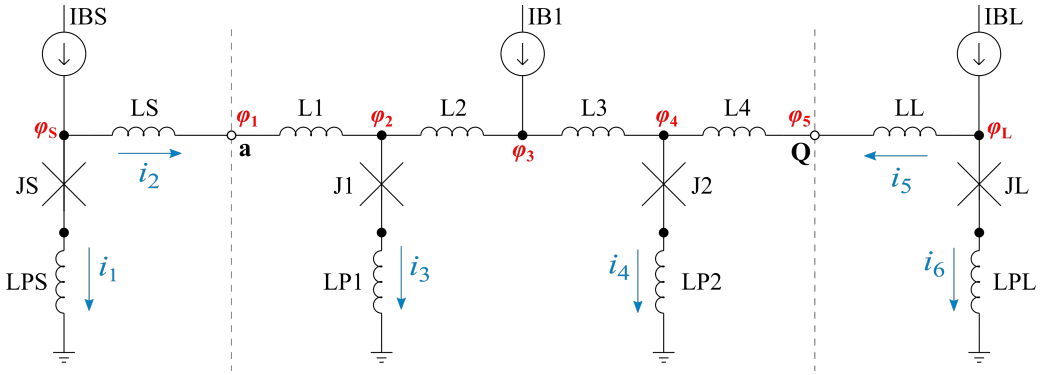


Figure 2.45: JTL with source and load circuits.

2.5 Current Leakage and Load Balancing

Current leakage within RSFQ circuits can be defined as DC current through a component, typically an inductor, when no DC current is expected. For the cells designed from Section 2.4.1 to 2.4.9, current leakage is typically found in the input and output inductors when the cells are connected to unbalanced sources and loads. Load balancing is important when cells are designed to be directly connected together.

Figure 2.45 shows an example of a JTL cell connected to source and load circuits. If the connected circuits are unbalanced, current will flow through L_S-L_1, L_4-L_L or both L_S-L_1 and L_4-L_L. This current leakage will cause the junctions within the source, JTL and load circuits to have differing bias current than what was designed. To prevent current leakage, φ_S must be equal to φ_1 and φ_2, so that $i_2 = 0$ μA. Similarly, $\varphi_4 = \varphi_5 = \varphi_L$ so that $i_5 = 0$ μA. It is important to note that current leakage is more prevalent when cells have more than one state, as the phase over the input/output junction changes depending on which state the cell is in. Adding additional matching JJs can reduce the effects of current leakage for multi-state cells, but there is a circuit size trade-off when adding these additional JJs.

The JTL, OR2, XOR and DFF cells have been tuned to establish a fixed phase over the input and output matching junctions during the start-up state and reset states. These tuned cells can also be referred to as the load balanced cells. The test circuit shown in Fig. 2.46 is constructed to test the operating margins for these load balanced RSFQ cells. The design values of the nominal critical current and the bias current coefficient are set to $I_c = 250$ μA and $B_{CC} = 0.7$ for this simulation. The operating margins of the test

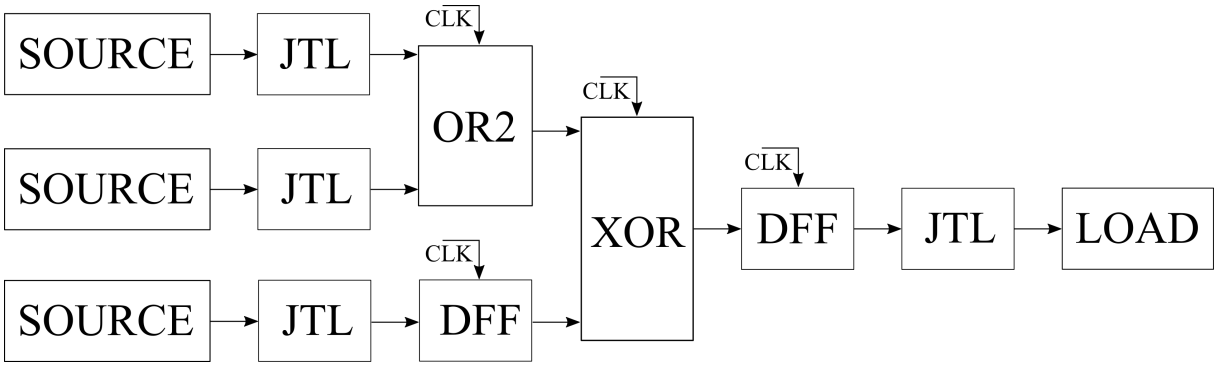


Figure 2.46: Test circuit set-up to analyse global operating margins.

circuit, constructed using the original designed cells, are shown in Fig. 2.47. It is seen that the global current variable sets the critical margin of the circuit at 10.6 %. The margin I_c is also investigated within Fig. 2.47. The total variation that I_c can undergo without causing circuit malfunction is ±30 % when I_c has a nominal value of $I_c = 250$ μA. The test circuit is now simulated using the load balanced cells to construct the circuit. The resulting global operating margins are shown in Fig. 2.48. The figure shows that implementing the load balanced cells increases the critical margin of I_{global} to 12.6 %. I_c can also undergo a variation of −52.6 % to 28.0 % before circuit malfunction occurs.

```
JoSIM Tools 1.1.3
Bglobal:  25.8 [                    ######|#####                    ] 19.2
Lglobal:  24.7 [                    ######|####                     ] 18.0
Iglobal:  10.6 [                      ##|####                       ] 18.0
Ic      :  30.0 [                   #######|########                ] 33.7
Critical margin: 10.6 % ['Iglobal-']
```

Figure 2.47: Operating margins of RSFQ test circuit with original designed RSFQ cells.

```
JoSIM Tools 1.1.3
Bglobal:  26.6 [                    ######|########                 ] 32.6
Lglobal:  18.9 [                      ####|########                 ] 32.3
Iglobal:  18.9 [                      ####|###                      ] 12.6
Ic      :  54.6 [              ###############|#######               ] 28.0
Critical margin: 12.6 % ['Iglobal+']
```

Figure 2.48: Operating margins of RSFQ test circuit with load balanced RSFQ cells.

It is important to note that load balancing only accounts for the current leakage when the connected cells are both within the start-up or reset state. It is therefore implausible to design multi-state RSFQ cells with certainty that no current leakage will occur when a direct connection to another cell is made. One solution for this problem is designing RSFQ cells that are connected using PTLs [21], [57], [58].

2.6 Conclusion

An education quality method for analysing RSFQ cells using phase-based equations has been formalised. Examples have been discussed on how this method can be altered to improve the design of the specified cell through establishing constraints on current distribution within the cell. The influence of multiple cell states on the phase-based equations were discussed. Various methods to verify circuit functionality were also reviewed. The concept of analysing operating margins and the yield percentage of circuits was introduced. Lastly, the effect of current leakage and loaf balancing for RSFQ circuits was explored.

Chapter 3

Passive Transmission Lines

3.1 Introduction

RSFQ cells can be connected through non-storing inductor loops, JTLs or PTLs to assemble larger circuits. RSFQ cells which cannot be placed directly next to one another, to form a non-storing inductive loop, have to be routed together with either JTLs, or PTLs. The type of connection used is determined by the required power consumption, transmission delays and routing space available on the chip. Superconductor PTLs provide a notable SFQ pulse propagation speed advantage when compared to JTLs [59]. PTLs also require less routing space than JTLs. However, PTL connections do come with a drawback as impedance mismatching between the RSFQ cells and PTL can cause SFQ pulse reflections [20]. These SFQ pulse reflections can cause timing jitter [22], [23] which can affect the operating margins of RSFQ cells.

This chapter presents a published article which analyses the trade-offs between various methods for improving impedance mismatching caused by PTL connections. The effectiveness of each method for minimising pulse reflections is analysed through circuit simulation. PTL transmitter and receiver circuits for the MIT-LL SFQ5ee process are presented with the aim of reducing SFQ pulse reflection.

3.2 Published Work

All relevant work, attached in Appendix B, is published in

- L. Schindler, P. le Roux and C. J. Fourie, "Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells," IEEE Transactions on Applied Superconductivity, vol. 30, no. 2, pp. 1-7, March 2020, Art no. 1300607, doi: 10.1109/TASC.2020.2964542.

3.3 Summary of Research Contribution

- The advantages and disadvantages of using PTLs with the MIT-LL SFQ5ee fabrication process were analysed.
- Impedance matching for PTL transmitters and receivers using an established reflection coefficient was investigated. The results were compared to results obtained

in [60] for the AIST STP2 fabrication process. It was confirmed that impedance models for RSFQ circuits can be established for various fabrication processes.

- Various optimisation methods were compared and the resulting operating margins for the circuits were analysed. This resulted in establishing constraints on circuit components connected to PTLs during parameter optimisation.
- The sensitivity of the reflection coefficient to the biasing current of the designed receiver circuit was investigated.
- The results obtained within the published work led to a better understanding on how cells connected to PTLs behave and how an RSFQ library with integrated PTL transmitters and receivers can be improved to minimise reflections caused by PTL connections.

3.4 Conclusion

Methods to improve impedance mismatch when implementing PTL connections, for the MIT-LL SFQ5ee fabrication process, were discussed. The effectiveness of each method was analysed through simulation and the operating margins for the RSFQ cells were analysed. It was found that the most efficient way to reduce SFQ pulse reflections, due to PTL impedance mismatch, is by connecting PTL transmitters and receivers to the RSFQ cells. The layout space overhead can also be decreased if the PTL transmitters and receivers are integrated within RSFQ cells. The RSFQ cell library presented in Chapter 4 applies the results from this published work to improve impedance mismatching caused by PTL connections.

Chapter 4

RSFQ Cell Library for Layout Synthesis

The methodology for establishing standardised cell layout synthesis presented within this chapter formed part of the oral presentation at ISEC 2019 [61]. The resulting conference paper [42] is attached in Appendix D. The work also contributed to a published paper regarding the design and characterisation of track routing architecture for RSFQ and AQFP circuits in a multilayer process [41]. This article is included in Appendix C.

4.1 Introduction

Numerous RSFQ cell libraries, such as the SUNY at Stony Brook [52], the IPHT cell library [62] and the Japanese CONNECT library [49], have been developed, but such libraries are often outdated or unavailable to the public. The work within this chapter therefore focuses on the development of a portable and open-source RSFQ cell library as described in [63]. The cell library developed within this chapter is based on optimised versions of the cells described in Chapter 2 and have integrated PTL transmitters and receivers. This chapter will focus on how the cell layouts can be standardised for the Massachusetts Institute of Technology Lincoln Laboratory (MIT-LL) SFQ5ee fabrication process [64]. The PTL transmitter (PTLTX) and PTL receiver (PTLRX) cells are included within the library to advance interoperability with other cell libraries. The following core cells are included in the MIT-LL RSFQ cell library:

Interconnects: JTLT, SPLITT, MERGET, PTLTX and PTLRX.

Logic cells: AND2T, OR2T, XORT and NOTT.

Buffers: DFFT and NDROT.

Interfacing cells: DCSFQ, DCSFQ-PTLTX, PTLRX-SFQDC and SFQDC.

The full documentation for the RSFQ logic cell library within the ColdFlux logic cell library document is included in Appendix K. Additional cells used for clock splitting and clock balancing are also included, but are relatives of the JTLT and SPLITT cells. Versions of these additional cells without integrated PTL transmitters and receivers are also available to construct a clocking network without the need for PTL connections.

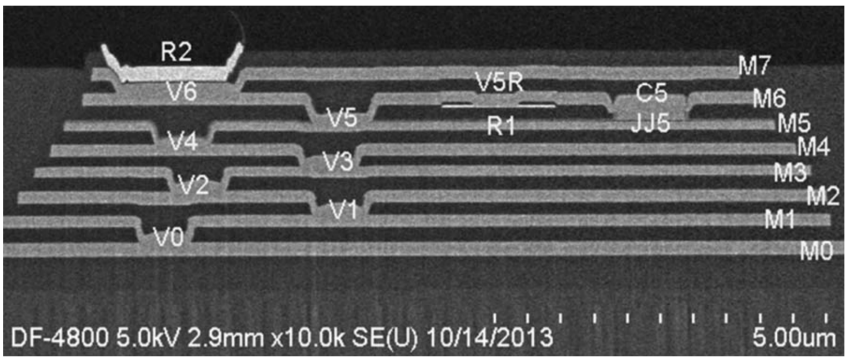


Figure 4.1: Scanning electron microscope (SEM) image of wafer cross section fabricated using the SFQ4ee fabrication process. Figure taken from [64]

4.2 Layout

The MIT-LL SFQ5ee process is based on the Nb/Al-AlOx/Nb tri-layer technology with a critical current density of 100 $\mu A/\mu m^2$ [65]. The fabrication process has eight superconductor layers, M0 to M7, and is a close relative of the MIT-LL SFQ4ee fabrication process shown in Fig. 4.1. The Josephson junctions are indicated through JJ5, the resistor layers through R1 and R2 and the vias between superconductor layers through V0 to V6. V5R indicates the vias connecting M6 to the resistor layer R1.

4.2.1 Layout track

Flux trapping within superconductor circuits can affect the operating margins of RSFQ circuits or can cause the circuit to completely malfunction. Moats are placed within superconducting ground planes to create low energy locations for flux trapping [66]–[69]. These moats help lower the probability trapped fluxons near JJs and inductors. Experiments regarding the influence of the placement, shape and size of moats are discussed in [70]. These experiments lead to the ability to simulate and analyse trapped flux within a layout using InductEx [71].

The MIT-LL SFQ5ee fabrication process also has several strict design rules regarding layer density, minimum distance between elements and maximum element size [72]. The requirement for moats and maximum layer density is combined to create the basis for the MIT-LL SFQ5ee track block shown in Fig. 4.2. The moats are represented by the 'No fill' cutout within Fig. 4.2. The track block provides a 10×10 μm template block from which an RSFQ cell layout is built.

4.2.2 Bias grid design

The RSFQ cells are biased through connecting resistors to a DC voltage biasing line. These bias lines carry current which couples to superconductor circuit loops [41]. To minimise the bias lines coupling with individual RSFQ cells, a single bias pillar per cell is used for the RSFQ cell library. The bias pillar is then split within the individual cell and ground plane to sky plane connections are inserted to form a shield around the internal bias grid. The RSFQ OR2T cell, shown in Fig. 4.3, provides an example of how an internal bias grid is implemented for this research. It is important to note that the internal bias grid must not form a loop around the cell as this will also cause unwanted

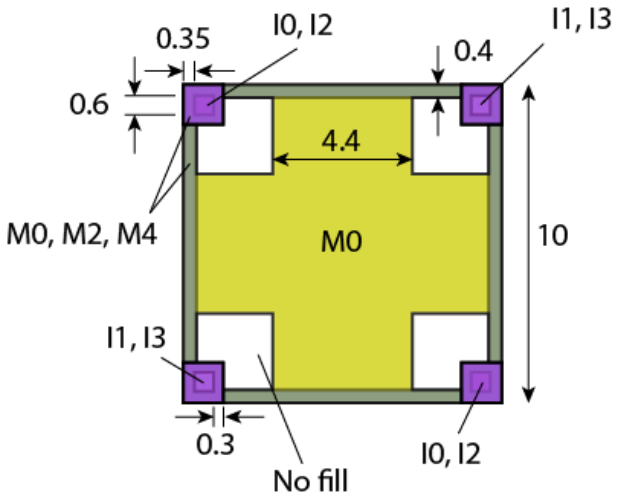


Figure 4.2: The basic track block for the MIT-LL SFQ5ee fabrication process. All dimensions are in μm. Figure taken from [41].

coupling. The implementation of an internal bias grid does come with a size trade-off, but often this allows the minimum layer density for layers with fewer structures, such as the JJ5 layer, to be realised. Josephson junction fill structures are also included within the OR2T layout in Fig. 4.3. These 'fake' JJs are not connected to any active elements and do not influence the functionality of the cell.

4.2.3 RSFQ logic cell library

The layouts for the RSFQ cell library are designed to have a fixed height and variable width. This convention allows for the RSFQ cells to be tightly stacked to form larger circuits. An example of how a larger circuit is synthesised is discussed in Section 4.4. The values for circuit elements within the layout, such as inductors, resistors and JJ areas, are extracted using InductEx [25], [26].

Connections between the ground plane and sky plane are scattered throughout each RSFQ cell layout. These connections create a stitching effect between the ground plane and sky plane which shortens the path of return currents [73]. A lack of stitching can cause return currents to be spread over a large surface of the ground plane. These currents can produce flux which can dramatically affect the operating margins of the circuit [73]. Fig. 4.4 shows how the ground plane is connected to the sky plane using elements of a shunted JJ to ground. The sky plane itself is omitted from the figure to improve the visibility of the via connections.

The layouts for all RSFQ cell library cells are found within the ColdFlux logic cell library document included in Appendix K.

4.3 Interface cells

Interface cells for RSFQ logic cells include a DCSFQ and SFQDC cell. The DCSFQ cell is designed to convert input voltage pulses into SFQ pulses. The SFQDC cell is designed to converts SFQ pulses to an output voltage level which can be measured by standard equipment. Two versions of each interface cell is available: one with either an integrated PTL transmitter or receiver and one without this PTL connection compatibility.

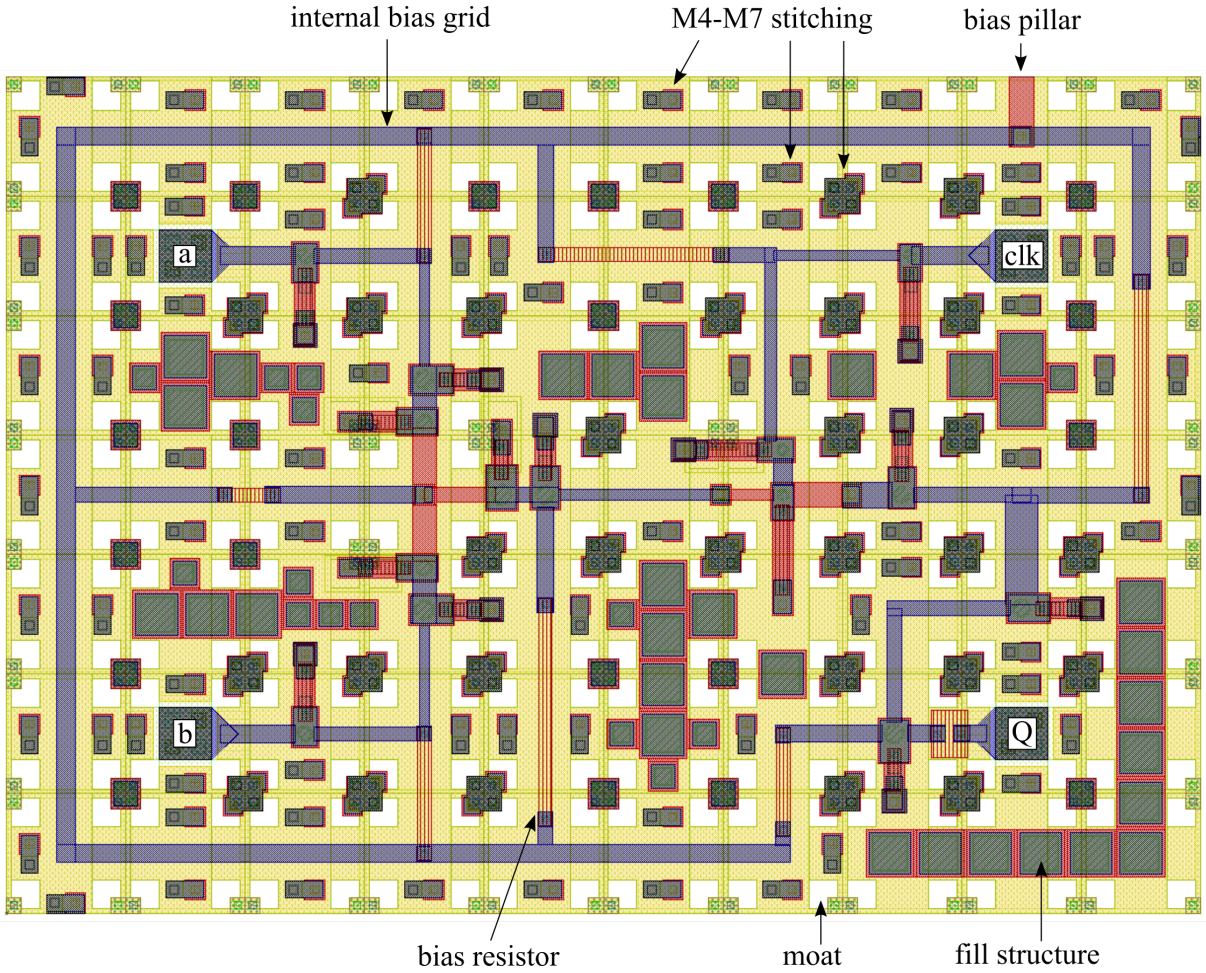


Figure 4.3: Layout of the RSFQ OR2T cell for the MIT-LL SFQ5ee process.

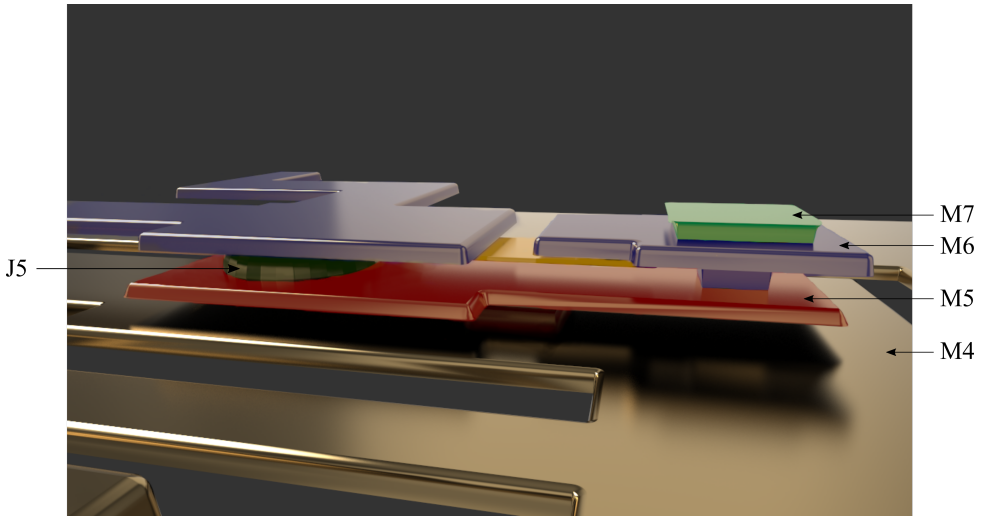


Figure 4.4: 3D model of shunted junction with connections to the ground plane and sky plane. Figure adapted from [74].

4.4 Layout Synthesis

The MIT-LL RSFQ cell library was developed with the aim that larger circuit layouts can be easily synthesised without the need to first adapt the cell layouts. To demonstrate the layout readiness of the RSFQ cell library, the layout of a 4-bit Kogge-Stone adder (KSA) using PTL connections was synthesised by J. de Villiers [75]. A segment of the GDS layout of the synthesised KSA is shown in Fig. 4.5. The layer fill segments are excluded to improve visibility of the PTLs and contact pads. The PTLs are routed on two separate layers and are shielded from coupling when crossing other PTLs.

4.5 Conclusion

This chapter presented an example portable RSFQ cell library for layout synthesis. The MIT-LL SFQ5ee fabrication process was briefly introduced. A layout track for the MIT-LL SFQ5ee process, which can be used as a basis for RSFQ and AQFP cell layouts, was demonstrated. The challenges of biasing larger RSFQ circuits were listed and an internal bias grid solution presented. Finally, an example layout of the construction of a synthesised 4-bit KSA with PTL connections was demonstrated.

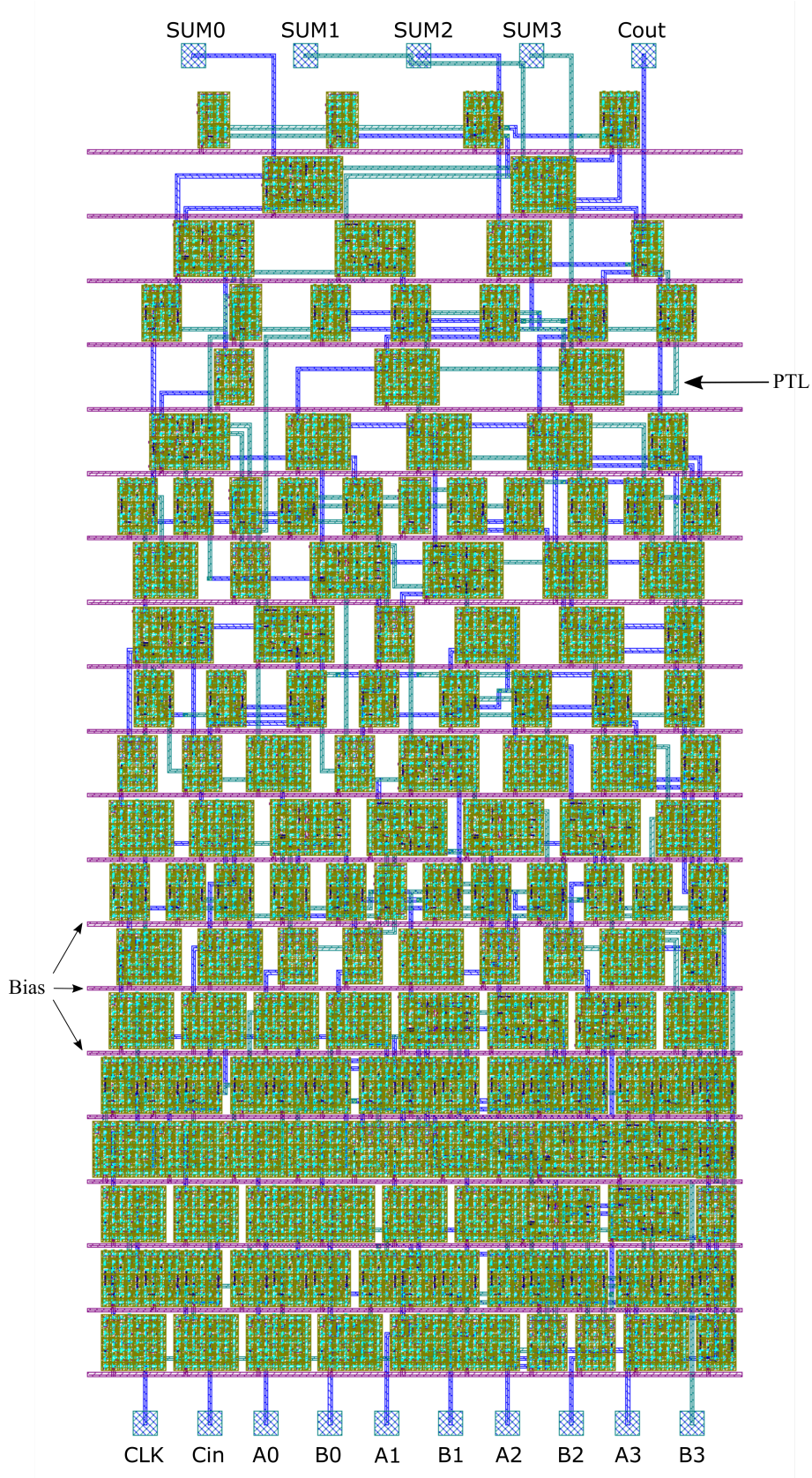


Figure 4.5: Layout of synthesised 4-bit KSA using the MIT-LL RSFQ cell library.

Chapter 5

Circuit Fabrication and Testing

5.1 Introduction

The SuperTools program presented several opportunities for circuit fabrication. Three chips containing several RSFQ circuit experiments, as well as circuit timing and resonance experiments were submitted for fabrication. This chapter presents preliminary measured results for some of these experiments on the fabricated chips. The test manuals for how the circuits should be measured, and which measurements are important, are also included.

5.2 Fabricated Circuits

Three chips (named SUMLL01-MRC, SUMLL02-MRC and SUMLL03) have been designed for fabrication. The test circuits on the chip are designed to test multiple characteristics of the RSFQ cell library developed in Chapter 4 along with Magnetic Rule Checking (MRC) experiments. The chips were fabricated by MIT-LL. Measurements for SUMLL01-MRC were conducted by NIST and preliminary measurements for SUMLL02-MRC have also been received. Due to the 2020 COVID-19 pandemic and global lockdowns, the lead time for chip production and result measurement has increased dramatically; presently more than 12 months from design submission. We aim to publish the measured results for all three chip designs when fabrication and testing has been completed.

5.2.1 SUMLL01-MRC

The first chip submitted, named SUMLL01-MRC, was developed to establish the functionality of the RSFQ DCSFQ and SFQDC cells as well as determining the robustness of these cells when exposed to magnetic fields. The GDS layout for the SUMLL01-MRC chip is shown in Fig. 5.1. The fill structures for the chip are removed to improve visibility of the test circuits and pads. The RSFQ experiments placed on the chip included three variations of the same basic test to confirm the functionality of the DCSFQ and SFQDC cells. If these core cells do not function as expected, all other results from larger experiments will be obsolete. Two chips containing identical SUMLL01-MRC designs were fabricated by MIT-LL. The chips were tested by a team at NIST following the test manual included in Appendix H. The flux trapping experiments included in SUMLL01-MRC were set up by Dr. K. Jackman and Prof. C. J. Fourie and results are published within [70].

The first experiment, named RSFQ01, contains a DCSFQ-JTL-SFQDC cell sequence with ground 'curtains'. The 'curtain' refers to the circuit being surrounded by connections

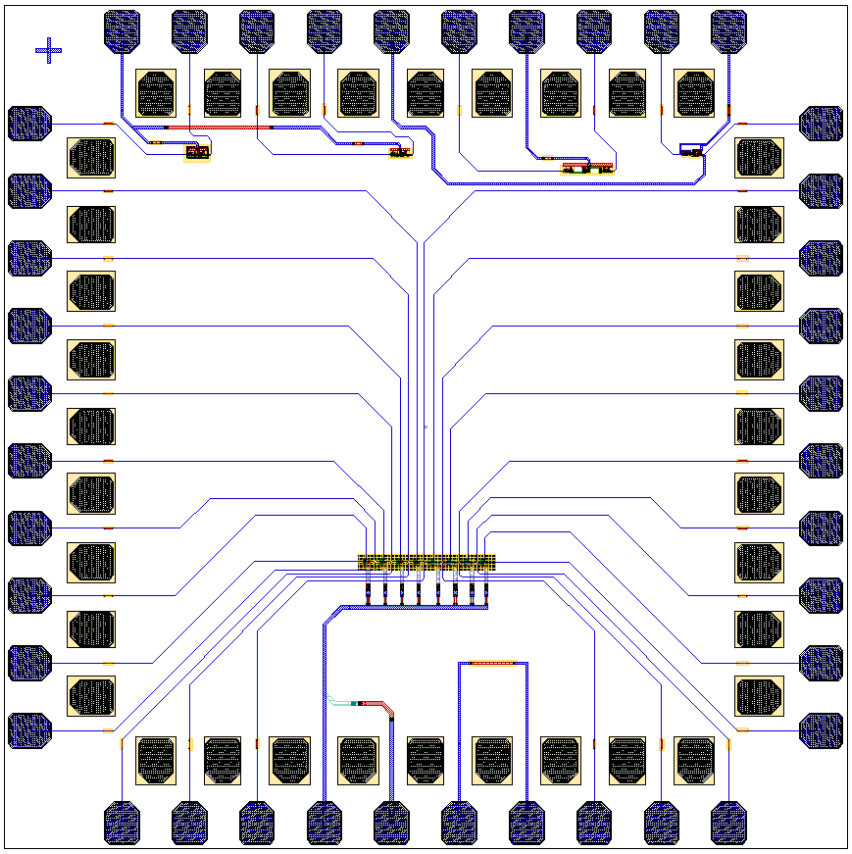
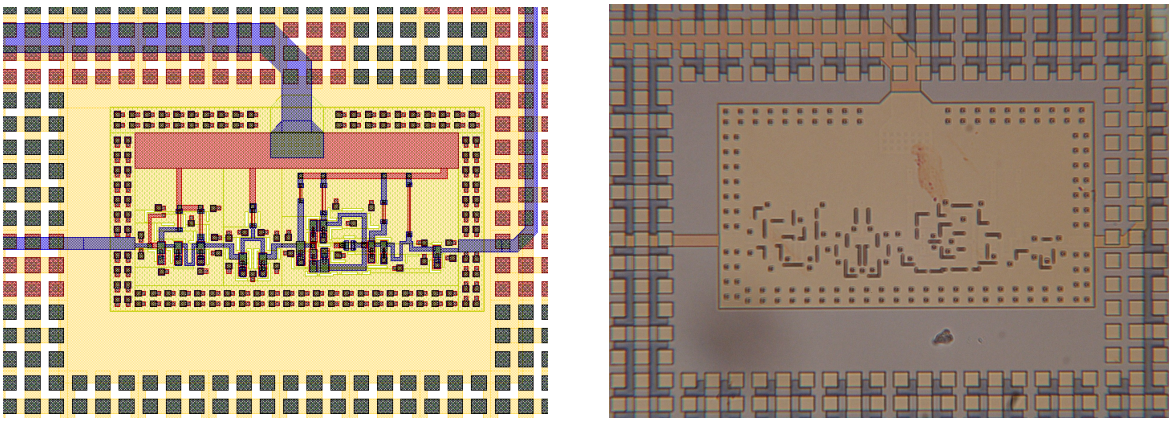


Figure 5.1: Chip SUMLL01-MRC layout for fabrication.

between the ground plane and sky plane. This is generally done as a technique to shield a circuit from external magnetic flux. A portion of the GDS layout is shown in Fig. 5.2a. The sky plane is omitted from the figure to improve visibility of the RSFQ cells and connections. It should be noted that the layouts used for SUMLL01-MRC and SUMLL02-MRC do not contain the layout track presented in Chapter 4.2 as these chips were submitted for fabrication before collaborative work on the layout track began. The fabricated circuit is shown in Fig. 5.2b. The circuit elements are not visible on the fabricated circuit as the circuit is fabricated to include a sky plane. The two SUMLL01-MRC chips containing RSFQ01 were tested by a team at NIST. An example voltage level measurement of a functional DCSFQ-JTL-SFQDC cell sequence is shown in Fig. 5.3. The measured output pulse train frequency is half of the input pulse train frequency due to the SFQDC. The input signal in Fig. 5.3 is offset by 20 mV for improved visibility. The measured bias current margins for both fabricated chips are listed in Table 5.1. The RSFQ01 maintained correct functionality on chip 2 for input signal amplitudes between 380 μA and 935 μA. The nominal input signal amplitude was designed to be 600 μA. Measurements regarding the input signal amplitude margins for chip 1 were not provided.

The second experiment, named RSFQ02, repeats the DCSFQ-JTL-SFQDC cell sequence in RSFQ01, but does not contain the ground 'curtains' around the circuit. The GDS layout for RSFQ02 is shown in Fig. 5.4a and the fabricated circuit in Fig. 5.4b. The biasing margins for both fabricated RSFQ02 experiments are listed in Table 5.1. The RSFQ02 maintained correct functionality on chip 2 for input signal amplitudes between 320 μA and 900 μA.



(a) (b)

Figure 5.2: The GDS layout (a) and fabricated circuit (b) for the RSFQ01 experiment on SUMLL01-MRC.

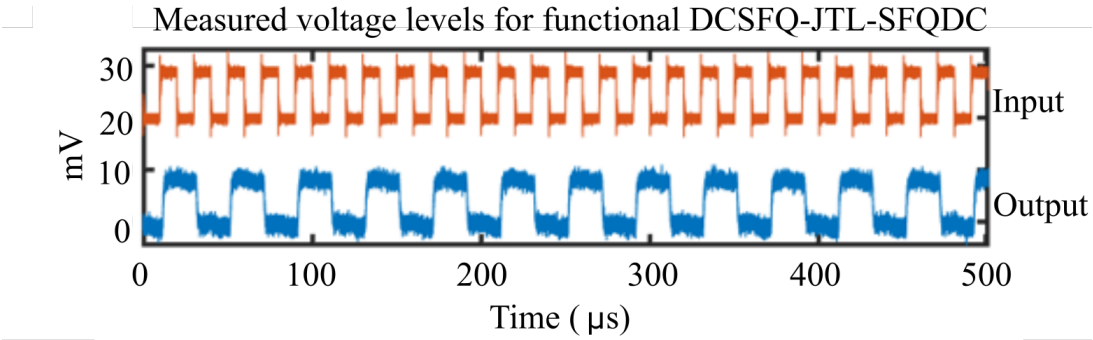
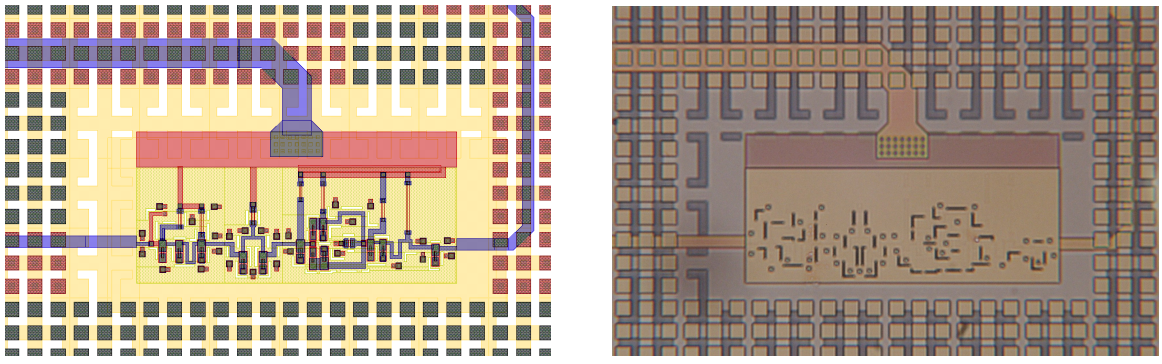
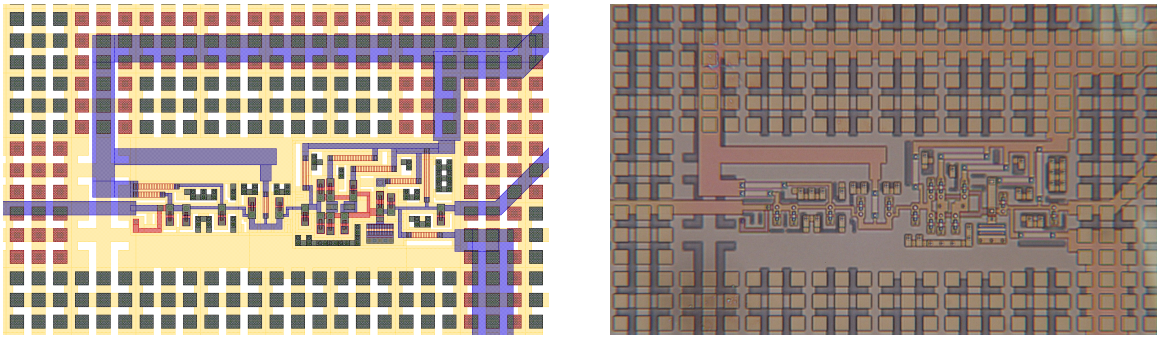


Figure 5.3: Example of voltage measurements showing correct functionality for the RSFQ01, RSFQ02 and RSFQ03 experiments on SUMLL01-MRC.



(a) (b)

Figure 5.4: The GDS layout (a) and fabricated circuit (b) for the RSFQ02 experiment on SUMLL01-MRC.



(a) (b)

Figure 5.5: The GDS layout (a) and fabricated circuit (b) for the RSFQ03 experiment on SUMLL01-MRC.

The third experiment, named RSFQ03, repeats the DCSFQ-JTL-SFQDC cell sequence, but does not include the sky plane. The experiment was submitted to determine the effect of a lack of shielding provided by a sky plane. The aim was to compare the bias current margins to the margins of RSFQ01 and RSFQ02. Fig. 5.5 shows the GDS layout of the test circuit compared to the fabricated circuit. The layout had to be adapted from RSFQ01 and RSFQ02 as the inductance values change when no sky plane is present. InductEx was used to ensure that the extracted inductances in RSFQ03 are identical to RSFQ01 and RSFQ02. The circuit elements are visible on the fabricated circuit as no sky plane is shielding the circuitry. The measured voltage levels showing an example of a malfunctioning RSFQ03 experiment on chip 1 is shown in Fig. 5.6. It is suspected that trapped fluxons cause JJs to switch unexpectedly which leads to circuit malfunction. Another possibility is that the circuit malfunction is caused by a fabrication error. The RSFQ03 experiment on chip 2 functioned as expected. The measured bias margins for RSFQ03 are listed in Table 5.1. No measurement information regarding the input signal amplitude margins for RSFQ03 were provided.

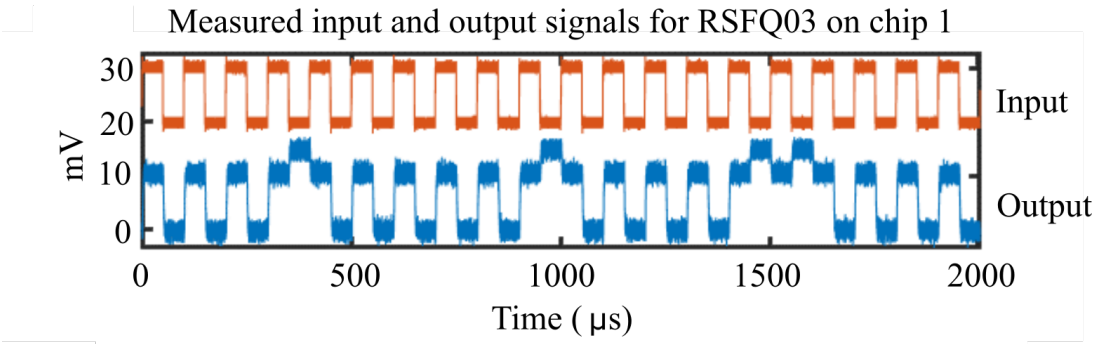


Figure 5.6: Voltage measurements showing an example of malfunction on the RSFQ03 experiment from the SUMLL01-MRC chip.

Table 5.1: Measured results for RSFQ experiments from SUMLL01-MRC.

	Expected bias margins	Measured bias margins
RSFQ01 chip 1	2.448 - 3.672 mA	2.54 - 3.50 mA
RSFQ01 chip 2	2.448 - 3.672 mA	2.50 - 3.80 mA
RSFQ02 chip 1	2.448 - 3.672 mA	2.68 - 3.37 mA
RSFQ02 chip 2	2.448 - 3.672 mA	2.70 - 3.58 mA
RSFQ03 chip 1	1.414 - 2.122 mA	Malfunction
RSFQ03 chip 2	1.414 - 2.122 mA	1.52 - 2.18 mA

5.2.2 SUMLL02-MRC

The SUMLL02-MRC chip was designed to test the functionality of some basic RSFQ cells developed for the SuperTools program. The circuits on this chip were designed to test the model accuracy and performance of the tools developed under the ColdFlux project. PTLs were used for pulse transmission to also verify the layouts used for the PTL as well as the integrated PTL transmitters and receivers of the ColdFlux RSFQ cell library. The GDS layout of the SUMLL02-MRC chip is shown in Fig. 5.7. The fill structures are removed from the figure to improve visibility of the experiments. Two chips containing the SUMLL02-MRC design were manufactured by MIT-LL. Preliminary measured results were done by NIST following the test manual found in Appendix I. Five RSFQ experiments were set up to test the functionality of some of the RSFQ cells developed under the ColdFlux project. The first experiment, named RSFQ01, consists of a DCSFQ-PTLTX-JTLT-PTLRX-SFQDC cell sequence. The second and third experiments, named RSFQ02 and RSFQ03 respectively, consist of a DCSFQ-PTLTX-DFFT-PTLRX-SFQDC cell sequence. The cells within RSFQ02 are connected with straight PTLs while RSFQ03 investigates the effect of PTL corners on pulse transmission. The fourth experiment, named RSFQ04, consists of a DCSFQ-PTLTX-NOTT-PTLRX-SFQDC cell sequence. The fifth experiment, RSFQ05, analyses the functionality of a DCSFQ-PTLTX-OR2T-PTLRX-SFQDC cell sequence. Corners are also included in the PTL interconnects in RSFQ05. The GDS layouts for all five RSFQ experiments on SUMLL02-MRC is shown in Fig. 5.8. Preliminary measured results for the RSFQ experiments on SUMLL02-MRC are listed in Table 5.2. Measurements not yet received are marked with N/A.

To verify the throughput delays calculated by TimEx, two timing experiments, TIMING01 and TIMING02, were constructed. TIMING01 analyses the time delay of a JTL circuit by comparing the time delay of four abutted JTLs to five abutted JTLs. A single input line is split within the circuit and each SFQ pulse is transmitted to the abutted JTLs. The bias line of the five abutted JTLs can be tuned until the time delay is the same as that of four abutted JTLs. A JJ comparator was designed to only produce an output SFQ pulse if two pulses reach the cell within 0.5 ps of each other. Comprehensive measurements have not yet been received and the aim is to publish the results once measured.

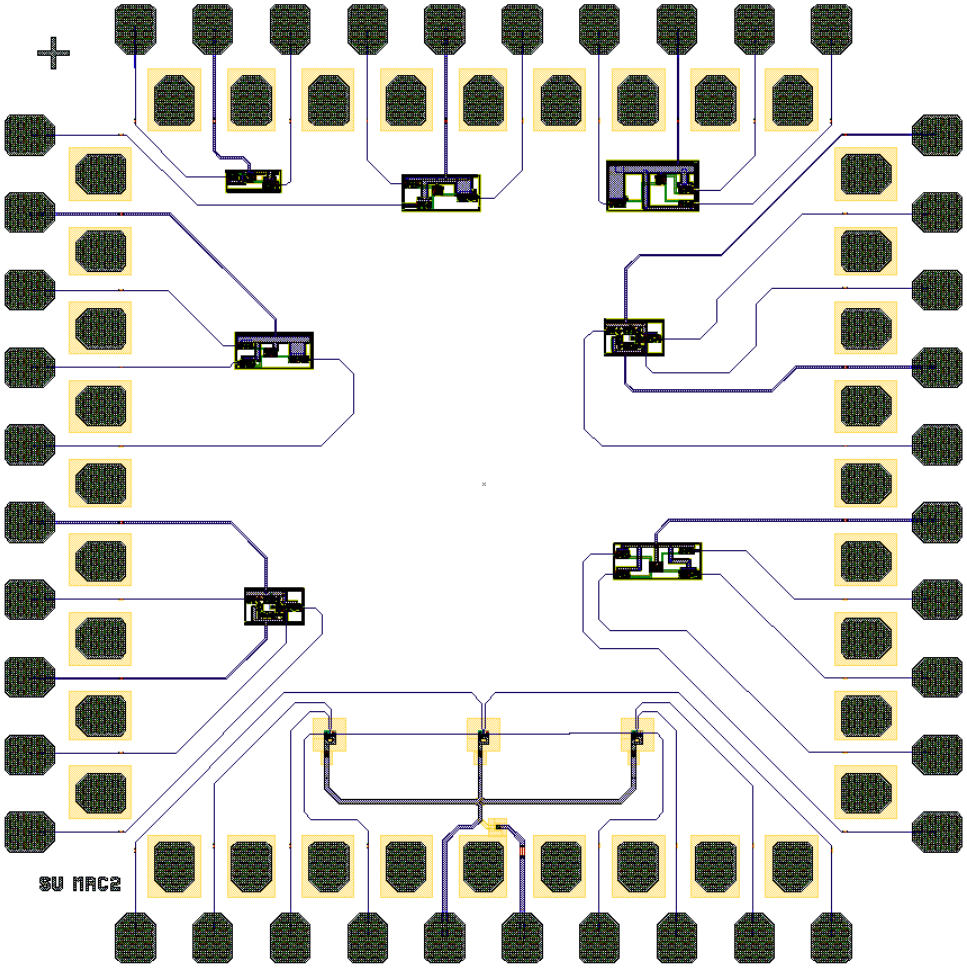


Figure 5.7: Chip SUMLL02-MRC layout for fabrication.

Table 5.2: Measured results for RSFQ experiments from SUMLL02-MRC.

	Expected bias margins	Measured bias margins
RSFQ01 chip 1	1.528 - 2.292 mA	2.21 - 2.47 mA
RSFQ01 chip 2	1.528 - 2.292 mA	2.31 - 2.53 mA
RSFQ02 chip 1	3.488 - 5.232 mA	N/A
RSFQ02 chip 2	3.488 - 5.232 mA	N/A
RSFQ03 chip 1	3.208 - 4.812 mA	N/A
RSFQ03 chip 2	3.208 - 4.812 mA	4.35 - 5.13 mA
RSFQ04 chip 1	3.504 - 5.256 mA	4.75 - 5.50 mA
RSFQ04 chip 2	3.504 - 5.256 mA	N/A
RSFQ05 chip 1	4.496 - 6.744 mA	5.56 - 6.90 mA
RSFQ05 chip 2	4.496 - 6.744 mA	N/A

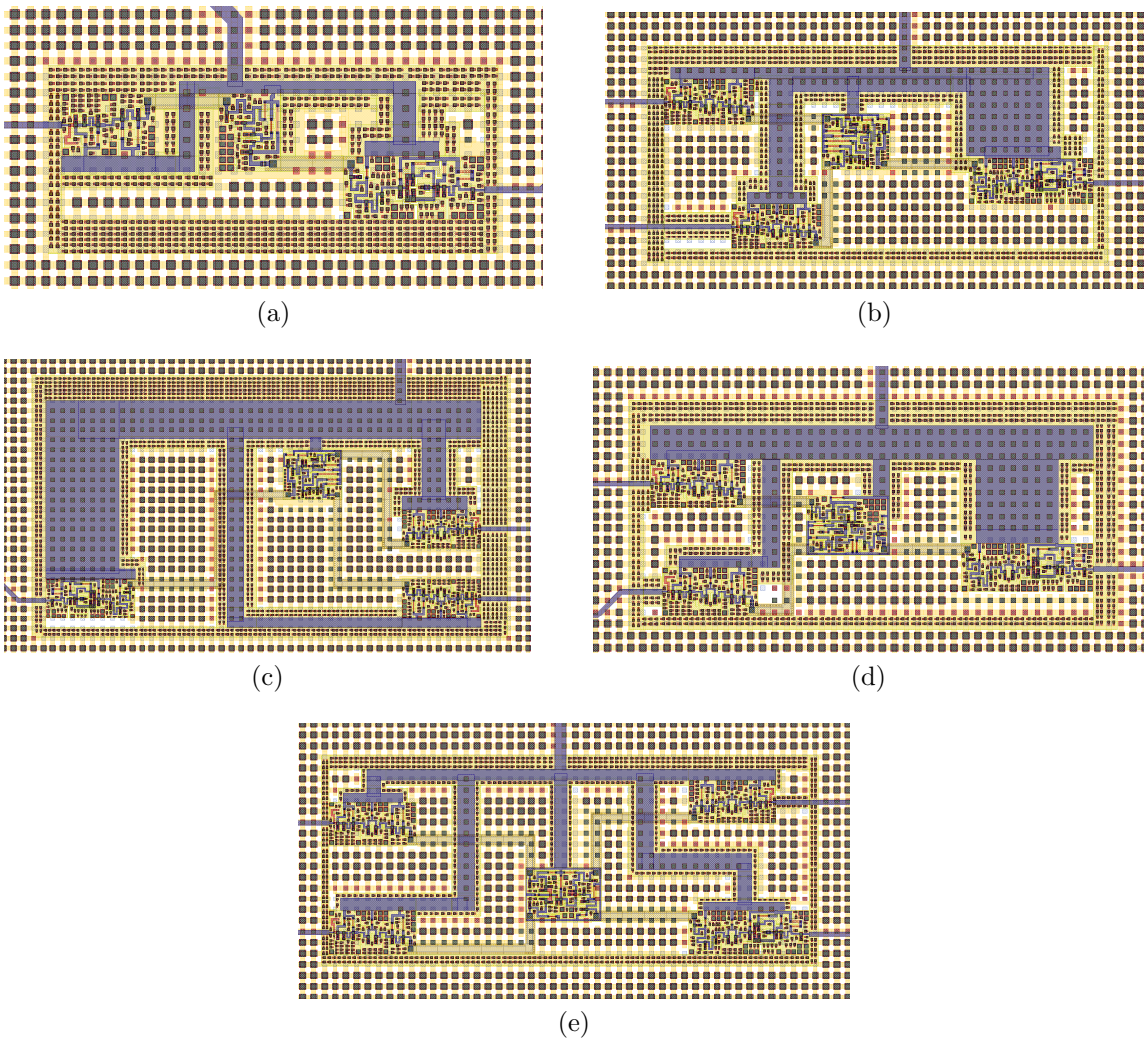
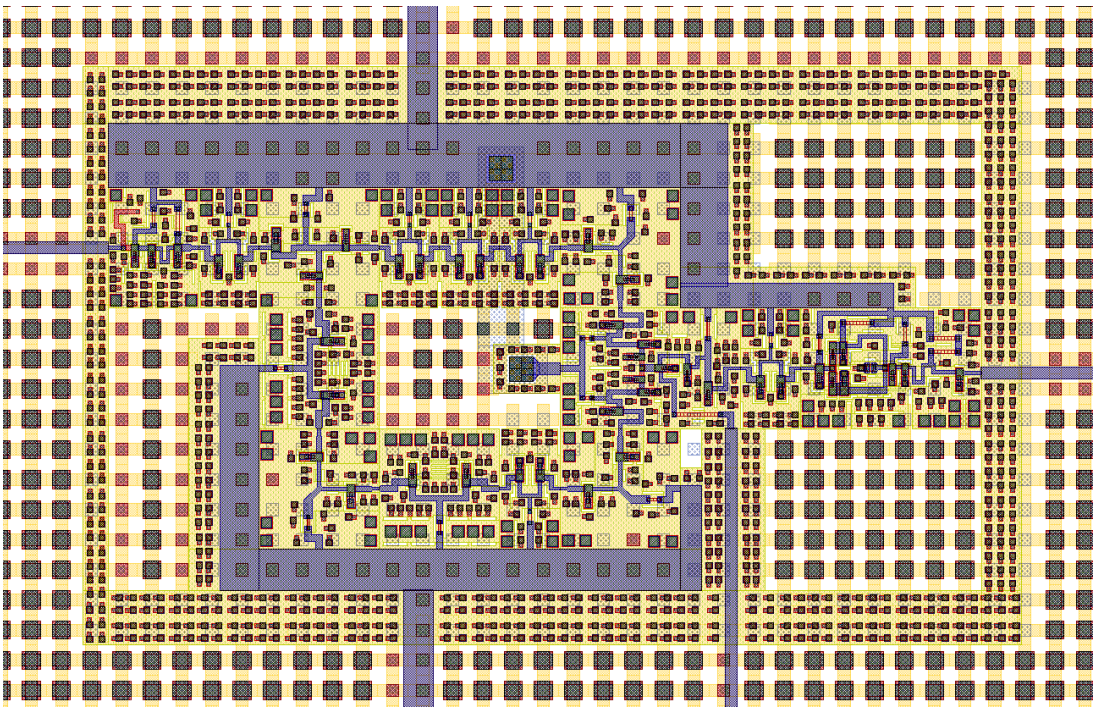
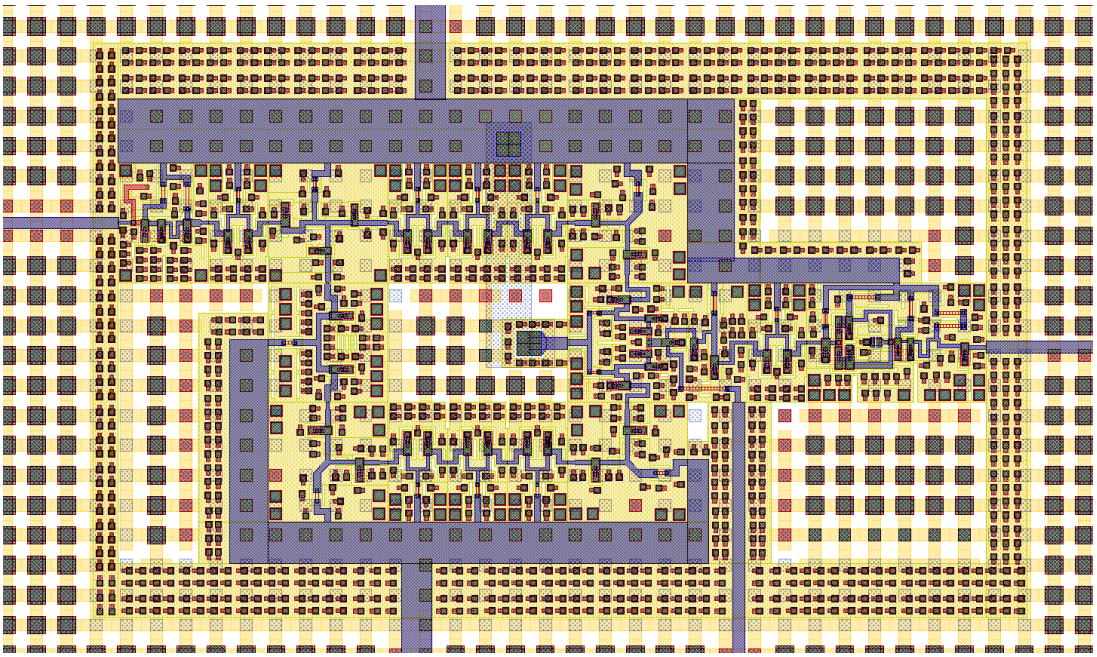


Figure 5.8: The GDS layouts for (a) RSFQ01, (b) RSFQ02, (c) RSFQ03, (d) RSFQ04 and (e) RSFQ05 experiments on SUMLL02-MRC.



(a)



(b)

Figure 5.9: The GDS layout for (a) TIMING01 and (b) TIMING02 experiments on SUMLL02-MRC.

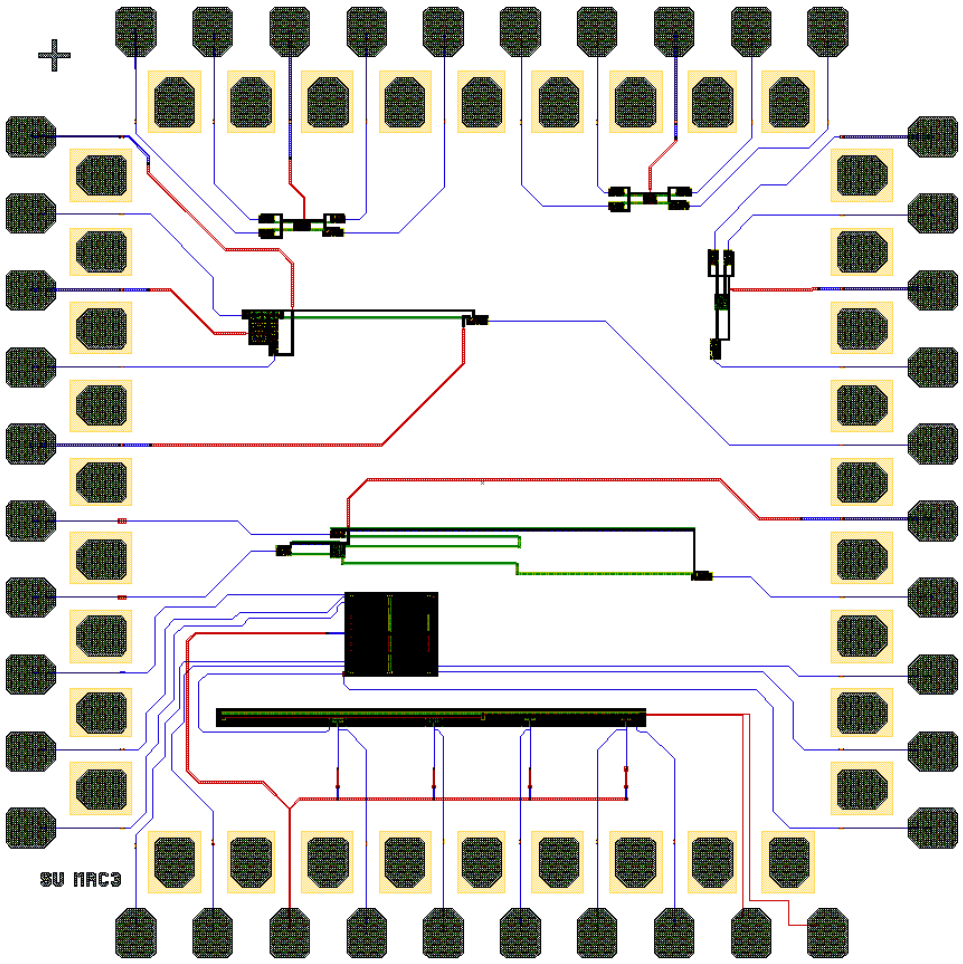
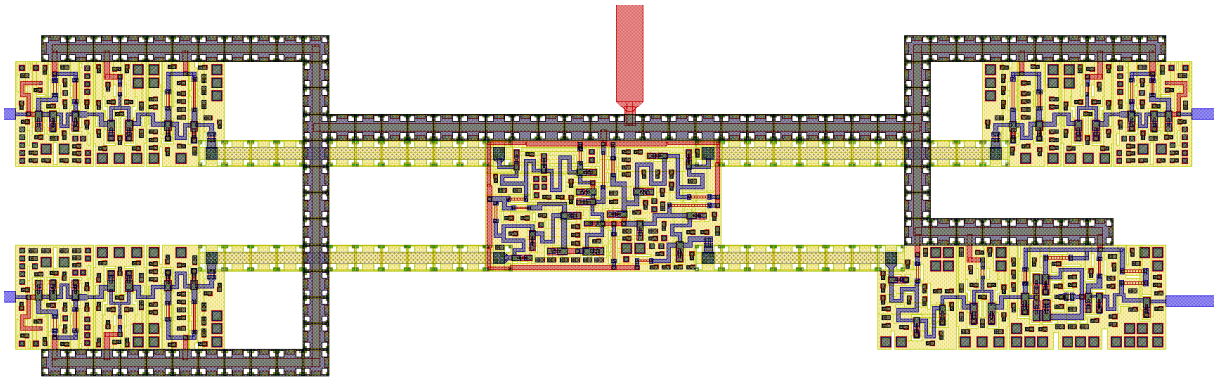


Figure 5.10: Chip SUMLL03 layout for fabrication.

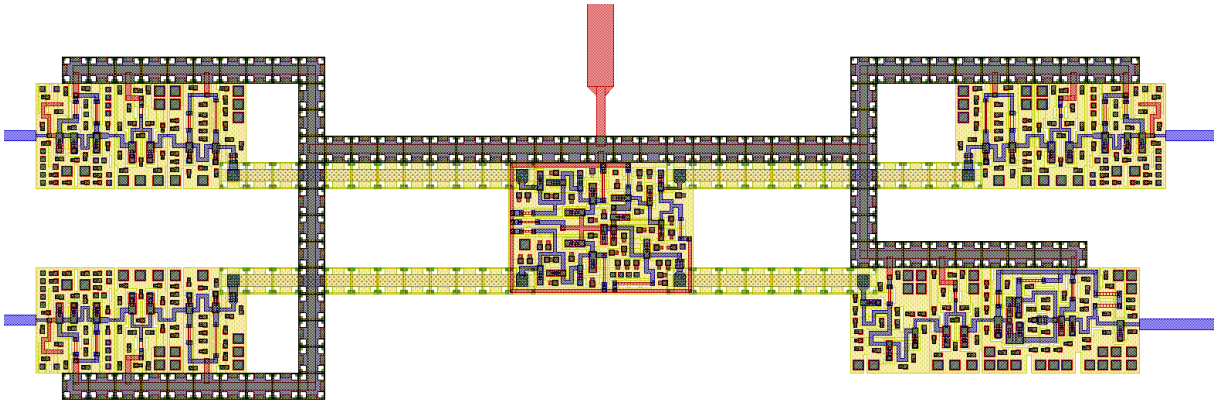
5.2.3 SUMLL03

The third chip, named SUMLL03, includes four experiments to validate the functionality of RSFQ cells designed for the ColdFlux project as well as a resonance experiment named RES01. The GDS layout for SUMLL03 is shown in Fig. 5.10. The fill structures for the chip are hidden to improve visibility of the test circuits. Two RSFQ experiments, RSFQ01 and RSFQ02, are set up to test the functionality of the NDROT and XORT cells respectively. Additionally, the RSFQ DFFT layout for the SUMLL03 chip has been updated to follow the layout track block presented in Chapter 4.2. The functionality of the updated DFFT cell for various PTL interconnect lengths are investigated. RSFQ03 is set up to test the DFFT with short straight PTLs and RSFQ04 tests the DFFT connected to long PTLs with corners. The GDS layouts for the individual RSFQ experiments are shown in Fig. 5.11. The fill structures are once again removed to improve visibility of the test circuits.

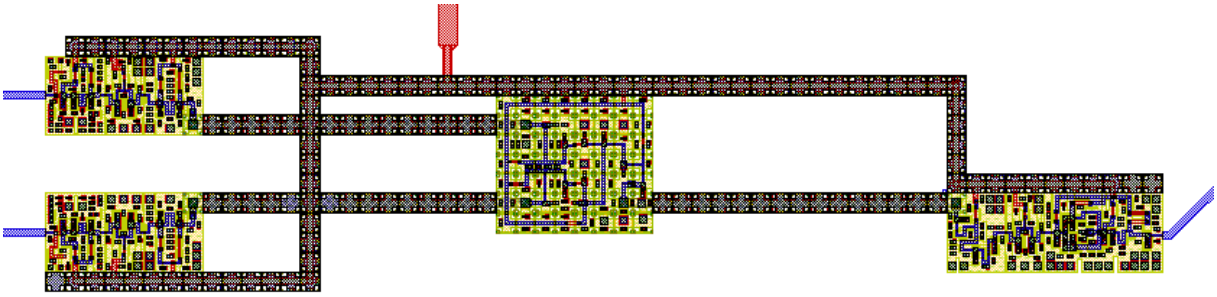
An additional experiment is set up to test the functionality and margins of the PTL transmitter and receiver cells when operating at the resonance frequency. This experiment is set up to verify the simulated results in Chapter 3 and [24]. A ring oscillator is constructed using JTLs with adjustable biasing to tune the output frequency of the oscillator in order to induce resonance on the PTL. The GDS layout for RES01 is shown in Fig. 5.12. The fill structures are omitted to improve visibility of the test structure.



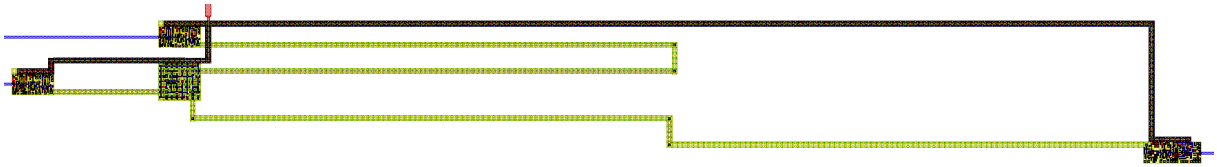
(a)



(b)



(c)



(d)

Figure 5.11: The GDS layouts for (a) RSFQ01, (b) RSFQ02, (c) RSFQ03 and (d) RSFQ04 experiments on SUMLL03.

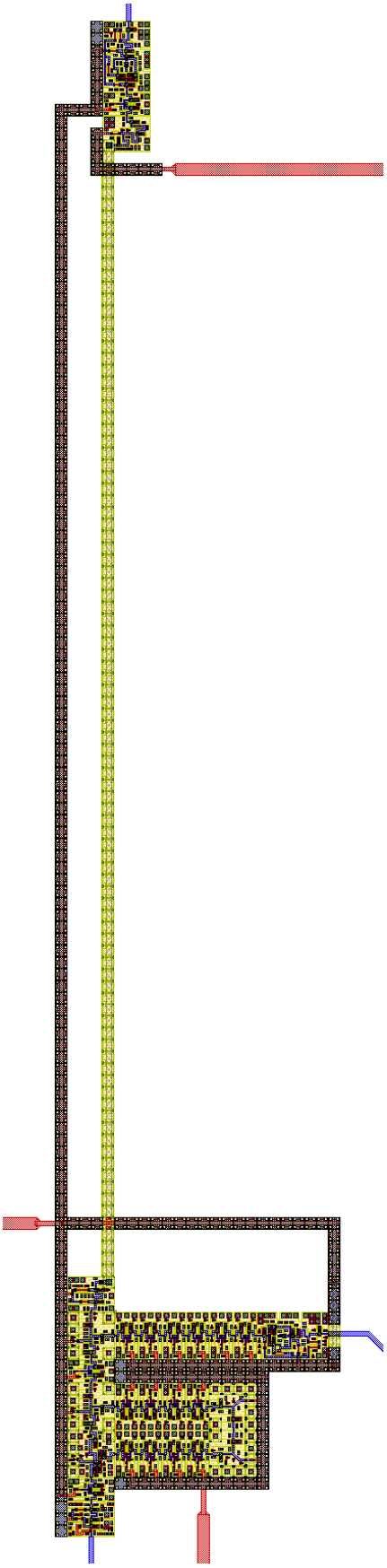


Figure 5.12: The GDS layout for RES01 on SUMLL03.

5.3 Conclusion

Three chip designs along with testing and measurement requirements were presented within this chapter. Multiple experiments to test various aspects of the RSFQ cell library developed for the ColdFlux project were designed. Test manuals for all three chip designs were also included in separate appendices. The three designs were submitted for fabrication by MIT-LL through the IARPA SuperTools program. The 2020 global pandemic caused significant delays to the fabrication and testing of the submitted designs. Preliminary measurements for two chip designs were included and discussed. The aim is to publish the measured results from NIST once they have been received.

Chapter 6

Conclusion

This dissertation presented an investigation of how conventional circuit analysis, such as KCL and KVL, can be adapted to construct phase-based equations representing the current distribution within RSFQ cells. These phase-based equations aided in the development of a formalised methodology to design and analyse various RSFQ cell designs. It was shown how these equations could be adapted to improve the operating margins of RSFQ cells, without the need of computationally expensive optimisation algorithms. Chapter 2 presented the design methodology for basic RSFQ cells up to physical cell layout. This included the calculation of cell operating margins, the analogue simulation, analysing the yield, and extracting the throughput delays and digital models using TimEx.

Chapter 3 presented a published paper which focused on the improvement of impedance matching of RSFQ cells to PTLs. Various methods to minimise SFQ pulse reflections were discussed. PTL transmitter and receiver cells were designed to improve impedance mismatching of PTLs for the MIT-LL SFQ5ee process.

The formalised RSFQ design theory from Chapter 2 and the research results from Chapter 3 were utilised to develop a portable RSFQ cell library for the IARPA SuperTools program. The standardisation of RSFQ cell layouts for multilayer fabrication processes was also discussed.

A variety of RSFQ test circuits were designed to evaluate the functionality of the RSFQ cell library developed for the SuperTools program. The tests included magnetic robustness of the cells, as well as circuits to measure the throughput delays of RSFQ cells. The challenges of testing RSFQ circuits and methods to measure meaningful results were discussed. Preliminary measured results for two fabricated chips were presented. The 2020 COVID-19 pandemic lead to considerable delays in chip fabrication, packaging and testing. Future work includes reporting on, and publishing, the official measured results once available.

The research presented an education quality design methodology for RSFQ cells. Through this work, the opportunity is presented to expand the education of circuit designers for RSFQ logic.

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Appendix A

Journal paper - Cell Design Methodology and Circuit Theory of RSFQ Logic

- L. Schindler and C. J. Fourie, "Cell Design Methodology and Circuit Theory of RSFQ Logic," Submitted for publication, 2020.

The formalisation of RSFQ cell design and circuit theory is presented within this paper. The majority of contributions to this article are my own. If the article is accepted for publication, the copyright will be transferred to Superconductor Science and Technology.

Cell Design Methodology and Circuit Theory of RSFQ Logic

Lieze Schindler and Coenrad J. Fourie, *Senior Member, IEEE*

***Abstract*—In contrast to transistor-based semiconductor circuits, there is currently no widely accepted formalized circuit theory or design methodology for superconductor RSFQ logic circuits. Even though experienced designers intuitively consider flux loops, nodal phase and branch currents when making design choices, the lack of a formalized design process makes it difficult for inexperienced RSFQ circuit designers to construct a functioning logic cell without a reference. This results in new circuit designers mostly recycling templates from published circuit designs. An iterative process is then followed where cell parameter values are adjusted, and the cell is run through electronic simulation engines until the desired functionality is reached. We propose the development of circuit design theory for RSFQ logic from first principles using phase-based circuit analysis. The circuit is designed using DC analysis to establish the DC operating point of the circuit. Phase-based analysis and simulation are then used to verify the dynamic circuit functionality. To demonstrate this method, we present the design of several examples. We analyze the initial operating margins of these designs and discuss design accuracy and efficiency.**

***Index Terms*—Circuit design, RSFQ, Superconducting integrated circuits**

I. Introduction

TRANSISTOR-BASED semiconductor circuits have widely accepted circuit theories and design methodologies. It is therefore still possible for inexperienced circuit designers to design semiconductor circuits which function as intended. The RSFQ logic family [1] currently has no widely accepted circuit theory or formalized design methodology for circuit design. The aim with this paper is to allow undergraduate students to design RSFQ circuits as easily as they can design simple transistor logic gates. To do this, the complexity and physics of RSFQ circuits should be reduced to a few engineering circuit equations.

We propose the development of circuit design theory for RSFQ logic from first principles using phase-based circuit analysis. The circuit is then designed using a DC analysis to establish a DC operating point that will result in a nominal circuit with good operating margins. Circuit simulation engines, such as JSIM [2], JoSIM [3] or WRSpice [4], are then used to verify the dynamic circuit functionality. We present two design examples – a Josephson transmission line (JTL) and a D flip-flop (DFF). This research forms part of the IARPA SuperTools program [5], [6] and aims to expand the knowledge of RSFQ logic cell design.

The research is based upon work supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120, and based on the research supported in part by the National Research Foundation of South Africa (Grant Number: 105859).

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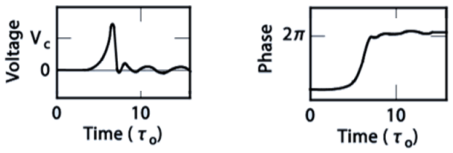

(a) (b)

Fig. 1. (a) SFQ pulse generated by junction with (b) associated 2π junction phase shift. Figure adapted from [1].

II. RSFQ Basics

Rapid Single-Flux Quantum (RSFQ) logic utilizes magnetic flux quanta passed between decision elements [1]. Associated current passes through inductive connections which results in short voltage pulses, as shown in Fig. 1a. These pulses are used for data representation. A Single-Flux Quantum (SFQ) pulse has an area equal to one flux quantum as evaluated through:

$$\begin{aligned}\text{Area of pulse} &= \int_{t1}^{t2} v(t)\mathrm{d}t \\ &= \int_{t1}^{t2} \frac{\Phi_0}{2\pi}\dot{\phi}(t)\mathrm{d}t = \frac{\Phi_0}{2\pi}[\phi_1 - \phi_2] \\ &= \Phi_0. \end{aligned} \tag{1}$$

In standard RSFQ logic, if an SFQ pulse is present during a clock period it represents a binary '1' and the lack of an SFQ pulse represents a binary '0'. When an SFQ pulse propagates through a Josephson junction (JJ), and results in instantaneous current in excess of the critical current I_C, the junction phase undergoes a 2π shift as shown in Fig. 1b. This is also referred to as the switching of a junction. For RSFQ logic, JJs are typically shunted with a resistor to be non-hysteretic, unless a fabrication process with self-shunted junctions is used.

RSFQ logic cells are constructed through three basic RSFQ building blocks shown in Fig. 2. Each block consists of inductor, JJ and bias current source elements. The transfer block transfers an SFQ pulse from one physical location to another. To achieve this, the value for the inductor is set as $L \sim \Phi_0/2I_c$ where I_c is the critical current of the JJ. The storage block stores an SFQ pulse within a junction-inductor loop. This is achieved by setting the inductor value as $L \sim \Phi_0/I_c$. The decision block is implemented through two JJs with different I_c values to control whether an SFQ pulse is transmitted or not. The typical relation between the critical currents of the two JJs is $I_{c2} = 1.4I_{c1}$ [1].

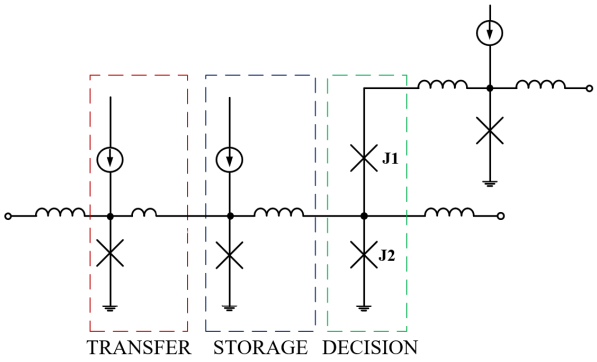

Fig. 2. Schematic of different RSFQ building blocks.

III. Phase-based RSFQ Circuit Design Methodology

A. Methodology

Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) are two commonly used circuit analysis methods taught to undergraduate engineering and physics students. These analysis methods are easy to understand and implement on basic circuits and powerful enough to find application in numerical circuit simulation tools. For this reason we develop a circuit analysis method for RSFQ circuits using KCL and KVL equivalents. As such, the circuit elements must be described in terms of the current flowing through the element or the voltage difference over the element. As discussed in Section II, the basic RSFQ circuit elements are JJs, inductors and current sources. Shunt resistors have no effect during DC analysis as current will always flow through a superconductor rather than a resistive material.

Once all the circuit elements are described in terms of the current through the element or the voltage across the element, KCL or KVL can be used to construct circuit equations. If the number of unknowns match the number of circuit equations, Newton's Method can be used to solve the values of the unknowns, also known as the root. Multivariate Newton's Method is a mathematical algorithm used to iteratively approximate the root of a function set. An initial guess for the unknown values is required. The next guess for the root is then calculated through:

$$\mathbf{x_{n+1}} = \mathbf{x_n} - \mathbf{J}(\mathbf{x_n})^{-1}\mathbf{f}(\mathbf{x_n}), \tag{2}$$

where $\mathbf{x_n}$ is the initial or previous guess, $\mathbf{f}(\mathbf{x_n})$ is the function set, $\mathbf{J}(\mathbf{x_n})$ is the pseudo-inverse Jacobian of $\mathbf{f}(\mathbf{x_n})$ and n is the number of iterations completed. The restrictions and special cases of Newton's Method are widely available in literature. For the purpose of this article, a script implementing Newton's Method was developed by assuming that a non-singular and non-zero $\mathbf{J}(\mathbf{x_n})$ can be constructed through the circuit equations.

B. Phase-based Josephson junction model

Various models have been developed to model the Josephson junction (JJ). A popular model is the RCSJ model [7] which models the JJ as an inductor in parallel with a capacitor and resistor. The RCSJ model is sufficient for modeling critically damped superconductor-insulator-superconductor (SIS) tunnel junctions used in various fabrication processes. The current through a Josephson junction is described through [8]:

$$i = I_c \sin\varphi + \frac{v}{R} + C\frac{dv}{dt}, \tag{3}$$

where I_c is the critical current of the junction, φ is the phase difference over the junction and R and C the internal junction resistance and capacitance, respectively. The Josephson phase-voltage relation is defined through [1]:

$$v = \left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt}. \tag{4}$$

We can combine (3) and (4) to describe the current through a JJ in terms of the phase:

$$i = I_c \sin\varphi + \left(\frac{1}{R}\right)\left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt} + C\left(\frac{\Phi_0}{2\pi}\right)\frac{d^2\varphi}{dt^2}. \tag{5}$$

For DC analysis, $d\varphi/dt = 0$ can be assumed. Therefore (5) can be reduced to represent the DC current through a JJ in terms of phase as:

$$i = I_c \sin\varphi. \tag{6}$$

The statement that the influence of the JJ's shunt resistor is negligible during DC analysis, is also verified through (6).

C. Phase-based inductor model

Considering the RCSJ model, the phase-voltage relation over an inductor for DC analysis can be characterized through (4). The voltage over an inductor is:

$$v = L\frac{di}{dt}. \tag{7}$$

Combining (4) and (7), a relation between phase difference over an inductor and current through an inductor can be established:

$$\left(\frac{\Phi_0}{2\pi}\right)\frac{d\varphi}{dt} = L\frac{di}{dt}. \tag{8}$$

Thus the current through an inductor in terms of phase, shown in Fig. 3, is derived as:

$$i = \varphi\left(\frac{\Phi_0}{2\pi L}\right), \tag{9}$$

where $\varphi = \varphi_1 - \varphi_2$. If $\varphi_1 \neq \varphi_2$, then current will flow through the inductor and no current will flow through the inductor if $\varphi_1 = \varphi_2$.

A summary of the phase-based component models are presented in Table I.

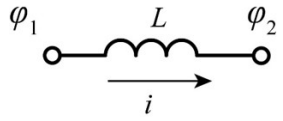

Fig. 3. Current through inductor in terms of phase difference over inductor.

TABLE I
SUMMARY OF PHASE-BASED COMPONENT MODELS

Component	Phase-based model
Josephson junction	$\varphi = \arcsin(i/I_c)$
Inductor	$\varphi = iL\,(2\pi/\Phi_0)$

IV. RSFQ Circuit Design Examples

A. JTL Circuit Design Example

The Josephson transmission line (JTL) is used for transmitting and reconstructing SFQ pulses. Although the most basic JTL has one Josephson junction, most RSFQ JTLs are symmetrical and use two transfer blocks as shown in Fig. 4. The JTL provides a basic example of how to analyze a circuit using phase-based circuit analysis. We include parasitic inductance of the connections to ground for completeness. Firstly, a DC analysis is done to determine how the current from the bias current source is distributed within the circuit. For this analysis, the following assumptions are made:

1) The phase at ϕ_1 equals the phase at ϕ_2 so that no current flows through L_1.
2) The phase at ϕ_5 equals the phase at ϕ_7 so that no current flows through L_4.

Considering these assumptions, we choose $I_{c1} = I_{c2} = 250\ \mu$A as a base design value for the RSFQ JTL circuit. The inductor design for a transfer block is $L \sim \Phi_0/2I_c$. Therefore $L \approx 4$ pH and $L_1 = L_2 = L_3 = L_4 = 0.5L$, as each inductor forms half of the inductor within a transfer block. The JJs are designed to be biased at $0.7I_c$, therefore I_{B1} is selected as 350 μA.

To derive the phase-based circuit equations, we consider the phase at φ_4:

$$\varphi_4 = \left(\frac{2\pi}{\Phi_0}\right) L_2 i_1 + \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right) L_{p1} i_1 \quad (10)$$

and

$$\varphi_4 = \left(\frac{2\pi}{\Phi_0}\right) L_3 i_2 + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right) L_{p2} i_2 \quad (11)$$

Evaluating Kirchhoff's current law (KCL) at φ_4 gives:

$$I_{B1} = i_1 + i_2 \quad (12)$$

Combining (10) and (11) and rearranging (12), we derive two functions with two unknowns:

$$\mathbf{f}(i_1, i_2) = \left(\frac{2\pi(L_2 + L_{p1})}{\Phi_0}\right) i_1 + \arcsin\left(\frac{i_1}{I_{c1}}\right) - \left(\frac{2\pi(L_3 + L_{p2})}{\Phi_0}\right) i_2 - \arcsin\left(\frac{i_2}{I_{c2}}\right) \quad (13)$$

and

$$\mathbf{g}(i_1, i_2) = I_{B1} - i_1 - i_2 \quad (14)$$

Newton's Method is then implemented to solve the two unknown currents. Newton's Method requires an initial guess for all unknown values. To avoid a complex arcsin function, the initial guess for the current flowing through a JJ must not be larger than the JJs critical current. The initial guess of $i_1 = i_2 = 0\ \mu$A is chosen and implementing Newton's Method, the unknown values converge to $i_1 = i_2 = 175\ \mu$A . Table II shows the comparison between the calculated values of the current distribution using Newton's Method and the simulated values.

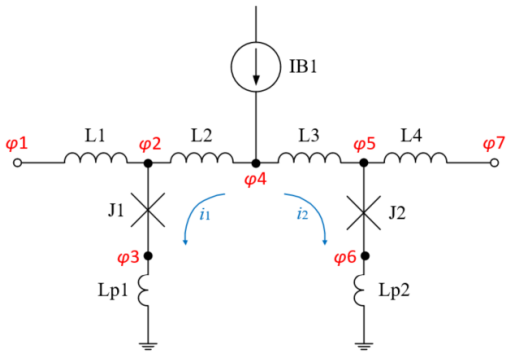

Fig. 4. Schematic of simplified JTL circuit.

TABLE II
COMPARISON BETWEEN CALCULATED AND SIMULATED VALUES FOR THE RSFQ JTL CIRCUIT.

	Calculated	Simulated
i_1	175.00 μA	175.00 μA
i_2	175.00 μA	175.00 μA
φ_2	0.8817 rad	0.8817 rad
φ_3	0.1063 rad	0.1063 rad
φ_4	1.9452 rad	1.9452 rad

We now consider the effect of connecting the JTL to other circuits by connecting another JTL as shown in Fig. 5. If $\varphi_5 = \varphi_8$, no current will flow through L_4 and L_5 leading to $i_3 = 0$. This is referred to as load balancing. But if $\varphi_5 \neq \varphi_8$, then i_3 will flow through L_4 and L_5. If $i_3 \neq 0$, then current leakage occurs between the circuits and the designed bias current distribution is distorted. This can affect the operation margins of the circuit and, in extreme cases, cause the circuit to malfunction. Fig. 6 is used to illustrate how current leakage can influence the operation margins of a circuit. The circuit in Fig. 5 is placed within a test circuit and simulated. The operation margins when $\varphi_5 = \varphi_8$ are shown in Fig. 6a. The bias current source I_{B2} is now reduced to 300 μA, so that $\varphi_5 \neq \varphi_8$ and the resulting operation margins are shown in Fig. 6b. It is seen that the current leakage caused by the

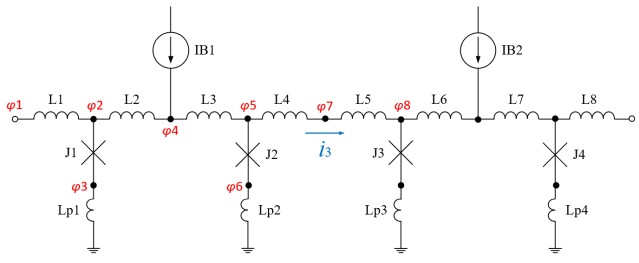

Fig. 5. Two JTLs connected together to illustrate current leakage.

```
B1 : 90.0 [   ###################|###########          ] 54.8
B2 : 89.6 [   ###################|###########          ] 54.9
IB1: 53.5 [           ###########|#################    ] 74.4
L1 : 90.0 [   ###################|###################  ] 90.0
L2 : 90.0 [   ###################|###################  ] 90.0
L3 : 90.0 [   ###################|###################  ] 90.0
L4 : 90.0 [   ###################|###################  ] 90.0
Critical margin: 53.5 % ['IB1-']
```

(a)

```
B1 : 90.0 [   ###################|#########            ] 46.3
B2 : 90.0 [   ###################|#########            ] 46.0
IB1: 43.0 [               #########|#################    ] 80.2
L1 : 90.0 [   ###################|###################  ] 90.0
L2 : 90.0 [   ###################|###################  ] 90.0
L3 : 90.0 [   ###################|###################  ] 90.0
L4 : 90.0 [   ###################|###################  ] 90.0
Critical margin: 43.0 % ['IB1-']
```

(b)

Fig. 6. Operation margins of the designed JTL when (a) two identical JTLs are connected and (b) when two JTLs with identical JJs, but different biasing currents are connected.

reduced bias current at I_{B2} has a significant effect on the operation margins. The critical margin at I_{B1} decreases from 53.5% to 43.0%.

B. DFF Circuit Design Example

The D flip-flop (DFF) is a multi-state device used to transmit an input set pulse synchronized with a reset (typically clock) signal. A basic DFF can be designed with three or four junctions [1]. Here, we design a more rugged DFF with seven junctions, shown in Fig. 7, that includes matching JJs, in the form of half-JTL stages at every input and output, as well as parasitic inductances to ground. The DFF has two states – a 'set' state where an input set signal has been received and a 'reset' state where a input reset signal has been received. The 'reset' state can also refer to the 'start-up' state of the DFF before any input signal has been received. The Mealy Finite State Machine diagram, extracted through TimEx [9], is shown in Fig. 8. The 'set' state is shown as state 1 and the 'reset' state is shown as state 0.

The RSFQ DFF circuit consists of transfer blocks, a storage block at $J_3 - L_3$ and a decision pair at $J_4 - J_5$. The J_2 junction also forms a decision pair with J_3 to act as a buffer junction if more than one input pulse is received before a reset signal. The same design procedure as the JTL example is followed – design the circuit in isolation at the DC operation point, simulate and analyze the functionality and calculate the operation margins.

For the DFF design, we choose $I_c = 250\ \mu$A and $I_{c1} = I_{c3} = I_{c4} = I_{c6} = I_{c7} = I_c$. We set $I_{c2} = I_{c5} = 0.71I_c$ for the decision pair blocks [1]. The inductor design for a transfer block is $L \sim \Phi_0/2I_c$. Therefore $L \approx 4$ pH and $L_1 = L_5 = L_7 = 0.5L$ as each inductor forms half of the inductor within a transfer block. The inductor design for a storage block is $L \sim \Phi_0/I_c$, therefore the storage inductor is set as $L_3 = 8$ pH. The values for the designed inductors are $L_1 = L_5 = L_7 = 2$ pH, $L_2 = L_4 = L_6 = 4$ pH and $L_3 = 8$ pH. The bias current sources are selected as $I_{B1} = I_{B3} = I_{B4} = 0.7I_c = 175\ \mu$A and $I_{B2} = I_c = 250\ \mu$A [1].

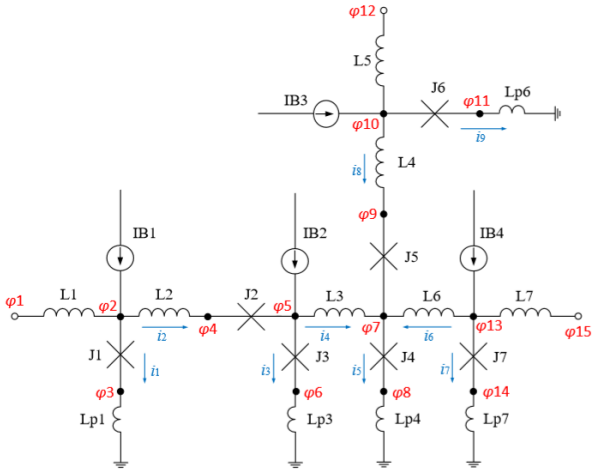

Fig. 7. Schematic of simplified DFF circuit.

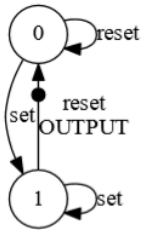

Fig. 8. Mealy Finite State Machine diagram of DFF.

1) Reset State: The 'reset' state indicates that an input reset signal was received by the DFF. Alternatively, it can also indicate that no input signals have been received and that the circuit is in a 'start-up' state. The DFF is analyzed using the phase-based component models established in Table I. The following assumptions are made to simplify circuit analysis:

1) The phase at ϕ_1 is equal to the phase at ϕ_2 so that no current flows through L_1.
2) The phase at ϕ_{12} is equal to the phase at ϕ_{10} so that no current flows through L_5.
3) The phase at ϕ_{13} is equal to the phase at ϕ_{15} so that no current flows through L_7.

Applying these assumptions, the phase change within the circuit is used to analyze the current flow at φ_2, φ_5, φ_7, φ_{10} and φ_{13}. The equations for the current distribution of the four bias current sources completes the nine equations needed for the nine unknown currents i_1 to i_9. The DFF, operating within the reset state, can therefore be described through the following equations:

$$f(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p7}i_7 - L_{p6}i_9 + L_4 i_8 - L_6 i_6\right) + \arcsin\left(\frac{i_7}{I_{c7}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) \quad (15)$$

TABLE III
COMPARISON BETWEEN CALCULATED AND SIMULATED VALUES FOR CURRENT DISTRIBUTION FOR THE DFF CIRCUIT RESET STATE.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	184.90956259373	184.909562593551	9.68E-11 %
i_2	-9.90956259372989	-9.90956259355176	1.80E-09 %
i_3	209.437554802441	209.437554798925	1.68E-09 %
i_4	30.6528826038287	30.6528826075229	-1.21E-08 %
i_5	80.1991225272621	80.1991225337204	-8.05E-09 %
i_6	28.1295130170933	28.1295130191328	-7.25E-09 %
i_7	146.870486982907	146.870486980867	1.39E-09 %
i_8	21.4167269063401	21.4167269070646	-3.38E-09 %
i_9	153.58327309366	153.583273092935	4.72E-10 %

$$g(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p1}i_1 - L_2 i_2 - L_3 i_4 - L_{p4} i_5\right) + \arcsin\left(\frac{i_1}{I_{c1}}\right) - \arcsin\left(\frac{i_2}{I_{c2}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) \quad (16)$$

$$h(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p1}i_1 - L_2 i_2 - L_{p3} i_3\right) + \arcsin\left(\frac{i_1}{I_{c1}}\right) - \arcsin\left(\frac{i_2}{I_{c2}}\right) - \arcsin\left(\frac{i_3}{I_{c3}}\right) \quad (17)$$

$$k(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p3}i_3 - L_{p6} i_9 + L_4 i_8 - L_3 i_4\right) + \arcsin\left(\frac{i_3}{I_{c3}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) \quad (18)$$

$$l(\boldsymbol{i}) = I_{B1} - i_1 - i_2 \quad (19)$$

$$m(\boldsymbol{i}) = I_{B2} + i_2 - i_3 - i_4 \quad (20)$$

$$n(\boldsymbol{i}) = i_4 + i_6 + i_8 - i_5 \quad (21)$$

$$o(\boldsymbol{i}) = I_{B4} - i_6 - i_7 \quad (22)$$

$$p(\boldsymbol{i}) = I_{B3} - i_9 - i_8 \quad (23)$$

Newton's Method, described in (2), is used to iteratively solve the values of i_1 to i_9. Table III shows the comparison between the calculated and simulated values for the current distribution in the DFF circuit for the reset state. It is seen that the calculated values are nearly identical to the simulated values. The difference is negligible and stems from limits in numerical precision.

2) Set State: The 'set' state indicates that an input set signal has been received by the DFF. When a single input set signal is received, junctions J_1 and J_3 switch and a flux quantum is stored within the $J_3 - L_3 - J_4$ loop. If another input set signal is received before a input reset signal, junction J_2 switches. The following assumptions are made in order to adapt (15)-(23) to account for the phase shift within the DFF:

1) The state change from reset to set causes the phase at ϕ_2 and ϕ_5 to increase with 2π.
2) The phase at ϕ_1 equals the phase at ϕ_2, so that no current flows through inductor L_1.
3) The phases at ϕ_7, ϕ_{10}, ϕ_{12}, ϕ_{13} and ϕ_{15} remain unchanged from the reset state.

Considering these assumptions, it is found that (15), (17), (19)-(23) still holds true for the set state. The 2π phase shift at ϕ_2 and ϕ_5 in the set state influences (16) and (18) as follows:

$$g(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p1}i_1 - L_2 i_2 - L_3 i_4 - L_{p4} i_5\right) + \arcsin\left(\frac{i_1}{I_{c1}}\right) - \arcsin\left(\frac{i_2}{I_{c2}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + 2\pi \quad (24)$$

and

$$k(\boldsymbol{i}) = \frac{2\pi}{\Phi_0}\left(L_{p3}i_3 - L_{p6} i_9 + L_4 i_8 - L_3 i_4\right) + \arcsin\left(\frac{i_3}{I_{c3}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + 2\pi \quad (25)$$

Newton's Method is once again used to iteratively solve the values of i_1 to i_9 for the set state through (15), (17) and (19)-(25). The set state of the DFF is simulated through a phase source in JoSIM [10]. The phase source makes it possible to simulate the 2π phase shift at ϕ_1 without an external test circuit. Table IV shows the comparison between the simulated and calculated current distribution values. It is seen that the calculation error is much larger for the set state than the reset state shown in Table III. This is mainly attributed to the assumptions that no current flows through L_1, L_5 and L_7. The DFF is designed for minimum current leakage during the reset state through load balancing. When the state of the DFF changes to the set state, the current distribution within the circuit changes and can affect the phases at the input and output ports. This can lead to current leakage which is not accounted for in the phase-based equations used to describe the current distribution within the DFF. As the possible current leakage is dependent on the source and load circuits, it is not viable to include these currents when establishing the phase-based equation calculations as simulation is required to determine the magnitude of current leakage.

V. CIRCUIT SIMULATION

The functionality of the designed circuits must be confirmed by simulating the circuits within a testbench. An example testbench evaluating all possible input combinations is shown

TABLE IV
COMPARISON BETWEEN CALCULATED AND SIMULATED VALUES FOR CURRENT DISTRIBUTION FOR THE DFF CIRCUIT SET STATE.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	148.038533649717	164.537414333393	-10.0274 %
i_2	26.9614663502826	31.2977713656466	-13.8550 %
i_3	52.9614538745911	56.687181599093	-6.57243 %
i_4	224.000012475692	224.610592980575	-0.27184 %
i_5	204.708390839295	205.063740664589	-0.17329 %
i_6	10.8939915710708	11.0378374552685	-1.30321 %
i_7	185.893991571071	186.037838618122	-0.07732 %
i_8	8.39763006532587	8.50901186224964	-1.30899 %
i_9	183.397630065326	183.509012836467	-0.06070 %

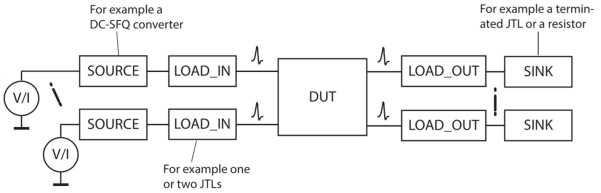

Fig. 9. Testbench for RSFQ circuits adapted from [9].

in Fig. 9. The DFF designed in Section IV-B is placed as the Device-Under-Test (DUT) and the JTL designed in Section IV-A is used as the load. The simulation results are shown in Fig. 10.

The simulated operation margins for the DFF are shown in Fig. 11. The critical margin is $+19.6\%$ and caused by J_4. The initial values for the bias current sources can now be adjusted to ensure that J_1, J_3, J_6 and J_7 are biased at $\approx 0.7I_c$. Adjusting the bias current sources also minimize the current leakage between the DFF and the connected JTL circuits. The adapted values for the bias current sources are $I_{B1} = 175$ μA, $I_{B2} = I_{B3} = 200$ μA and $I_{B4} = 215$ μA. The operation margins of the adapted DFF circuit is shown in Fig. 12. The critical margin is increased to $+23.3\%$ for J_4.

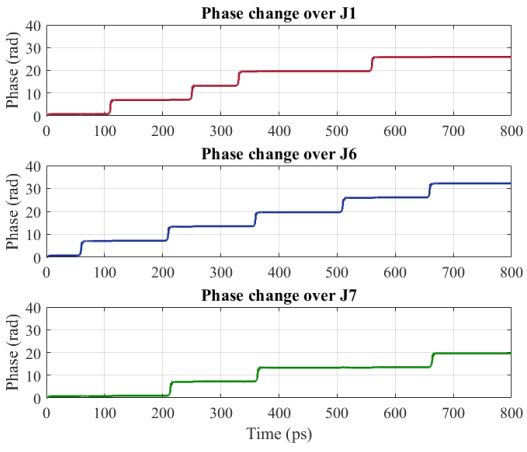

Fig. 10. Simulation of DFF circuit functionality showing the phase change of the junction closest to the set input port (top), reset input port (middle) and output port (bottom).

```
B1 : 63.5 [         ############|##########           ] 48.1
B2 : 57.4 [          ############|#####               ] 25.6
B3 : 35.2 [              #######|#########           ] 42.8
B4 : 49.8 [            #########|####                ] 19.6
B5 : 59.3 [          ############|#####               ] 23.1
B6 : 24.2 [                #####|#####               ] 26.6
B7 : 69.0 [       ###############|########          ] 39.1
IB1: 70.2 [       ###############|##################  ] 89.7
IB2: 47.0 [           ##########|#######             ] 35.1
IB3: 34.4 [               #######|##################  ] 85.0
IB4: 57.4 [          ############|##################  ] 90.0
L1 : 90.0 [   ##################|##################  ] 90.0
L2 : 90.0 [   ##################|##########          ] 47.9
L3 : 46.8 [             #########|########          ] 44.0
L4 : 90.0 [   ##################|###############     ] 69.5
L5 : 85.2 [    #################|##########          ] 47.5
L6 : 68.8 [      ###############|##################  ] 90.0
L7 : 90.0 [   ##################|##################  ] 90.0
Critical margin: 19.6 % ['B4+']
```

Fig. 11. Operation margins of the designed DFF.

```
B1 : 70.8 [       ###############|##########          ] 46.5
B2 : 31.0 [              ######|#######              ] 32.3
B3 : 54.6 [          ############|#####               ] 25.2
B4 : 46.8 [            #########|#####               ] 23.3
B5 : 47.4 [            #########|#######             ] 33.8
B6 : 25.6 [                #####|######              ] 30.7
B7 : 52.3 [           ##########|############        ] 55.5
IB1: 69.2 [       ###############|##################  ] 90.0
IB2: 34.9 [              #######|##############      ] 68.1
IB3: 43.7 [            #########|############        ] 58.8
IB4: 66.0 [        #############|############        ] 61.3
L1 : 90.0 [   ##################|##################  ] 90.0
L2 : 90.0 [   ##################|############        ] 57.9
L3 : 45.3 [            #########|############        ] 59.9
L4 : 90.0 [   ##################|##################  ] 90.0
L5 : 90.0 [   ##################|###########         ] 54.4
L6 : 90.0 [   ##################|##################  ] 90.0
L7 : 90.0 [   ##################|##################  ] 90.0
Critical margin: 23.3 % ['B4+']
```

Fig. 12. Operation margins of the adapted DFF so that each JJ within a transfer block is biased at $\approx 0.7I_c$.

RSFQ circuits are generally optimized to adhere to a critical margin of $\pm 20\%$ to account for process variations during fabrication. The DFF circuit does meet this requirement, but it can also be sent to an optimization tool to further optimize the operation margins. Optimization tools can consider both the static and dynamic behavior of a circuit during the optimization process [11].

To analyze the effect of the matching JJs, we simulate the phase difference at φ_2, φ_5, φ_7, φ_{10} and φ_{13} according to the DFF circuit schematic in Fig. 7. Table V shows how the phase at each node changes when the state of the circuit changes. A phase change of roughly 100 % indicates that a nearby junction underwent a 2π phase shift. The phase at the input ports during operation can be assumed to have a maximum fluctuation of approximately 2.6 %. The maximum phase fluctuation at the output port is 3.25%. The comparison of nodal phase change between φ_2 and φ_5 is shown in Fig. 13. The same input sequence as Fig. 10 is used to analyze the change of nodal phase. It is seen that the phase difference at φ_2 is significantly smaller than the phase difference at φ_5 when the state of the DFF changes from state 1 to state 0.

VI. DESIGN EXCEPTIONS

Special cases exist where circuit design using Newton's Method is not possible. An example of this is the SFQDC circuit. This circuit converts an SFQ pulse at the input to a

TABLE V
COMPARISON OF CHANGE IN NODAL PHASE FOR THE DFF CIRCUIT

State change	Average nodal phase change (fraction of 2π)				
	φ_2	φ_5	φ_7	φ_{10}	φ_{13}
State 0 → State 0	0.0000	0.0000	0.0001	1.0000	0.0000
State 0 → State 1	0.9745	0.8706	0.1134	0.0257	0.0325
State 1 → State 1	0.9998	0.0003	0.0001	0.0001	0.0000
State 1 → State 0	0.0254	0.1294	0.8867	0.9745	0.9673

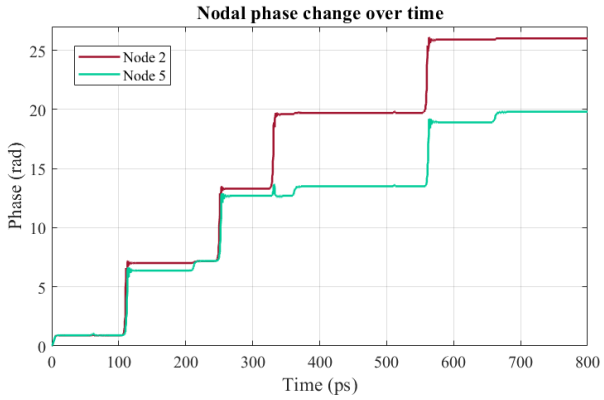

Fig. 13. Comparison of nodal phase change within the DFF circuit.

constant DC voltage at the output. This circuit is typically inserted at the output of a chip so that it is possible to measure the functionality of a chip without high-frequency measuring equipment. The SFQDC has certain JJs that constantly undergo a 2π phase shift, even during DC operation. There is therefore fluctuating current within the circuit loops due to the switching JJs. Due to the current fluctuation, Newton's Method will not converge.

VII. CONCLUSION

A phase-based circuit analysis technique was formalized for analysis and design of RSFQ logic circuits. Phase-based component models were established and two design examples, a two-junction single-state JTL and a seven-junction two-state DFF, were evaluated. We found that it is possible to accurately calculate the current distribution for a circuit at DC operation using the established phase-based circuit equations and Newton's Method. The effect of analyzing a circuit in isolation was discussed along with possible current leakage effects when the circuit is then connected to other circuits. The designed JTL and DFF circuits were simulated within a testbench circuit. It was found that adding matching JJs to the input and output ports of a circuit decreases phase fluctuation (and therefore current leakage fluctuation) when the circuit state changes. The short-comings and design exceptions for the developed RSFQ design method were also discussed. The formalized design method is shown deliver nominal circuit designs with good margins. It can be extended to other cells in the RSFQ logic family and can be used to provide a formalized teaching method for undergraduate and postgraduate circuit designers.

ACKNOWLEDGMENT

The authors would like to thank J. Delport for implementing phase mode analysis within JoSIM and P. Le Roux for discussions regarding design exceptions using Newton's Method.

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Appendix B

Journal paper - Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells

- L. Schindler, P. le Roux and C. J. Fourie, "Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells," IEEE Transactions on Applied Superconductivity, 2020. [24]

The majority of the contributions to this article are my own. The co-authors provided insight into the physics of SFQ pulse propagation on passive transmission lines. Copyright for this paper is held by IEEE Transactions on Applied Superconductivity.

Impedance Matching of Passive Transmission Line Receivers to Improve Reflections Between RSFQ Logic Cells

Lieze Schindler, *Student Member, IEEE*, Paul le Roux, *Student Member, IEEE*, and Coenrad J. Fourie, *Senior Member, IEEE*

***Abstract*—Devices used for rapid single flux quantum (RSFQ) cell interconnects include passive transmission lines (PTLs) and Josephson transmission lines. In this article, we demonstrate software analysis methods with which reflections on PTLs can be improved through impedance matching without compromising the margins of the connected RSFQ logic cells. RSFQ cells are typically designed to connect to PTL transmitters and receivers before attaching the PTL interconnects. These transmitters and receivers are used as matching and buffer stages between the cell and the PTL; and can be adjusted to minimize impedance mismatching. We integrate PTL transmitters and receivers within the RSFQ cell to decrease the amount of Josephson junctions required to incorporate PTL interconnect functionality. Frequency domain analysis on each cell provides equivalent impedance characteristics used for impedance matching.**

***Index Terms*—Circuit optimization, impedance matching, reflection coefficient, rapid single flux quantum (RSFQ), superconducting integrated circuits.**

I. Introduction

RAPID single flux quantum (RSFQ) logic utilizes magnetic flux quanta passed between decision elements—which results in short voltage pulses as associated current passes through inductive connections—for data representation [1]. The quantized area of the voltage pulse, a few picoseconds wide, corresponds to a single flux quantum (SFQ) $\Phi_0 \approx 2.07 \times 10^{-15}$ Vs. These short SFQ pulses allow for high-speed digital applications with low power consumption. RSFQ cells can be connected directly using a nonstoring inductive loop or, alternatively, the cells can be connected using Josephson transmission lines (JTLs) or passive transmission lines (PTLs) [2]–[4] to bridge longer distances. The choice of cell connection depends on various factors. These include the required power consumption, transmission delay restrictions, available routing space on the chip, and distance between the two cells to be connected. JTLs can transmit pulses without reflections, but drawbacks include increased power consumption and higher probability of timing errors with increased JTL length due to jitter [5]. A major drawback of PTLs is pulse reflection due to an impedance mismatch between RSFQ cells and the PTL [6]. This can cause timing jitter and affect the operating margins of a circuit [7], [8]. A notable advantage of superconducting PTLs is high-speed pulse propagation [9].

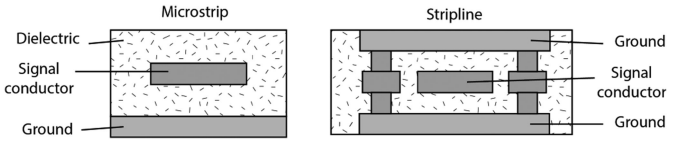

Fig. 1. Cross section of typical thin-film PTL geometries in superconductor integrated circuits for microstrip and stripline. The dielectric is mostly SiO_2, layer thickness is in the range of 100–500 nm, and line width is in the order of 5–10 μm.

Fig. 1 shows the typical structure of microstrip and stripline PTLs. In this work, we investigate a stripline PTL. Such a superconducting PTL, with a SiO_2 dielectric, typically has a phase velocity or pulse propagation speed of approximately 90–110 μm/ps at 4.2 K (about 0.3c), depending on the kinetic inductance contribution. For the MIT Lincoln Laboratory (MIT-LL) SFQ5ee fabrication process [10], a JTL with an approximate time delay of 5 ps can be laid out with a cell length of roughly 30 μm [11]. The JTL, therefore, has a pulse transmission of approximately 6 μm/ps. PTL interconnects, thus, allow signal transmission at more than an order of magnitude faster than JTLs [8].

In this article, we analyze methods for improving impedance mismatching focused toward application to the MIT-LL SFQ5ee fabrication process [10]. This research forms part of the ColdFlux project [12] under the intelligence advanced research projects activity (IARPA) SuperTools program [13]. For ColdFlux, placement-and-routing are developed that utilize PTLs for on-chip gate-to-gate interconnects [4], [14]. We, therefore, investigate how reflections induced by impedance mismatching between PTLs and transmitter/receiver cells can be improved, according to simulation, for the MIT-LL

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SFQ5ee fabrication process. We also analyze the influence of integrating the PTL transmitters and receivers within RSFQ cells and simulate these operating margins.

II. Impedance Matching, Noise, and Margin Optimization

A. Pulse Reflections

Pulse reflections are considered to be weak reflected waves, which do not possess enough energy to switch a Josephson junction (JJ) and are classified as weak noise [15]. These reflections are a result of impedance mismatch and can lead to a higher decision jitter [16]. If the circuit operates at its resonance frequency, the weak noise can accumulate on the PTL in such a way that it degrades the circuit's operating margins [6]. The resonance frequency is defined as

$$f_{\text{res}} \equiv \frac{1}{T_{rt}} \tag{1}$$

where T_{rt} is the round trip propagation time for a pulse through the PTL [15]. Optimal impedance matching for weak noise does not necessarily coincide with optimal impedance matching for SFQ pulse transmission. We shall focus on the theoretical impedance matching for weak noise and integrate the results into circuit improvement for SFQ pulse transmission.

B. Impedance Matching

Impedance matching should also consider the physical constraints of a PTL stemming from chip layout. The width of a PTL can be adjusted to match the input impedance of the receiving cell, but factors like chip space, minimum PTL width, and routing track pitch set firm constraints on this method of matching.

Impedance mismatch is often measured in terms of the reflection coefficient. The normalized reflection coefficient indicates the amount of pulse reflection on the PTL. Therefore, a small reflection coefficient indicates minimal impedance mismatch. The line's properties changes with frequency [17], and the reflection coefficient is, therefore, also dependent on frequency. At the operating temperature 4.2 K, and below the gap frequency, 750 GHz, the frequency-dependent effect can be ignored. The reflection coefficient can be approximated as

$$\Gamma = \left| \frac{X_{\text{in}} - (X_o + Z_0)}{X_{\text{in}} + (X_o + Z_0)} \right| \tag{2}$$

where X_{in} is the input impedance of the PTL receiver, X_o is the output impedance of the PTL transmitter, and Z_0 is the characteristic impedance of the PTL at dc conditions. These definitions are discussed in Section III through Figs. 3 and 4 and (9) and (10).

The method of adjusting the characteristics of the PTL transmitters and receivers to match the impedance of the PTL is extensively discussed in [6], [15], [16], [18], and [19]. We will follow a similar method, but will also investigate how this theory can be applied to integrate PTL transmitters and receivers within a RSFQ cell designed for the MIT-LL SFQ5ee fabrication process. Additionally, we analyze the characteristic impedance of a PTL designed for the MIT-LL SFQ5ee process and investigate how the margin optimization of the PTL transmitter and receiver circuits affect the SFQ pulse reflections on the PTL.

C. Margin Optimization

The maximum amount of power is transferred when the least amount of pulse reflection occurs. This point of maximum power transfer should, theoretically, correspond to the operation point with optimal margins under the condition that the pulse reflections are dissipated before the next pulse arrives. We optimize the circuit margins by maximizing the statistical distance between the point of operation and all known points of failure. The maximization is achieved by repeatedly performing a margin analysis and, given the new information, stochastically searching for a new best point until convergence is reached. Many methods are discussed in the literature [20]–[23] and any optimization method leading to optimal margins should lead to sufficient results.

D. Vias and Corners

In a placed and routed chip for very large scale integration, there are corners and vias along the length of a PTL in order to connect different cells. This is also used to implement PTL crossover. These corners and vias create impedance mismatch effects. These effects have to be investigated with a numerical model. The frequency dependence of the superconducting material properties and high-frequency reflection effects have to be taken into account in the numerical model. To our knowledge, this has not been done for superconductor integrated circuit thin-film PTLs and is outside the scope of this article.

If an equivalent model of the vias and corners can be simulated in simulation program with integrated circuit emphasis (SPICE), the netlist can be optimized with these effects included. The method of minimizing reflections using margin analysis presented here does not lose generality by not investigating the effects of corners and vias in our investigation.

III. Circuit Model Design

A. Josephson Junction

The JJ is a nonlinear device, which can be approximated through various models. These include the Resistively and Capacitively Shunted Junction (RCSJ), the nonlinear resistively shunted junction, the tunnel-junction-microscopic model, and variations of the above-mentioned models [24]. For our application, we chose the RCSJ model developed by [25] as the model is sufficient for critically damped superconductor-insulator-superconductor tunnel junctions such as those used in the MIT-LL SFQ5ee process.

Fig. 2 shows the RCSJ model, as described in [24]. The model describes a Josephson impedance, X_L, in parallel with the internal capacitance, C_J, and the normal resistance, R_N. The model is extended with an external shunt resistor, R_S, and parasitic inductance L_P. The circuit symbol used to represent our extended RCSJ model is also shown in Fig. 2. The ideal Josephson inductance describes the characteristics at low frequencies

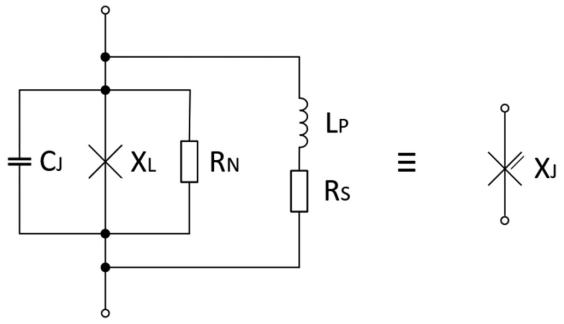

Fig. 2. RCSJ model with external shunt resistor, R_S, and parasitic inductance, L_P. The equivalent circuit symbol is shown on the right.

and is defined as

$$L_J = \frac{\Phi_0}{2\pi I_C \cos\phi} \tag{3}$$

where I_c is the JJ critical current and ϕ is the Josephson phase [24]. We assume a constant biasing current, $I_b = I_c \sin\phi$, is applied and that $\sin\phi < 1$. The equivalent Josephson impedance at low frequencies is therefore

$$X_L = j\omega L_J = \frac{j\omega\Phi_0}{2\pi I_C \cos\left(\arcsin\left(I_b/I_c\right)\right)}. \tag{4}$$

The equivalent impedance of the RCSJ model, X_J, in terms of frequency, ω, is described through the following equation:

$$X_J = \left(\frac{1}{j\omega C_J} \parallel X_L \parallel R_N\right) \parallel \left(j\omega L_P + R_S\right). \tag{5}$$

The model equation in (5) can be simplified under the following conditions [24, eq. (2.21)]:

$$R_S \ll R_N \text{ and } \omega L_p \ll R_S \tag{6}$$

where ω indicates the frequencies of interest, which, for our purposes, are well below the plasma frequency. We analyze at $f =$ 165 GHz (to replicate [19]) and $L_p \approx 1\text{pH}/\square$ if $R_S \approx 2\Omega/\square$. The MIT-LL SFQ5ee fabrication process leads to a relatively large parasitic inductances caused by the external shunt resistor. As a result, the conditions in (6) are not met for the MIT-LL SFQ5ee process. The simplified model, as used in [15], [16], [18], and [19], can, therefore, not be implemented in our case.

B. Passive Transmission Line

The width of a PTL influences the minimum track pitch of a circuit. A circuit utilizing a small track pitch can be laid out in a more compact format than a circuit with a larger track pitch. The assumption for a PTL with no loss and no dispersion can be made if the PTL length is 1–10 cm [26]. We assume that all on-chip PTL connections will not exceed twice the chip side length—which is comfortable below 10 cm. The PTL model is, therefore, based on the assumption of a lossless PTL with the characteristic impedance defined as

$$Z_0 = \sqrt{\frac{L_k + L_m}{C}} \tag{7}$$

where L_k is the kinetic inductance, L_m is the magnetic inductance, and C is the capacitance. As the width of the PTL is decreased, the capacitance decreases and the kinetic inductance increases. The change in magnetic inductance is neglectable for our purpose. Therefore, if the width of the PTL decreases, the characteristic impedance will increase.

The MIT-LL SFQ5ee fabrication process specifications were followed to design an example PTL layout with minimum width. Following this, a 4.5-μm superconducting stripline layout model was constructed. Using InductEx [27], along with the method discussed in [17], the characteristic impedance of the PTL was extracted as approximately 5 Ω. Similar theoretical results were calculated using the superconducting microstrip line characteristic impedance equation developed in [28].

The PTL cell connection is simulated in JoSIM [29] as a lossless transmission line with a characteristic impedance of 5 Ω. A transmission delay of 10 ps is selected (equivalent to a line length of about 1 mm). According to (1), the resonance frequency of the selected PTL will be

$$f_{\text{res}} = \frac{1}{T_{rt}} = \frac{1}{2 \cdot 10\text{ ps}} = 50\text{ GHz}. \tag{8}$$

We will, therefore, simulate a 50-GHz input pulse train connected to the PTL to analyze circuit behavior at the resonance frequency.

C. PTL Transmitter and Receiver

PTL transmitter circuits are used to transfer an SFQ pulse from an RSFQ circuit to a PTL and PTL receiver circuits reconstructs an SFQ pulse from the PTL to the RSFQ circuit. A JTL will act as a buffer as well as an SFQ pulse reconstruction device if it consists of two or more stages [18]. Fig. 3 shows how the PTL transmitter is designed as a two-stage JTL. The addition of a series resistor to either the transmitter or receiver circuit prevents flux trapping on the PTL along with providing improved impedance matching for weak noise [15], [30]. However, these series resistors also lead to unwanted attenuation of the SFQ pulse. The tradeoff between improved impedance matching for weak noise and improved SFQ pulse transmission implementing these series resistors was analyzed in [15]; it was found that the resistor value can be optimized according to the characteristic impedance of the relative PTL. This was done through analyzing the effect of the series resistor when operating at resonance frequency and tuning the value of the resistor until a sufficient relation between SFQ pulse transmission and degree of pulse reflection was achieved.

Following the results of [15], we implement a series resistor of 1.36 Ω in the transmitter circuit, illustrated in Fig. 3. Implementing frequency domain analysis for weak noise, we derive the equation for the output impedance in Fig. 3 as

$$X_o = \left(X_{J1} + j\omega L_2\right) \parallel X_{J2} + j\omega L_3 + R. \tag{9}$$

A design similar to the PTL transmitter is used for the PTL receiver circuit. Fig. 4 shows the PTL receiver designed as a three stage JTL. The input impedance for the receiver circuit is

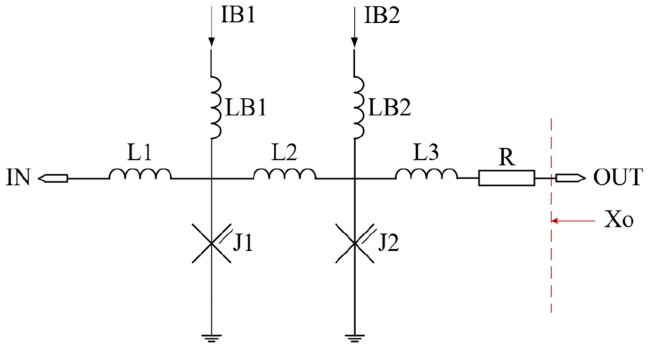

Fig. 3. Schematic of the designed PTL transmitter circuit. J1 = 200 μA, J2 = 162 μA, L1 = 2.5 pH, L2 = 3.3 pH, L3 = 2 pH, and R = 1.36 Ω.

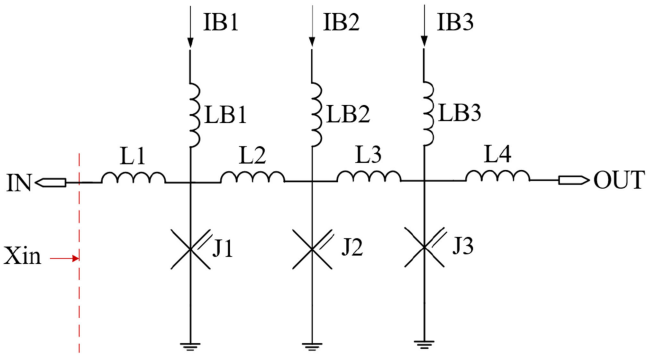

Fig. 4. Schematic of the designed PTL receiver circuit. J1 = J2 = 150 μA, J3 = 250 μA, L1 = 2 pH, L2 = 4 pH, L3 = 4.2 pH, and L4 = 2.8 pH.

calculated through

$$X_{\text{in}} = [(X_{J3} + j\omega L_3) \parallel X_{J2} + j\omega L_2] \parallel X_{J1} + j\omega L_1. \quad (10)$$

The physical layout of transmitter and receiver circuits can cause major area overhead. Circuits implementing PTL connections can consequently require more chip area than circuits with conventional JTL connections [8]. We, therefore, integrate PTL transmitters and receivers within individual logic cells, as proposed in [31], for the ColdFlux project. Matching JJs can be removed through this integration, allowing the circuit area to be minimized.

IV. Simulation Results

A. Simulation Setup

The MIT-LL process implements Nb/Al-AlOx/Nb JJs with a critical current density of 100 μA/μm^2 [10]. We set the McCumber parameter to $\beta_c \approx 1$ for all junctions to analyze a critically damped system. A lossless PTL with a characteristic impedance $Z_0 = 5\ \Omega$ is selected for simulation when a nominal critical current $I_{C\text{nominal}} = 250\ \mu$A is used. The biasing current is designed $I_b \approx 0.7 I_c$. This relation is known to produce minimal pulse reflections [6]. The parasitic inductances found within the physical cell layout is taken into consideration during the simulation.

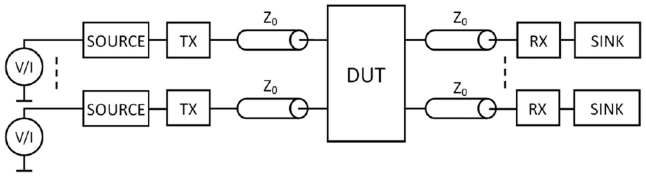

Fig. 5. Test circuit used for RSFQ circuit simulation. The DUT has integrated PTL transmitters and receivers.

The RSFQ cells were simulated in JoSIM [29] using the test circuit shown in Fig. 5. The source, typically a DCSFQ converter, is connected to a PTL transmitter (TX) followed by a PTL (Z_0) linked to the device-under-test (DUT). The PTL receiver is integrated within the DUT together with the corresponding PTL transmitter. The current through the sink is measured to ensure the output pulse generated by the DUT retains enough energy to propagate through a PTL and switch the PTL receiver (RX).

B. Test Cases

We use the delay flip-flop (DFF) as an example DUT for the circuit improvement process. We implement the results from (8) and drive the DUT with a pulse train at the resonant frequency, 50 GHz. The resonance frequency is used to analyze how the pulse reflections affect the circuit functionality when the worst case occurs [6].

We investigate three test cases where the DUT is connected as seen in Fig. 5.

1) The first test case is a benchmark test where no circuit parameter optimization is performed on the DUT.
2) The second test case optimizes all the circuit parameters of the DUT for optimal circuit margins, theoretically corresponding to optimal SFQ pulse transmission.
3) The third test case analyzes how the results from the second test case affects the pulse reflections on the PTL, and optimizes selected circuit parameters to maximize impedance matching for weak noise.

The test cases analyze the normalized reflection coefficient along with the margins of the global parameters at the resonant frequency. The global margins represent the respective fabrication tolerance for JJs, inductances, and biasing currents.

C. Reflection Coefficient

The theoretical reflection coefficient is calculated using (2). The output impedance of the PTL transmitter was calculated, using (9), as $X_o = 2.320 + j3.429\ \Omega$. The characteristic impedance of the PTL simulated as $Z_0 = 5\ \Omega$. The DUT was simulated and the normalized reflection coefficient for the simulation was compared to the calculated value. The simulated area of the pulse voltage was calculated in the center of the incoming PTL to determine the pulse reflection, normalized to the area of the input pulse. The resulting input impedance for the receiver, along with the calculated and simulated reflection coefficient for each test case is listed in Table I. The input impedance for the receiver was calculated using the ideal case, which attributes to

TABLE I
PARAMETER VALUES AND REFLECTION COEFFICIENT FOR RECEIVER CELL CONNECTED TO A 5-Ω PTL WITH DIFFERENT OPTIMIZATION METHODS

Optimization	Impedance (Ω)	Reflection Coefficient	
		Theoretical	Simulated
No optimization	1.621 + j3.410	0.3633	0.3597
Complete parameter	1.273 + j4.074	0.3089	0.3552
Selected parameter	1.191 + j5.125	0.2115	0.2395

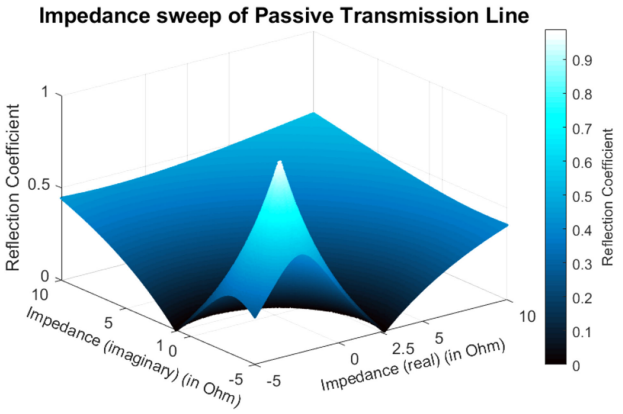

Fig. 6. Impedance sweep of a PTL investigating the reflection coefficient when connected to the designed RSFQ transmitter and receiver.

the difference between the calculated and simulated reflection coefficient in Table I.

We found that the complete margin optimization in the second test case did not drastically improve the simulated reflection coefficient. The receiver circuit in Fig. 4 is adapted for the third test case, according to results from [6], to adhere to the inductance relation where both L_2 and $L_3 \approx \Phi_0/2I_c$. This relation provides constraints to the value of the PTL receiver input impedance to improve overall impedance matching with the PTL. Parameter value constraints are, therefore, placed on L_2 and L_3 during the second margin optimization process to investigate the resulting effect on the reflection coefficient. The results for the selected parameter optimization are listed in Table I and it is seen that the simulated reflection coefficient was reduced from 0.3597 in the first test case to 0.2395 in the third test case. The simulated reflection coefficient decreased by approximately 33% from test case 1 to test case 3.

An impedance sweep of the PTL was done using MATLAB to determine the optimal operation point with a minimum reflection coefficient when the PTL is connected to the designed RSFQ PTL transmitter and receiver. The resulting graph is shown in Fig. 6. Negative impedances are shown on the graph, but are not viable implementation options. According to the impedance sweep, the optimal operation point for the PTL with minimum reflection will be at $Z_0 \approx 2.5\ \Omega$.

D. Global Parameters

We also analyze the improvement in global parameter margins for each test case. These global parameter margins indicate the fabrication tolerances for JJ values, inductance values and the biasing current of the circuit. A circuit with large operating margins for global parameter are more robust toward fabrication variations. The results are listed in Table II. It is seen that the margins are the most improved for the selected parameter optimization. We deduce that the constraints placed on L_2 and L_3 leads to a more stable parameter optimization than the complete parameter optimization due to a more constant input impedance of the PTL receiver.

TABLE II
GLOBAL PARAMETER MARGINS FOR A RECEIVER CELL CONNECTED TO A 5-Ω PTL

Optimization	Junctions		Inductance		Bias Current	
No optimization	-8.4	+16.2	-35.2	+51.3	-16.2	+12.0
Complete parameter	-15.5	+16.2	-50.6	+69.6	-21.8	+21.8
Selected parameter	-22.5	+15.5	-51.3	+75.9	-21.8	+26.7

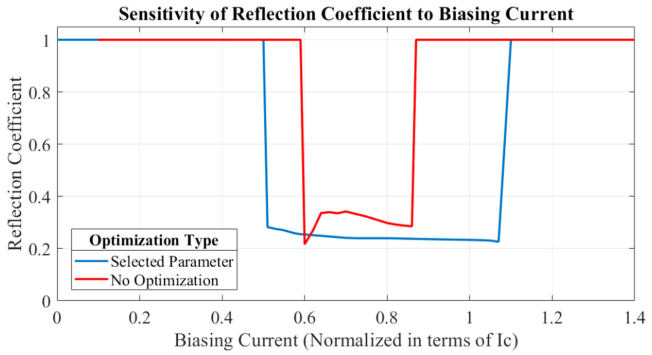

Fig. 7. Sensitivity of reflection coefficient to the biasing current for both the unoptimized and selected parameter optimized receiver circuits. The biasing current is normalized in terms of I_c. A reflection coefficient of 1 indicates a region of circuit malfunction.

E. Influence of Biasing Current

The first test case designed the integrated PTL receiver and transmitter for $I_b \approx 0.7I_c$. This relation is known to produce minimal pulse reflections [6]. This relation is investigated through analyzing the sensitivity of the reflection coefficient at different values of I_b (for the receiver circuit) after the selected parameter optimization. The reflection coefficient is measured after a few pulses to ensure that the effects of the resonant frequency are present. Fig. 7 shows the comparison of the reflection coefficient of the circuit before optimization and after selected parameter optimization. A reflection coefficient of 1 indicates a region of circuit malfunction.

The reflection coefficient of the circuit with no optimization is more sensitive to the changes in biasing current than the case of selected parameter optimization. The minimum reflection coefficient, for the case of no optimization, is 0.2165 and is found at $0.6I_c$, which is on the edge of circuit malfunction. We found that, for the case of the DFF receiver circuit after selected parameter optimization, the reflection coefficient decreases slightly as I_b increases while $0.5I_c < I_b < 1.1I_c$. We deduce that the receiver circuit functions correctly at higher biasing currents,

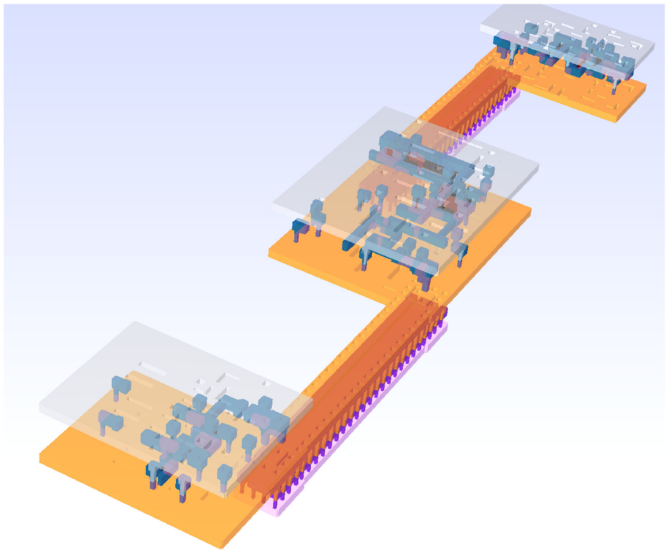

Fig. 8. Three-dimensional rendering of PTL test circuit to show the position of transmission lines below the ground plane in the MIT-LL SFQ5ee process. The vertical dimension has been stretched for clarity.

$1.0I_c \leq I_b < 1.1I_c$, due to current bleeding to the junctions within the DUT connected to the integrated PTL receiver circuit. The minimum reflection coefficient is 0.2262 and is found at $1.07I_c$, which is on the edge of circuit malfunction, similar to the case with no circuit parameter optimization.

V. Circuits

The PTL drivers and optimized receivers have now been implemented in the cells of the ColdFlux RSFQ cell library. A low-frequency test circuit was designed for fabrication in the MIT-LL SFQ5ee process [10], although the objective was to test magnetic rule checking models and tools as described elsewhere [32]. A 3-D rendering of the test circuit with InductEx is shown in Fig. 8. This test setup only verifies that the transmitter-PTL-receiver combination transmits SFQ pulses successfully, and cannot be used to measure reflection coefficients.

In future work, we will add high-frequency on-chip test structures to test the efficiency of the optimization.

VI. Conclusion

In this article, we investigated different methods to improve pulse reflections on PTLs. The PTL transmitter and receiver circuits were designed as JTLs to act as SFQ pulse reconstruction devices as well as a buffer between the stripline PTLs and connected cells for the MIT-LL SFQ5ee process. We investigated pulse reflections at resonance frequency and simulated the test circuit for the worst case scenario. The tradeoff between circuit improvement for weak noise and the optimization for SFQ pulse transmission was analyzed. We found that the inductances within the PTL receiver circuit has a large influence in the reduction of pulse reflections. Constraints were placed on selected inductors during the optimization process. We were able to improve simulated pulse reflections for the DFF by approximately 33%. It was found that the pulse reflections after selected parameter optimization were minimally influenced by the bias current of the receiver circuit when the cell is within the operating region. The optimized PTL receiver circuits now form part of every cell with integrated PTL receivers in our ColdFlux RSFQ cell library.

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Appendix C

Journal Paper - Design and Characterisation of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process

- C. J. Fourie, C. L. Ayala, L. Schindler, T. Tanaka and N. Yoshikawa, "Design and Characterization of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process," IEEE Transactions on Applied Superconductivity, 2020. [41]

In this paper we introduce a track routing architecture for RSFQ and AQFP layouts focused on the MIT-LL SFQ5ee fabrication process. The work was done as a collaboration between a team of researchers from Stellenbosch University and Yokohama National University in Yokohama, Japan. The copyright for this paper is held by IEEE Transactions on Applied Superconductivity.

Design and Characterization of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process

Coenrad Johann Fourie, *Senior Member, IEEE*, Christopher Lawrence Ayala, *Member, IEEE*, Lieze Schindler, *Student Member, IEEE*, Tomoyuki Tanaka, and Nobuyuki Yoshikawa, *Senior Member, IEEE*

***Abstract*—Place and route tools for synthesized superconductor logic circuits, either for dc-biased rapid single flux quantum (RSFQ) or ac-biased adiabatic quantum flux parametron (AQFP), are required to automate the design of complex logic circuits. For hand-crafted circuit layout, logic cells, clock, and bias distribution, and signal interconnect can be optimized for tight fit and the adherence to design rules. For complex systems with thousands of logic gates, a hand-crafted approach is not efficient and automated place and route tools are a necessity. Such tools require logic cell layout for placement with a minimum set of rules, followed by an interconnect design that allows maximum routability and strict adherence to layer fill requirements. In this article, we present the design and characterization of a routing architecture that allows rule-based automated place and route for both RSFQ and AQFP logic families. We show that a layout tile size of 10 $\times$ 10 μm can be designed to accommodate all design rules for layout fill densities, passive transmission line routing, bias current distribution, and the vias needed to stitch multiple ground planes and provide shielded signal and bias tracks. We also characterize the performance of the layout architecture in terms of transmission line parameters and bias current coupling with powerful simulation tools developed for the SuperTools project. The result is a track layout that doubles as chip fill, is now used for integrated circuit layout under SuperTools and is also applicable to any similar fabrication process with at least eight superconductor metal layers.**

***Index Terms*—Adiabatic quantum flux parametron (AQFP), interconnects, rapid single flux quantum (RFQ), routing, shielding.**

I. Introduction

THE Mead and Conway revolution during the late 1970s was a huge milestone in the semiconductor industry that paved the way for very large scale integration (VLSI) through the establishment of technology-agnostic design rules, systematic methodologies, and best practices [1]. Subsequently, these guidelines have been codified into electronic design automation (EDA) tools enabling the ubiquitous development of the CMOS circuitry that we use today. Progress in superconductor EDA (S-EDA) tools recently has led to the development of place and route methods with the goal of approaching VLSI-level superconductor electronics. Under the IARPA SuperTools program [2], as well as in preparation for it, such place and route tools for synthesized logic circuits have been developed [3], [4]. These tools cover both dc-biased rapid single flux quantum (RSFQ) logic circuits [5] and ac-biased adiabatic quantum flux parametron (AQFP) logic circuits [6]. For automated place and route, digital circuits require arbitrary length interconnects. We thus limit interconnect design to the passive transmission line (PTL) for ballistic pulse propagation [7]. The PTL has been studied thoroughly before [8] and the successful use of such PTL interconnects for large single flux quantum (SFQ) circuit layouts have been demonstrated many times [9]. Design and evaluation of vias between stripline PTLs have also been shown [10], [11], and it was experimentally verified that stripline PTLs below a main ground plane with properly matched via holes is good for SFQ pulse propagation up to 80Gb/s over distances of up to 10mm and with up to 30 via holes [11]. We thus design place and route tools and a PTL interconnect architecture within these confines.

A tiled layout structure applicable to automated place and route [12] of SFQ circuits in the National Institute of Advanced Industrial Science and Technology (AIST) advanced design process (ADP) process [13] has been designed [14]. This layout structure can be used for an entire chip layout. A fast routing method for SFQ circuits in this process has been developed previously [15].

Although a more advanced fabrication process [16] will ease the design constraints, the development schedule of SuperTools required a track architecture solution for the MIT Lincoln Laboratories SFQ5ee process, for which material thicknesses, critical dimensions, and electrical characteristics have been published [17]. A PTL design for this process has been presented recently [18]. It is used with a cell tile layout [19] that allows for RSFQ and energy-efficient rapid single flux quantum (ERSFQ) [20] cell interchange and provides a signal PTL track pitch of 20 μm (with bias lines interspersed with signal tracks) and two layers of PTL. This layout provides for long flux trapping moats at the cell edges. It is not compatible with our placement tools and libraries.

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An automated placement and routing methodology for asynchronous ERSFQ circuit design has also recently been proposed to include track design and PTL interconnects [21]. Although it presents a thorough solution for asynchronous circuit design, it is not compatible with our clocked RSFQ and AQFP libraries or the SuperTools tool chain.

For a row-based place and route strategy used with our ColdFlux [22] tools under SuperTools [23], we set out to design a routing track architecture composed of symmetrical blocks or tiles that provide an uninterrupted 10 μm track pitch for signal PTLs, with two layers of PTLs under circuit cells and up to four layers of PTLs over dedicated routing tracks. This route track architecture must fill the entire active area of a chip, so that it needs to satisfy the following requirements:

1) it must be possible to fit any transmission line through the track block;
2) all vias needed for ground plane stitching must fit in the track block;
3) all layer density restrictions must be adhered to both minimum and maximum layer fill;
4) all signal line to signal line vias must fit inside the track blocks;
5) track blocks must tile correctly, with no design rule check (DRC) violations, irrespective of the routing or via contents of neighboring blocks;
6) flux trapping moats must be incorporated in the track block;
7) bias lines must fit in the same track architecture.

For the design and characterization of the routing track architecture, we make extensive use of the S-EDA tools developed and verified under ColdFlux and packaged as part of InductEx.

Although the design presented here is for the MIT-LL SFQ5ee process, it can be adapted with minor changes to subsequent evolutions of the process. Taking cues from what Mead–Conway has done for the semiconductor industry, we ensured that much of the design philosophy and all of the analysis methods described here can be transferred to other multilayer superconductor fabrication processes as well with the intention of establishing the basic design guidelines for achieving functional large-scale integration of superconductor electronics.

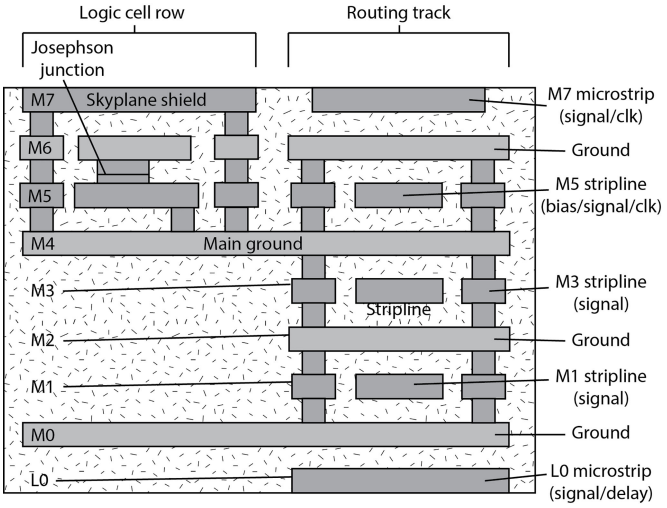

Fig. 1. Simplified illustration of a cross section of the ColdFlux layout stack in the MIT-LL SFQ5ee process showing the assignment of PTL layers.

II. Routing Architecture Design Constraints

A. Layer Stack

The MIT-LL SFQ5ee layer stack is described in detail in [16] and [17]. Josephson junctions are formed between the base and counter electrodes in superconductor metal layers M5 and M6. This leaves M4 as the obvious ground plane to reduce the inductance from a junction to ground (especially for the parasitic inductance of the resistors added to shunt the Josephson junctions in RSFQ circuits). M7 is then available as a sky plane layer for shielding RSFQ logic cell layouts or for creating the meandering excitation ac line and dc offset line for AQFP logic cell layouts.

For the ColdFlux project [22], a row-based cell-placement strategy is used to stack logic cells [23]. Routing tracks between rows allow the use of all metal layers for interconnect synthesis, while *over-the-cell* routing is only available in the layers below M4–thus effectively transporting signals underneath cells. The distance between interconnected cells can be large compared to the cell size, so that all interconnects are implemented as PTLs.

For a rugged RSFQ cell library with a typical Josephson junction critical current of 250 μA, we require PTLs with a characteristic impedance of about 5 Ω [24]. Such a low impedance requires wide conductors that consume valuable chip real estate when a conductor-above-ground microstrip is used. For striplines, where the conductor is sandwiched between two ground planes, the conductor width is almost halved. We thus maximize the utilization of striplines.

Fig. 1 shows the assignment of microstrip and stripline PTLs in the ColdFlux layout stack, as well as the layers required for logic circuits. All PTLs below the M4 ground plane can be routed anywhere, while PTLs above M4 can only be routed between logic cell rows. The specification of the PTLs below the M4 ground plane is also compatible with AQFP logic even though the AQFP is not ballistically transferring SFQ pulses but rather positive/negative current pulses whose duration is proportional to the system clock period.

B. Placement and Layout of Active Circuits

1) RSFQ: Fig. 2 shows the row-based place and route strategy used by ColdFlux for RSFQ circuits. The track pitch of 10 μm defines all cell and PTL dimensions. Logic cells are designed to be five tracks tall (50 μm) and any integer number of tracks wide. Input and output pins are always laid out to match the tracks.

2) AQFP: The AQFP has two key components: 1) dc SQUID that is magnetically coupled to an excitation clock line, and has a data input/output; 2) output transformer to drive the dc SQUID output across a PTL. The layout of the AQFP logic cell for the MIT-LL SFQ5ee process is based on a minimalist approach [25] in which we use the following four subcells to create AQFP Boolean logic cells.

a) *Buffer:* A nominally designed AQFP in which the output data is a copy of the input data.

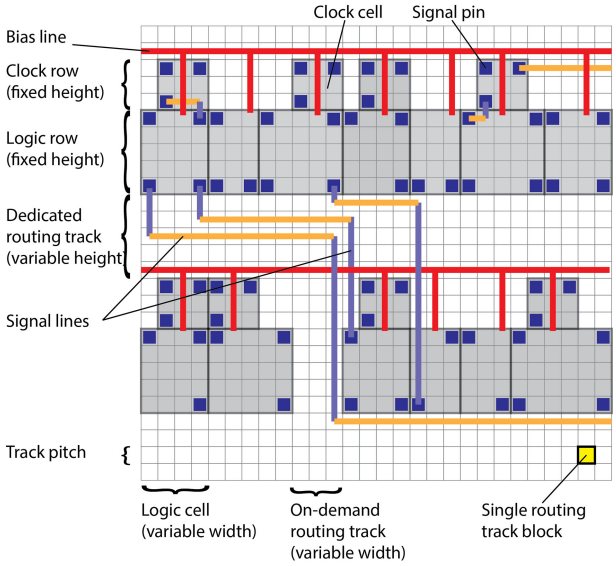

Fig. 2. Schematic representation of the row-based place and route strategy used for RSFQ circuits in ColdFlux.

b) *Inverter:* Similar to the buffer but with an inverted coupling coefficient at the output transformer to generate an inverted copy of the input data at the output.
c) *Constant:* Also similar to the buffer but lacks an input. The layout of the dc SQUID has a slight asymmetry so that a logic "1" or a logic "0" (when the layout is a mirror reflection) is produced when an excitation flux is applied to it.
d) *Branch:* A simple 1-to-2 or 1-to-3 network of inductors used to split the output current generated from a buffer. The same structure can be used in reverse as a 2-to-1 or 3-to-1 confluence that sums up the output currents of multiple subcells into a single output.

This small set of subcells are carefully designed and optimized in a similar fashion as [25]. By using only these four subcells, an expressively rich set of Boolean logic cells can be created including 3-input majority, 2-input AND, and 2-input OR. These logic cells can naturally operate with positive (via buffer subcell) or negative (via inverter subcell) inputs without the additional logic overhead of using discrete inverter cells as they are already integrated into the logic cells.

The buffer, inverter, and constant are designed to each be 30 μm (3 tracks) wide and 40 μm (4 tracks) tall for compatibility with the specified routing architecture. The branch subcell is designed to be 20-μm (2 tracks) tall with its width being an integer multiple of the width of the buffer. With these dimensions in mind, a typical Boolean logic gate (e.g., 2-input AND/OR, 3-input majority) would have a 90-μm width and a 60-μm height. It is important that the width of the subcell is odd-numbered so that the physical layout of the cell is symmetrical to avoid unwanted parasitic couplings. If the width was even-numbered, then the input/output ports would favor the left or right side of the overall cell layout resulting in an asymmetrical structure. Although we can mitigate these parasitic couplings by using the skyplane shield, it is shown in [25] that shielding over the AQFP reduced the coupling coefficient of the output transformer thus severely limiting the maximum distance that an AQFP logic cell can propagate its output.

The AQFP logic cells are magnetically coupled to a 4-phase sinusoidal clock-bias generated by two ac sources and a dc offset [26] serially distributed by the M7 layer. The dc SQUID of the AQFP is on M6. The input port and the driving inductor of the output transformer are on M5 which are then connected to the PTLs below M4. The PTL conductor width used for RSFQ in this routing architecture is 4.5 μm which is wider than what was originally designed for AQFP logic in [25] and [26]. Data are transferred from one AQFP cell to another by means of current $I \approx \Phi_0/L$, where Φ_0 is the magnetic flux quantum and L is the inductance of the conductor in the PTL. The wider conductor used in this routing architecture is not a problem here because it reduces the inductance of the conductor per unit length, allowing the AQFP to propagate its output over longer distances. The AQFP logic cells also follow a row-based placement described in [4] and is compatible with the ColdFlux strategy illustrated in Fig. 2.

3) ERSFQ and LR-Biased RSFQ: For ERSFQ circuits [20], the high kinetic inductance layer L0 provides the requisite high inductance for bias branches. Due to the placement of L0 at the bottom of the MIT-LL SFQ5ee layer stack, this requires bias pillars from the active electronics to L0 for each circuit cell which creates obstructions in the routing layers M1 and M3. ERSFQ can thus use the same place and route strategy as RSFQ, except that routing solutions will require more layout space and will be more difficult to complete.

Similarly to ERSFQ circuits, *LR*-biased [27], [28] RSFQ circuits operating at lower voltages than standard RSFQ require large series bias inductances. If such bias inductors are included in the cell layout, *LR*-biased RSFQ is fully compatible with our track block architecture. However, due to the layout of the track block and the well-defined position of the ground plane holes, bias inductances cannot be raised with ground plane holes as was done in earlier demonstrations [28], [29].

C. Options Not Used

A layout strategy presented in [18] and [19] uses M2 and M3 as striplines between M1 and M4 ground planes. This requires one fewer ground plane, which frees up M0 for a dc power distribution network. It is useful for higher PTL impedance (such as 8 Ω) and when a bias pillar is already necessary to connect ERSFQ bias to the high kinetic inductance layer L0. For the ColdFlux place and route strategy, however, it is inefficient.

First, the dc bias pillars block routing resources in the M2/M3 PTL layers, so that the signal track pitch is 20 μm. In previous work on synthesis, and place and route, we have identified routing as the limiting constraint for large scale circuit synthesis when two (or two-and-a-half) routing layers are available. We thus require maximum utilization of the two-layer signal routing architecture with an unimpeded 10 μm track pitch. To enable this for RSFQ circuits, we put the dc bias above the main ground plane so that no subterranean dc bias pillars are necessary.

Second, the minimum characteristic impedance that we can achieve within the design rules for M2 or M3 striplines between M1 and M4 ground planes is 5.67 Ω when the signal conductor

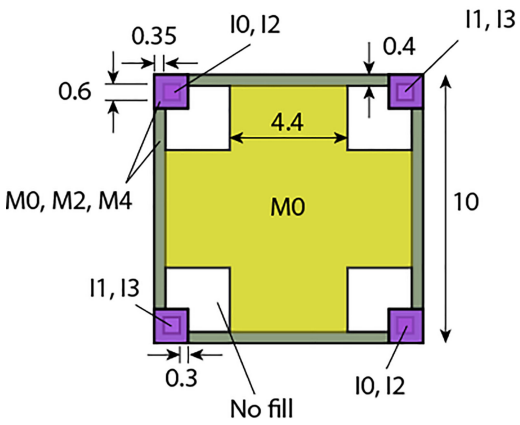

Fig. 3. Dimensions of the basic routing track block. All dimensions are in μm.

is 6.5-μm wide. This structure includes holes in M1 and M4 to keep metal fill below 80%.

We thus do not consider M2-M3-conductor PTLs any further for routing signals in RSFQ or AQFP circuits in the ColdFlux project.

D. Design Rule Requirements

The complete MIT-LL SFQ5ee process design rules are not open to the public, and can thus not be discussed here. However, the routing architecture has been designed to satisfy all width, spacing and overlap limitations for any layer or layer combination.

One limiting rule is of importance: the maximum global density for any metal layer is 80%. Routing blocks are placed everywhere in the active area, so that the metal on each layer in the routing block must fill less than 80% of the block area. This necessitates holes in all ground plane layers, which double as flux trapping moats.

With a few exceptions, via stacking is not allowed. The track block thus must use staggered vias in a way that does not violate design rules for any possible combination of track block placement, signal line routing, signal via insertion, or logic cell placement.

III. Routing Architecture Specifications

A. Dimensions

Fig. 3 shows the dimensions of the basic routing track block.

We designed a layout block for the interconnect infrastructure that is exactly 10 $\times$ 10 μm in size and can be tiled automatically everywhere in the active chip area to provide routing access. The block contains M0 fill and staggered via stacks all the way up to I3 to connect to the main ground plane in M4. At μT flux density (the peak value of the geomagnetic field), there are three fluxons in a 10 $\times$ 10 μm area if the field is perpendicular to the area. We leave four holes in the routing block to provide sufficient flux trapping sites even at full geomagnetic field.

Layer M1 is used for x-axis routing and M3 for y-axis routing. Blocks not used for routing are filled with an M1 or M3 filler to exceed the 15% minimum fill density. Layer M2 is filled with a filler to create a 79% fill density where no M1–M3 vias pass. We fill the main ground plane M4 with a filler similar to that of M2 everywhere outside of logic cells. Bias current is routed on M5 and shielded by M6. We create an M6 ground plane everywhere outside logic cells to allow M7 microstrip lines to ferry clock signals to clock splitters. Clock-line crossover is available through a stripline in unused M5 space where no logic cells or bias distribution exist.

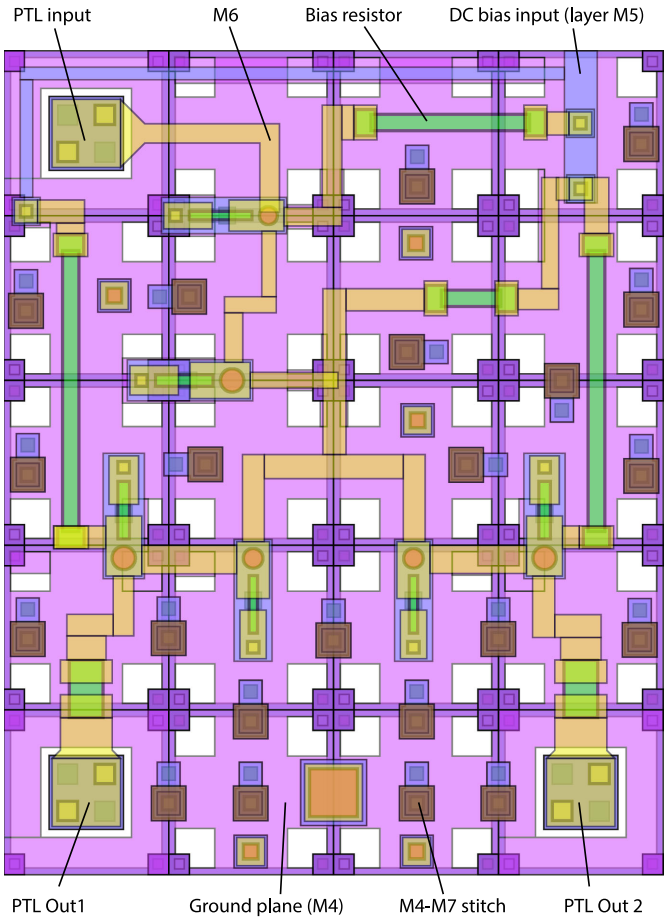

Fig. 4. Example RSFQ splitter layout that fits the routing block architecture.

A three-dimensional (3-D) rendering of an arbitrary composition of track blocks with the ColdFlux track architecture dimensions is shown in Fig. 5. This shows the staggering of stitching vias between metal layers, the fill-in around vias, and the connection of different striplines and microstrip. The fill-in of metal layers such as M1 and M3 where no signal lines are routed is also visible.

This block provides ground plane stitching every 10 μm in both horizontal directions to limit PTL resonance.

All our logic cells are designed to fit the routing block architecture. An example of an RSFQ splitter with a PTL receiver and two PTL drivers integrated in the cell is shown in Fig. 4. The input and output pins connected to vias that connect to M3, and exactly line up with the routing tracks. The M7 sky plane is omitted in this example for clarity. The layout shows how Josephson junctions, inductors, and resistors are placed around the dedicated ground plane holes, and how holes are plugged locally in M4 when circuit components overlap such holes.

B. Layout and Fill Sequence

The layout and fill sequence for RSFQ and AQFP is as follows.

1) The basic routing block is placed everywhere. The block provides M0 at 79% fill, as well as staggered vias I0, I1, I2 and I3 to connect M0 to M4.
2) Logic cells are placed from GDS cell libraries in rows as dictated by the place-and-route tool output constrained to the 10 × 10 μm grid size.
3) Clock splitters are placed from GDS cell libraries in clock rows as dictated by the place-and-route tool output.
4) All PTL tracks are routed as wires in L0 (10-μm wide), M1 and M3 (4.5-μm wide), M5-(5 μm wide) and M7 (8.5-μm wide) as dictated by the place-and-route tool output. For AQFP, M7 is 2-μm wide and is routed as three meandering rails for the two ac clocks and one dc offset with M6 occasionally used to go underneath an M7 obstacle (i.e., a different ac or dc rail).
5) All holes in M0 track blocks that overlap an L0 microstrip are filled.
6) All holes in M6 track blocks that overlap an M7 microstrip are filled except for M7 microstrips passing over AQFP logic cells.
7) All signal lines in M5 are duplicated to M4 and M6 to narrow flux trapping holes and prevent inflation of the stripline characteristic impedance.
8) M0 from the basic routing block is replaced with a via plug for any M1-to-L0 connection.
9) All M1-to-M3 vias, M3-to-M5 vias, and M5-to-M7 vias are filled with via plugs.
10) All bias lines are routed in M5 (4-μm wide between rows, but arbitrary width for trunk lines along chip edge) as dictated by the post place-and-route layout synthesis tool (RSFQ only). If a track block contains a bias line structure in M5, all sides not crossed by the bias line structure receive an M4-to-M6 staggered via to seam the M4 ground plane to an M6 shield tile above and create a caged bias line structure.
11) All tiles (outside of circuit blocks) without M5 are filled with an M5 track fill block.
12) All tiles (outside of circuit blocks) without M6 are filled with M6 shield/ground tiles.
13) Staggered via curtain blocks that connect M4 to M6 are placed along any edge of a bias line block that is not crossed by a bias line structure (RSFQ only).
14) All M6 tiles are seamed to M4 on any tile edge where the seam object does not intersect a bias or transmission lines (RSFQ only).
15) Unused M7 tiles are filled with track fill blocks to maintain fill density but not over AQFP logic cells.

IV. Numerical Analysis of Routing Architecture

A. Electromagnetic Characteristics

For characteristic impedance calculation with InductEx, we used a dielectric permittivity at 4.2 K of 11.7 for the silicon substrate, 4.6 for the silicon dioxide isolation layers, and 1 for the free space above the chip.

Impedance calculation with InductEx is set up to include all holes and vias in the ground plane within one track pitch from the signal lines. Excitation ports are connected to both ground planes for stripline calculations, as shown in the Appendix.

TABLE I
Transmission Line Parameters

PTL	Line width (μm)	Z0 (Ω)	Phase velocity (μm/ps)
M7-M6	8.5	5.30	101.3
M6-**M5**-M4	5.0	5.46	96.9
M4-**M3**-M2	4.5	5.35	95.1
M2-**M1**-M0	4.5	5.35	95.1
L0-M0	10.0	5.52	25.4

The calculated transmission line parameters are shown in Table I. The phase velocity is used for static timing analysis, as well as post-layout simulation of the circuit operation.

For signal line vias between stripline or microstrip conductors, via plug tiles with the same dimensions as the track block are used. Vias between metal layers are staggered to maintain design rule compliance. The ground stitches at the track block corners connect the different ground planes when signal lines are connected, but the gap between the signal center pad and the ground plane "sleeve" can be more than 2 μm. This raises the inductance at the signal via plug, and reduces capacitance, so that characteristic impedance increases. The reflection and transmission S-parameters of a 50 μm section of M3 stripline with matched loads of 5.35 Ω has been calculated with Tetra-Henry and are shown in Fig. 6. A 3-D tetrahedral model of the transmission line sandwiched in the track block discussed here was used for simulation. The S-parameters of a similar structure, where the signal conductor in M3 is connected to M1 through a via plug (labeled "worst") is also shown. It is evident that the reflection coefficient increases significantly.

As mitigation, we use a signal via plug that pulls a ground sleeve closer to the signal via pad and adds extra ground stitches on open edges of the signal via block (as can be seen in the 3-D renderings in Fig. 5). This via, labeled "best" in Fig. 6 performs better. From the results, we expect the SFQ signal power loss up to 400 GHz for 100 vias to be about 1 dB, which is acceptable for the ColdFlux place and route strategy.

The "best" via is shown in Fig. 7 as it is modeled with Inductex for S-parameter calculation or inductance calculation. In this example, the current distribution is shown when the M1–M3 signal line is excited. It is clear that provision must be made for ground plane return current to shift between ground planes in close proximity to the via.

B. Performance

1) Bias Line Shielding: Bias lines carry current that couple to superconductive circuit loops. We limit the maximum current in any bias track to 100 μA (out of a process limitation of 120 μA for a 4 μm wide line in M5).

Any bias line will couple to superconductor loops in its vicinity. There is no clear guideline for the acceptable maximum coupling between bias lines and superconductor electronic circuits, so we set out to establish such guidelines. As a starting point, we use a typical two-junction SQUID with $I_c = 500\ \mu A$ and a 6-pH loop inductance in layer M6 of the MIT-LL SFQ5ee

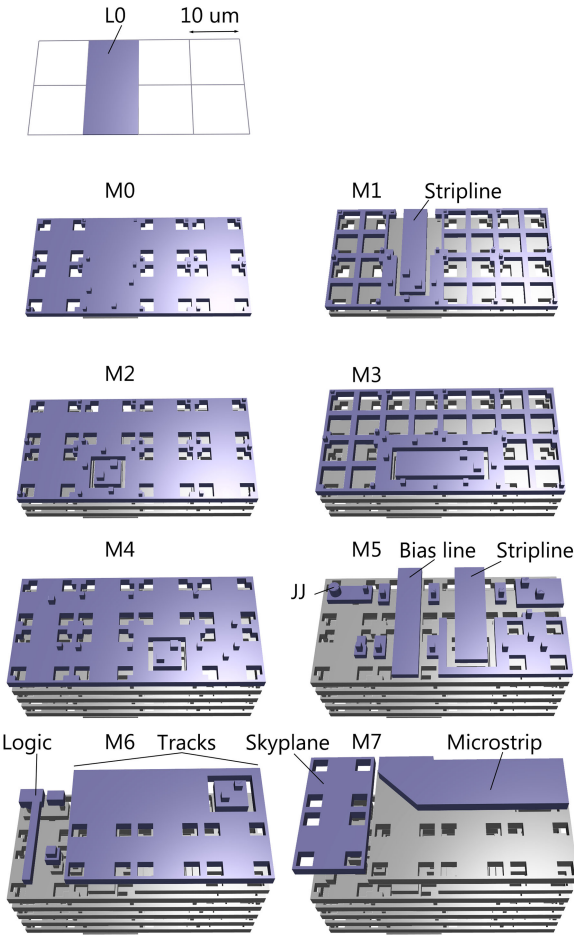

Fig. 5. Three-dimensional rendering of an arbitrary 4 × 2 track block composition. The vertical dimension has been scaled up by a factor of eight for clarity.

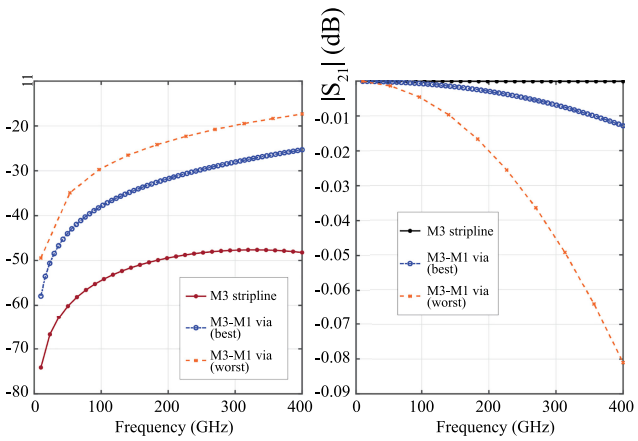

Fig. 6. S-parameters for a 50 μm length of stripline in M3, with via options to M1, as calculated with TetraHenry. Matched loads are 5.35 Ω.

process. Each junction has $I_c = 250\ \mu A$, which is the standard value for our RSFQ cells.

From experiments [30] and verification with InductEx [31], it is known that if a typical flux trapping moat of 1-μm width located 1 μm from the edge of the SQUID loop inductor and runs the entire length of this inductor, is filled with one magnetic flux

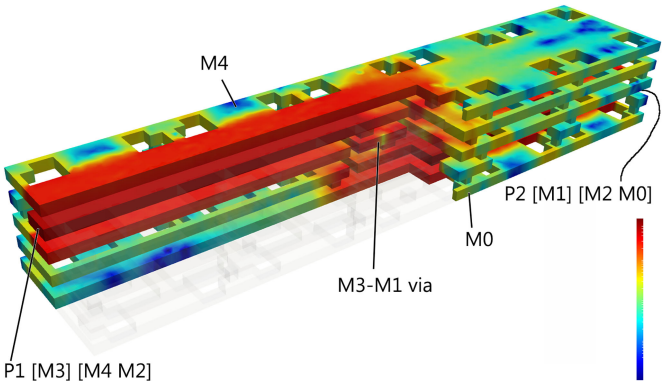

Fig. 7. Cross section of a 3-D simulation model for the M3-to-M1 stripline transition with an optimially filled via. The vertical dimension has been scaled up for clarity. The logarithmic current density profile over four orders of magnitude when the input on M3 and the output on M1 are excited is shown, as calculated with InductEx.

quantum, then the resulting dc current induced in the SQUID loop is approximately 20 μA and I_c for the SQUID is lowered by 4%. With proper moat design, subsequent flux trapping counteracts this induced current, so that the worst case I_c deviation should not exceed 5%.

We can limit the maximum change in I_c caused by an energized bias current line to 5% to match the effects of typical moats, but as we show in [30] it is possible to design moats with less coupling. We also have observed shifted circuit operating margins when flux is trapped in moats. We thus propose the design of bias current lines that limit the deviation in I_c for our example SQUID to a maximum of 1%.

For the evaluation of bias current coupling, we use InductEx. The layout of the bias line is modeled, together with the full track block architecture. A 500-μA SQUID with loop inductance in M6 is included, with the center line of the SQUID loop inductance either 10 μm (one track pitch) or 20 μm from the center of the bias line. In our circuit layouts, a local bias ring at the cell edges (in M5) result in all active electronics being at least 5 μm from the cell edges, so that 10 μm is the minimum expected distance of any circuit inductor to a bias line center. The SQUID is biased at $0.7I_c$, which is typical for RSFQ circuits.

With InductEx, the coupling from the bias line to the SQUID loop is calculated for both distances, as well as for two layout options: one where the SQUID only has an M4 ground plane and two where the SQUID is also shielded with an M7 sky plane that is stitched to M4. For each of these four possibilities, we evaluate the coupling from a bias line in M7, a bias line in M5, and a caged M5 bias line that fits in our track block layout. From the mutual inductance, we calculated the current induced in the SQUID loop if the nonlinear Josephson inductance is taken into account. The results are shown in Table II, where the induced current in the SQUID is calculated for 100 μA of bias current and ignores switching.

It is clear that M7 bias line performs very badly, inducing enough current to switch the open and shielded SQUID junctions at 10 and 20 μm (the SQUID switches when the induced current reaches about 175μA.) The M5 bias line is almost four times better, but the caged M5 bias line has two orders of magnitude

TABLE II
BIAS LINE COUPLING TO AN 500 μA SQUID WITH LOOP INDUCTOR IN M6 WHERE BIAS CURRENT IS 100 μA

Bias line (distance)	Open SQUID		M7 shielded SQUID	
	M_{par} (H)	I_{ind} (μA)	M_{par} (H)	I_{ind} (μA)
M7 (10 μm)	1.089E-13	916.9	2.326E-14	204.8
M7 (20 μm)	3.850E-14	324.2	1.015E-14	89.3
M5 (10 μm)	3.399E-14	286.2	7.092E-15	62.4
M5 (20 μm)	1.215E-14	102.2	3.216E-15	28.3
M5 caged (10 μm)	1.392E-15	11.2	1.645E-16	1.45
M5 caged (20 μm)	4.308E-16	3.62	9.782E-17	0.86

Bias line distance is measured from the center of the bias line to the center of the SQUID loop inductor.

TABLE III
MAXIMUM BIAS CURRENT ALLOWED IN A BIAS LINE TO LIMIT THE CHANGE IN CRITICAL CURRENT OF A 500-μA SQUID TO 1%

Bias line (distance)	Open SQUID (mA)	M7 shielded SQUID (mA)
M7 (10 μm)	0.55	2.44
M7 (20 μm)	1.54	5.60
M5 (10 μm)	1.75	8.91
M5 (20 μm)	4.89	17.7
M5 caged (10 μm)	42.8	345
M5 caged (20 μm)	138	581

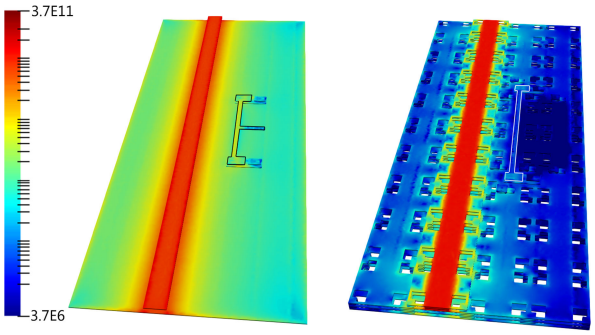

Fig. 8. Current distribution as calculated with InductEx for a bias line in M7 over a solid ground plane in M4 near an unshielded victim SQUID (on the left) and a caged bias line in M5 near a victim SQUID shielded with an M7 skyplane (on the right). The current density scale is in A/m^2. Both bias lines are excited with a current of 100 μA. The induced current in the ground plane underneath the SQUID and the SQUID loop are orders of magnitude lower when the bias line is in M5 and caged, as is also evident in Table II.

lower coupling to the SQUID. From the results, it is clear that the caged M5 bias line can be used with sky plane shielded circuitry even at one track pitch separation of 10 μm.

Table III shows the maximum current that can be fed through a bias line to limit the deviation in the critical current of the SQUID to less than 1%. The caged M5 bias line is safe up to and beyond 100 μA.

Fig. 8 shows the current distribution calculated with InductEx for two bias current routing and shielding configurations. The bias line is always 4-μm wide, and the center of the victim SQUID loop inductor is 10 μm from the center of the bias line. The unshielded SQUID on the left has a loop inductance of 6 pH. The shielded SQUID on the right has a loop inductance of 5.5 pH.

2) Flux Trapping Moats: The critical field (see [32] for a detailed discussion) of the flux trapping holes is calculated with InductEx and TetraHenry as 18.1 μT for holes from M0 to M4 and M7 (used for logic circuits) and 18.7μT for holes from M0 to M7 (all metal layers inclusive) as used for routing tracks. These holes are the no-fill areas visible in Fig. 3.

With InductEx, we calculate the current induced in a 500-μA SQUID with its loop inductor placed at the center of a track block as 0.64 μA per fluxon. Due to symmetry in the moat placement, we expect fluxons to trap with near equal density on both sides of an inductor, so that it is safe to assume a maximum fluxon-induced current of about 1 μA in any similar circuit inductor, which is acceptable.

V. CONCLUSION

We have designed a routing track architecture for the multi-layer MIT Lincoln Laboratories SFQ5ee process that adheres to all design rules and layer fill requirements and allows the automated physical synthesis of bias, clock and signal routing in RSFQ and AQFP circuits after logic synthesis and place and route using S-EDA tools. This closes the gap between high level design and the tape-out of layout masks for large-scale superconductor digital circuits.

Thorough characterization has been done to ensure that the routing track architecture adheres to the requirements of our circuit libraries. We show that all required characteristic impedances can be achieved, that the flux trapping holes are sufficient for practical field strengths, that coupling from holes to circuit structures is sufficiently small, that bias lines with 100-mA dc current can be pumped through bias lines while coupling to circuits are maintained within tight limits, and that the frequency response of transmission line vias are acceptable for more than 30 vias between drivers and receivers.

Although the dimensions of a track block may need to be adapted, the same track architecture can be used in other multilayer processes with at least eight metal layers. Due to fill requirements, we do not foresee a reduction in track pitch if stacked vias are allowed in future SFQ*x*ee fabrication process nodes.

APPENDIX

The InductEx setup procedure is provided for the numerical calculation of the characteristic impedance for the M3 stripline discussed in this article. This allows complete reproduction of the results and serves as a starting point for reproduction of any of the other results presented here, or for the evaluation of alternate routing solutions.

The geometry of the a 50-μm length of M3 stripline is described fully in Fig. 9. The track block layout can be reproduced from this layout file. Ports are declared with the positive terminals on layer M3 and the negative terminals on both layers M4 and M2. A reduced version of the MIT Lincoln Laboratory SFQ5ee process file for InductEx is shown in Fig. 10. The 3-D model of the M3 stripline and the InductEx calculation of the characteristic impedance can be reproduced with these two files and the InductEx command:

```
inductex ptlm3.ixi
```

```
$PARAMSTRING
  -l mitllredux.ldf -z
$END
$STRUCT
  Name routeblockm2
  $POLY
    Layer M2
    XY
    ( 2.8, 0.4 )
    ( 7.2, 0.4 )
    ( 7.2, 2.8 )
    ( 9.6, 2.8 )
    ( 9.6, 7.2 )
    ( 7.2, 7.2 )
    ( 7.2, 9.6 )
    ( 2.8, 9.6 )
    ( 2.8, 7.2 )
    ( 0.4, 7.2 )
    ( 0.4, 2.8 )
    ( 2.8, 2.8 )
    ( 2.8, 0.4 )
  $END
$END
$STRUCT
  Name routeblock
  $POLY
    Layer M2
    XY
    (  8.75, 10    )
    (  8.75,  8.75 )
    (  9.6,   8.75 )
    (  9.6,   1.25 )
    (  8.75,  1.25 )
    (  8.75,  0.4  )
    (  1.25,  0.4  )
    (  1.25,  1.25 )
    (  0.4,   1.25 )
    (  0.4,   8.75 )
    (  1.25,  8.75 )
    (  1.25,  9.6  )
    (  8.75,  9.6  )
    (  8.75, 10    )
    (  0,    10    )
    (  0,     0    )
    ( 10,     0    )
    ( 10,    10    )
    (  8.75, 10    )
  $END
  $POLY
    Layer M4
    XY
    (  8.75, 1.25 )
    ( 10,    1.25 )
    ( 10,    0    )
    (  8.75, 0    )
    (  8.75, 1.25 )
  $END
  $POLY
    Layer M4
    XY
    ( 0,    1.25 )
    ( 1.25, 1.25 )
    ( 1.25, 0    )
    ( 0,    0    )
    ( 0,    1.25 )
  $END
  $POLY
    Layer M4
    XY
    (  8.75, 10    )
    ( 10,    10    )
    ( 10,     8.75 )
    (  8.75,  8.75 )
    (  8.75, 10    )
  $END
  $POLY
    Layer M4
    XY
    ( 0,    10    )
    ( 1.25, 10    )
    ( 1.25,  8.75 )
    ( 0,     8.75 )
    ( 0,    10    )
  $END
  $POLY
    Layer I3
    XY
    ( 9.05, 9.65 )
    ( 9.65, 9.65 )
    ( 9.65, 9.05 )
    ( 9.05, 9.05 )
    ( 9.05, 9.65 )
  $END
  $POLY
    Layer I3
    XY
    ( 0.35, 0.95 )
    ( 0.95, 0.95 )
    ( 0.95, 0.35 )
    ( 0.35, 0.35 )
    ( 0.35, 0.95 )
  $END
  $POLY
    Layer M3
    XY
    (  8.75, 1.25 )
    ( 10,    1.25 )
    ( 10,    0    )
    (  8.75, 0    )
    (  8.75, 1.25 )
  $END
  $POLY
    Layer M3
    XY
    ( 0,    1.25 )
    ( 1.25, 1.25 )
    ( 1.25, 0    )
    ( 0,    0    )
    ( 0,    1.25 )
  $END
  $POLY
    Layer M3
    XY
    (  8.75, 10    )
    ( 10,    10    )
    ( 10,     8.75 )
    (  8.75,  8.75 )
    (  8.75, 10    )
  $END
  $POLY
    Layer M3
    XY
    ( 0,    10    )
    ( 1.25, 10    )
    ( 1.25,  8.75 )
    ( 0,     8.75 )
    ( 0,    10    )
  $END
  $POLY
    Layer I2
    XY
    ( 9.05, 0.95 )
    ( 9.65, 0.95 )
    ( 9.65, 0.35 )
    ( 9.05, 0.35 )
    ( 9.05, 0.95 )
  $END
  $POLY
    Layer I2
    XY
    ( 0.35, 9.65 )
    ( 0.95, 9.65 )
    ( 0.95, 9.05 )
    ( 0.35, 9.05 )
    ( 0.35, 9.65 )
  $END
$END
$STRUCT
  Name routeblockm4
  $POLY
    Layer M4
    XY
    (  1.25, 10    )
    (  1.25,  9.6  )
    (  2.8,   9.6  )
    (  2.8,   7.2  )
    (  0.4,   7.2  )
    (  0.4,   8.75 )
    (  0,     8.75 )
    (  0,     1.25 )
    (  0.4,   1.25 )
    (  0.4,   2.8  )
    (  2.8,   2.8  )
    (  2.8,   0.4  )
    (  1.25,  0.4  )
    (  1.25,  0    )
    (  8.75,  0    )
    (  8.75,  0.4  )
    (  7.2,   0.4  )
    (  7.2,   2.8  )
    (  9.6,   2.8  )
    (  9.6,   1.25 )
    ( 10,     1.25 )
    ( 10,     8.75 )
    (  9.6,   8.75 )
    (  9.6,   7.2  )
    (  7.2,   7.2  )
    (  7.2,   9.6  )
    (  8.75,  9.6  )
    (  8.75, 10    )
    (  1.25, 10    )
  $END
$END
$STRUCT
  Name ptlm3
  $PATH
    Layer M3
    width 4.5
    XY
    (  0, 5 )
    ( 50, 5 )
  $END
  $SREF
    Name routeblock
      XY
      ( 40, 0 )
  $END
  $SREF
    Name routeblock
      XY
      ( 30, 0 )
  $END
  $SREF
    Name routeblock
      XY
      ( 20, 0 )
  $END
  $SREF
    Name routeblock
      XY
      ( 10, 0 )
  $END
  $SREF
    Name routeblock
      XY
      ( 0, 0 )
  $END
  $SREF
    Name routeblockm2
      XY
      ( 40, 0 )
  $END
  $SREF
    Name routeblockm2
      XY
      ( 30, 0 )
$END
$SREF
  Name routeblockm2
    XY
    ( 20, 0 )
$END
$SREF
  Name routeblockm2
    XY
    ( 10, 0 )
$END
$SREF
  Name routeblockm2
    XY
    ( 0, 0 )
$END
$SREF
  Name routeblockm4
    XY
    ( 40, 0 )
$END
$SREF
  Name routeblockm4
    XY
    ( 30, 0 )
$END
$SREF
  Name routeblockm4
    XY
    ( 20, 0 )
$END
$SREF
  Name routeblockm4
    XY
    ( 10, 0 )
$END
$SREF
  Name routeblockm4
    XY
    ( 0, 0 )
$END
$PATH
  Layer TERM
  Text "Z1 [M3] [M4 M2]"
  XY
  ( 0, 7.25 )
  ( 0, 2.75 )
$END
$PATH
  Layer TERM
  Text "Z2 [M3] [M4 M2]"
  XY
  ( 50, 7.250 )
  ( 50, 2.750 )
$END
$END
```

Fig. 9. Geometry file for characteristic impedance extraction of M3 stripline.

```
$Parameters
  Units             =  1e-6
  SegmentSize       =  0.5
  AbsMin            =  0.025
  ProcessHasGroundPlane = TRUE
  LastDieLayerOrder =  10
  GPLayer           =  40
  TermLayer         =  19
  TextLayer         =  18
  TerminalInRange   =  1.0
  EpsilonR          =  4.6
  EpsilonRBelow     =  11.7
  EpsilonRAbove     =  1
$End
$Layer  // M2 conductor
  Number      =  20
  Name        =  M2
  Thickness   =  0.200
  Lambda      =  0.090
  Order       =  6
  Mask        =  1
  Filmtype    =  S
$End
$Layer  // I2 isolation
  Number      =  21
  Name        =  I2
  Thickness   =  0.200
  Order       =  7
  Mask        = -1
  Filmtype    =  I
  EpsilonR    =  4.6
$End
$Layer // M3 conductor
  Number      =  30
  Name        =  M3
  Thickness   =  0.200
  Lambda      =  0.09
  Order       =  8
  Mask        =  1
  Filmtype    =  S
$End
$Layer  // I3 isolation
  Number      =  31
  Name        =  I3
  Thickness   =  0.200
  Order       =  9
  Mask        = -1
  Filmtype    =  I
  EpsilonR    =  4.6
$End
$Layer // M4 global ground
  Number      =  40
  Name        =  M4
  Thickness   =  0.200
  Lambda      =  0.09
  Order       =  10
  Mask        =  1
  Filmtype    =  S
$End
```

Fig. 10. Layer definition file with minimum layer information for characteristic impedance extraction of M3 stripline.

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Appendix D

Conference paper - Standard Cell Layout Synthesis for Row-Based Placement and Routing of RSFQ and AQFP Logic Families

- L. Schindler, R. van Staden, C. J. Fourie, C. L. Ayala, J. A. Coetzee, T. Tanaka, R. Saito and N. Yoshikawa, "Standard Cell Layout Synthesis for Row-Based Placement and Routing of RSFQ and AQFP Logic Families," 2019 IEEE International Superconductive Electronics Conference (ISEC). [42]

The work presented within this article is a collaborative effort between teams from Stellenbosch University and Yokohama National University in Japan. The layout synthesis tool was developed by R. van Staden and extended by J. A. Coetzee. The implementation of the tool for RSFQ and AQFP logic cell layouts was contributed by the remaining co-authors. The copyright for this paper is held by IEEE Transactions on Applied Superconductivity.

Standard Cell Layout Synthesis for Row-Based Placement and Routing of RSFQ and AQFP Logic Families

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***Abstract*—In this work under the IARPA SuperTools program we developed a layout synthesis tool with scripting support. The user specifies the relative positions of Josephson junctions and inductances constrained by a user-defined cell height and cell width. Tight integration with the three-dimensional inductance extraction tool, InductEx, allows inductances to be automatically generated while meeting reasonable design values. Based on these user inputs, the tool can synthesize the physical layout of logic cells for multiple SFQ circuit technologies according to design rules and layer parameters. Furthermore, it enables the straightforward regeneration of entire cell libraries when design rules change or when libraries have to be redesigned for more advanced fabrication processes. We describe the methodology of our synthesis tool and show the results applied to both RSFQ and AQFP logic families.**

***Index Terms*—layout synthesis, paramterized cells, superconductor circuits**

I. Introduction

The SuperTools research program funded by IARPA is a large development effort to produce electronic design automation (EDA) tools for the design of very-large-scale integration (VLSI) superconductor electronics [1]. Under the SuperTools program, the development of standard logic cell libraries that are compatible with automated placement and routing algorithms is required. Standard cell layouts need to conform to row dimensions, as well as to routing track pitch dimensions on which the place-and-route tools operate. The layout revision cost of entire logic cell libraries is inflated by the evolution of the MIT Lincoln Laboratory (MIT-LL) SFQ fabrication process due to changes in design rules such as minimum or maximum dimensions, spacing and surround values to change and layer parameters to shift [2].

We present a layout synthesis tool with scripting support, a subdivision of SPiRA [3], as an alternative to layout synthesis by hand. A set of user-defined parameters forms the basis of a parameterized cell (PCell). A PCell describes how layout elements must be generated according to defined parameters. SPiRA takes a set of user-defined parameters as input, processes the given parameters and automatically generates a layout in GDSII format. SPiRA integrates with InductEx for impedance extraction and has an integrated design rule checker to confirm that no design rules are broken within the layout. The fabrication process can be customized within the script providing the user with the option to simply update the parameters and regenerate the layout if the need arises.

II. Standard Cell Library

Standard RSFQ and AQFP logic cell libraries for layout synthesis have been developed for the ColdFlux project [4], which falls under the IARPA SuperTools program. The RSFQ library follows the fixed-height but variable width methodol-

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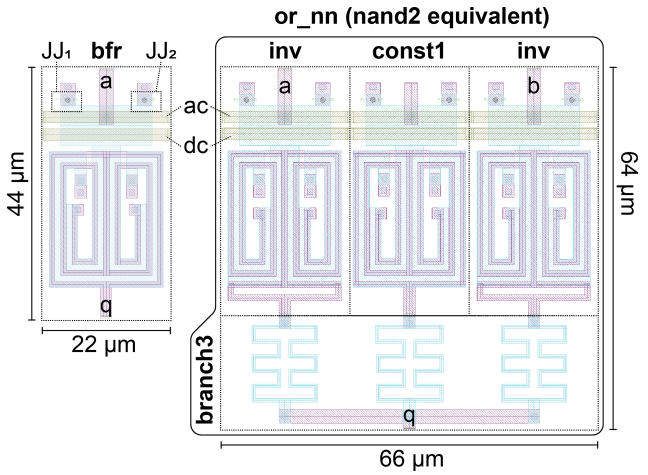

Fig. 1. Layout of the AQFP buffer (bfr) and NAND gate (or_nn). The critical current of both JJ_1 and JJ_2 are 50 μA. The NAND gate consists of two inverters (inv), a single constant-1 (const1) sub-cell, and a branch3 sub-cell which does an additive merge (majority operation) on the connected sub-cells. Note that the sub-cell footprints as well as the ac and dc rails are all uniform in the cell design so that sub-cells can be abutted together to form more complex Boolean logic cells.

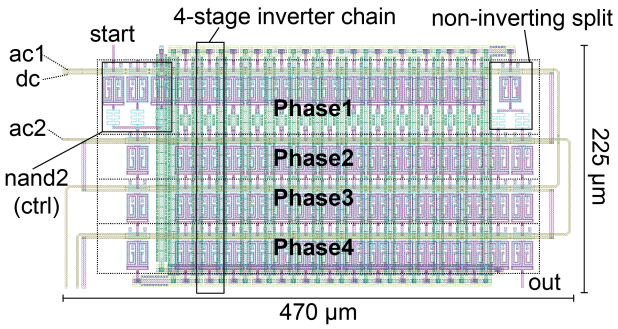

Fig. 2. Row-based layout of an AQFP inverting circular shift register consisting of 59 inverting stages. Cells clocked by the same clock phase co-exist on the same row and are abutted together to form the clock-power networks consisting of ac and dc microstrip lines in each row. A NAND2 gate provides a way to control the oscillator through an active-high 'start' signal.

ogy proposed in [5]. This allows for the cells to be placed in predefined rows for a more area-efficient chip design. This methodology allows for the use of CMOS-based place-and-route tools.

AQFP cells also follow a fixed-height variable-width methodology as shown in Fig. 1. First a set of sub-cells have been designed for AQFP, namely: bfr (buffer), inv (inverter), const1/0 (constant-1 or constant-0), and branch [6], [7]. Each sub-cell has been carefully sized so they can be abutted together to form Boolean logic gates which can be seen in Fig. 1 for the or_nn cell (OR gate with two negative inputs, equivalent to a nand2 gate). For example, the active sub-cells (bfr, inv, and const) are all the same size with identical pin positioning. Each of those active sub-cells have a standardized placement of the power-clock rails (ac and dc) such that by abutting sub-cells (or their higher-level compositions), a power-clock network forms in each row. This is applied in a row-based design of an AQFP inverting circular shift register consisting of 59 inverting stages in a feedback loop as shown in Fig. 2. Cells belonging to the same clock phase share the same row and are abutted together to form the power-clock rails for that row. Data propagates from one phase to the next (modulo 4) through stripline PTLs.

RSFQ cells are connected using passive transmission lines (PTLs) during the routing algorithm. PTL drivers and receivers are therefore required to ensure that a pulse propagates through a PTL. The RSFQ cell library includes additional cells with integrated PTL drivers and receivers. AQFP cells are also connected using PTLs which can be placed both manually or automatically through a channel routing algorithm. Unlike RSFQ cells, AQFP cells can directly drive and receive data using PTLs without a separate driver or receiver circuit. The PTLs are used to propagate positive (or negative) current as data instead of SFQ pulses. The drawback is that the current signals on long PTLs experience attenuation due to large parasitic inductance. This limits cell-to-cell PTL lengths to approximately 1 mm before the AQFP cannot correctly determine the logic state of the signal [7]. The solution for this is to insert another buffer (or several as needed) as a repeater to re-amplify the signal.

III. Layout Synthesis Methodology

Superconducting circuit designers have to currently lay out each cell by hand. This can be extremely time consuming, especially if the user is inexperienced or unfamiliar with the fabrication process. We are developing a tool, named SPiRA [8], which can automatically generate a cell layout utilizing user-defined parameters within a script. A complete introduction to SPiRA and its capabilities is presented in [3].

Cell layouts can be scripted as Python-based parameterized cells (PCells). PCells include user-defined information regarding cell width and height, junction sizes, junction placements, inductor values, width and placement along with port placements and other information required for impedance extraction. The tool uses the PCell script to generate a cell layout in GDSII format. The layout then undergoes design-rule-checking (DRC) and error feedback is collected and stored. If DRC errors are present within the layout, the layout synthesis tool gives error feedback to the user. If no DRC errors are detected, the layout is sent to InductEx [9] for impedance extraction. The results from InductEx can then be processed and the layout adjusted if the extracted values differ from the design values. The layout is once again checked for DRC errors. The iterative process continues until the extracted vales are within a certain tolerance specified by the user.

Once the extracted inductance and resistance values correlate with the designed values, the user can run the built-in SPiRA layout-versus-schematic (LVS) tool to extract the electrical schematic represented in the circuit layout. Electrical simulation can then be used to verify the operation of the circuit.

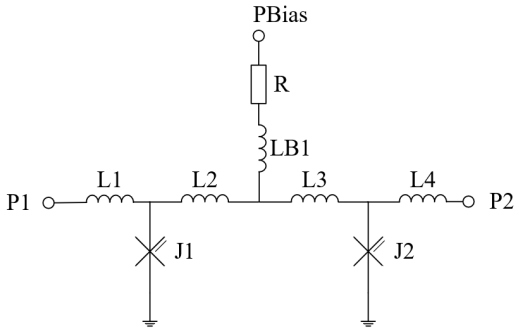

Fig. 3. Schematic of an RSFQ JTL with shunted JJs used as a reference for a layout script. Designed values are $L_1 = L_2 = L_3 = L_4 = 2$ pH, J_c=250 μA and I_b=350 μA (R=7.429 Ω with Vb=2.6 mV)

IV. Layout Script Example

We present an example layout script to show how a user can set up a SPiRA-compatible PCell. The script contains multiple user-defined parameters. It is important to note that SPiRA only generates the layout defined by the user through the PCell script. The current version of SPiRA does not improve the layout itself. The reliability of the design is only as good as the DRC and electrical rule checks as defined in the process design kit. Future work includes the integration with InductEx for automated impedance extraction feedback, and the implementation of this feedback to adjust the layout (for example inductor width) to better correlate the designed and extracted inductance and resistance values.

The following script provides an example of how a Josephson Transmission Line (JTL) PCell can be scripted with SPiRA compatibility. The schematic of the JTL is shown in Fig. 3.

```
class Jtl(spira.Circuit):
    p1 = spira.Parameter(fdef_name='create_p1')
    p2 = spira.Parameter(fdef_name='create_p2')
    p3 = spira.Parameter(fdef_name='create_p3')
    jj1 = spira.Parameter(fdef_name='
        create_jj_100sg_0')
    jj2 = spira.Parameter(fdef_name='
        create_jj_100sg_1')
    res0 = spira.Parameter(fdef_name='create_res_0')
    via_i5 = spira.Parameter(fdef_name='
        create_via_i5')

    def create_p1(self):
        return spira.Port(name='T1', midpoint
            =(-10,8), orientation=0, width=1)

    def create_p2(self):
        return spira.Port(name='T2', midpoint=(10,8)
            , orientation=180, width=1)

    def create_p3(self):
        return spira.Port(name='T3', midpoint=(0,28)
            , orientation=270, width=1.5)

    def create_jj_100sg_0(self):
        jj = dev.Junction(width=1, gnd_via=True,
            sky_via=True)
        T = spira.Translation((-3.4, 1.1)) + spira.
            Rotation(180)
        return spira.SRef(jj, transformation=T)

    def create_jj_100sg_1(self):
        jj = dev.Junction(width=1, gnd_via=True,
            sky_via=True)
        T = spira.Translation((3.4, 1.1)) + spira.
            Rotation(180)
        return spira.SRef(jj, transformation=T)

    def create_res_0(self):
        res = Resistor()
        T = spira.Translation((0, 15)) + spira.
            Rotation(90)
        return spira.SRef(res, transformation=T)

    def create_via_i5(self):
        via = dev.ViaI5()
        V = spira.SRef(via)
        V.connect(port=V.ports['M6_P2'], destination
            =self.res0.ports['M6_P4'])
        return V

    def create_structures(self, elems):
        elems += [self.jj0, self.jj1]
        elems += self.res0
        elems += self.via_i5
        return elems

    def create_routes(self, elems):

        elems += RouteManhattan(
            ports=[self.jj0.ports['M6_P1'], self.p1
                ],
            width=1, layer=RDD.PLAYER.M6.METAL,
            corners=self.corners)

        elems += RouteManhattan(
            ports=[self.jj1.ports['M6_P3'], self.p2
                ],
            width=1, layer=RDD.PLAYER.M6.METAL,
            corners=self.corners)

        elems += RouteStraight(p1=self.p3,
            p2=self.via_i5.ports['M5_P0'].copy(width
                =1.5),
            layer=RDD.PLAYER.M5.METAL)

        elems += RouteStraight(
            p1=self.res0.ports['M6_P2'].copy(width
                =2),
            p2=spira.Port(midpoint=(0,10),
                orientation=90, width=1, port_type='
                dummy'),
            width_type='sine',
            layer=RDD.PLAYER.M6.METAL)

        pl = spira.PortList()
        pl += self.jj0.ports['M6_P0']
        pl += spira.Port(midpoint=(0,10),
            orientation=180, port_type='dummy')
        pl += self.jj1.ports['M6_P0']
        elems += RouteManhattan(ports=pl, width=1,
            layer=RDD.PLAYER.M6.METAL, corners=self.
            corners)

        return elems

    def create_elements(self, elems):
        el = spira.ElementList()
        el += self.structures
        el += self.routes
        margin = 1
```

```
        box_shape = el.bbox_info.bounding_box(margin
            )
        elems += spira.Polygon(shape=box_shape,
            layer=spira.Layer(40))
        elems += spira.Polygon(shape=box_shape,
            layer=spira.Layer(70))
        return elems

    def create_ports(self, ports):
        ports += [self.p1, self.p2, self.p3]
        return ports
```

The script starts off by creating a JTL class. Three ports parameters are defined as `p1`, `p2` and `p3`. These ports are required by InductEx for impedance extraction and, for a JTL circuit, typically represent the input port, the output port and the biasing line port. The Josephson junction (JJ) parameters are then defined by `jj0` and `jj1`. The biasing resistor parameter, `res0`, and a via parameter, `via_i5`, are also defined.

The port parameters also specify a function definition, `fdef_name`. This function definition specifies the port name, the centre point, the width and orientation of the port. Similar functions define the size, placement and orientation of the JJ, biasing resistor and via structures.

The JJ, biasing resistor and via structures are then defined as elements to be connected together through inductors. These connections between structures are spawned through the `create_routes` function - which define routing elements between newly created ports (`M6_P1`, `M6_P3`, `M5_P0`, `M6_P2`) and ports defined at the beginning of the script (`p1`, `p2`, `p3`). The width of the routing is set to 1 μm.

The elements are then created and the polygons representing the ground and sky planes are calculated and created. The port elements are also created to complete the JTL class. The JTL class is called from the main script to create the GDSII layout file.

V. Preliminary Results

An example RSFQ JTL layout was scripted, as described in Section IV, and generated using SPiRA. The resulting layout of the JTL is shown in Fig. 4. The size, orientation and placement of junctions and the biasing resistor were specified. Inductor values were defined through the routing connections and width specifications. Port information, used by InductEx, was also included in the script. The layout underwent DRC and the layer density was extracted. SPiRA currently does not have the functionality to generate additional fill structures or moats within a layout to comply with layer density specifications, but the information can be applied by the user to adjust the PCell script.

InductEx was used for inductance and resistance extraction for the first iteration of layout generation. The extracted impedance values are compared to the designed values in Table I. It is seen that the values inductors L_1 and L_4 are much higher than the designed values. The dimensions of the biasing line resistor, R, also has to be adjusted to reduce the risk of circuit malfunction due to lowered biasing current. This

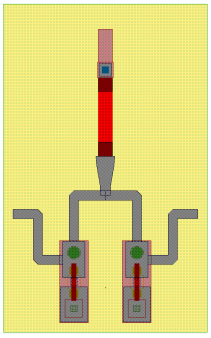

Fig. 4. Layout of JTL with ground plane generated by SPiRA. Extracted values are $L_1 = L_4 = 2.018$ pH, $L_2 = L_3 = 1.724$ pH, J_c=254 μA and I_b=334 μA (R=7.782 Ω with Vb=2.6 mV).

TABLE I
Comparison of Designed and Extracted Parameter Values for the First Iteration of Automated Layout Generation.

Parameter	Design value	Extracted value	% Difference
L1, L4	2.0 pH	3.011 pH	+50.57 %
L2, L3	2.0 pH	2.157 pH	+7.83 %
R_b	7.429 Ω	9.591 Ω	+29.10 %
I_b	350 μA	271.09 μA	-22.55 %

information is an example of necessary feedback to SPiRA required to improve the layout script.

The PCell scripts are not generated by SPiRA, but written by a user and this leads to the possibility of human error. The feedback acquired from inductance and resistance extraction can, in the future, be implemented by SPiRA to adjust the PCell script to better correlate the layout script with the designed inductance values without additional user input.

The main advantages of SPiRA is that a user only has to script a PCell once to represent a cell layout, regardless of the fabrication process. Several fabrication processes are supported by SPiRA and if the cell layout is required for a different fabrication process, the user can simply select a different fabrication process from the rule-deck-database and SPiRA can generate the cell layout for the specified process.

VI. Conclusion

A working layout synthesis tool with scripting support was presented. User-defined parameters are included within a script which SPiRA uses to generate a layout. The tool includes its own DRC and can integrate with InductEx for impedance extraction. The tool provides the user with the opportunity to fully customize the layout through a script, and the layouts can be regenerated with ease if adjustments to user-defined parameters are made.

Additionally, the exploration and co-optimization of logic cell libraries and the "quality-of-result" (QoR) of place-and-route tools can be aided with a layout synthesis tool such as SPiRA. Chip-level QoR is not just a place-and-route optimization problem but it is also influenced by standard cell design. With the synthesis tool we can hereafter explore

good pin placements within the cell, track pitch dimensions, and other standard cell properties by creating a collection of standard cell libraries and evaluating which place-and-route tools give the best QoR results for a set of benchmark circuits. Likewise, it aids in the development of place-and-route tools to try alternative algorithms or strategies that call for more experimental cell design, a feedback process that can be significantly sped up through cell layout synthesis.

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Appendix E

Phase-Based Equations for Designed RSFQ Cell Library

RSFQ DFF cell

This section provides comprehensive phase-based equations for all conditions of the set state for the RSFQ DFF cell as shown in Fig. 2.12. The DFF cell goes into the set state when an input pulse at **A** is received without an input pulse at **CLK**. When the DFF goes into the set state, the J_1 and J_2 junctions will switch and undergo a 2π phase shift. A fluxon is stored within the J_3-L_3-J_4 loop during the set state. Referring to Fig. E.1,

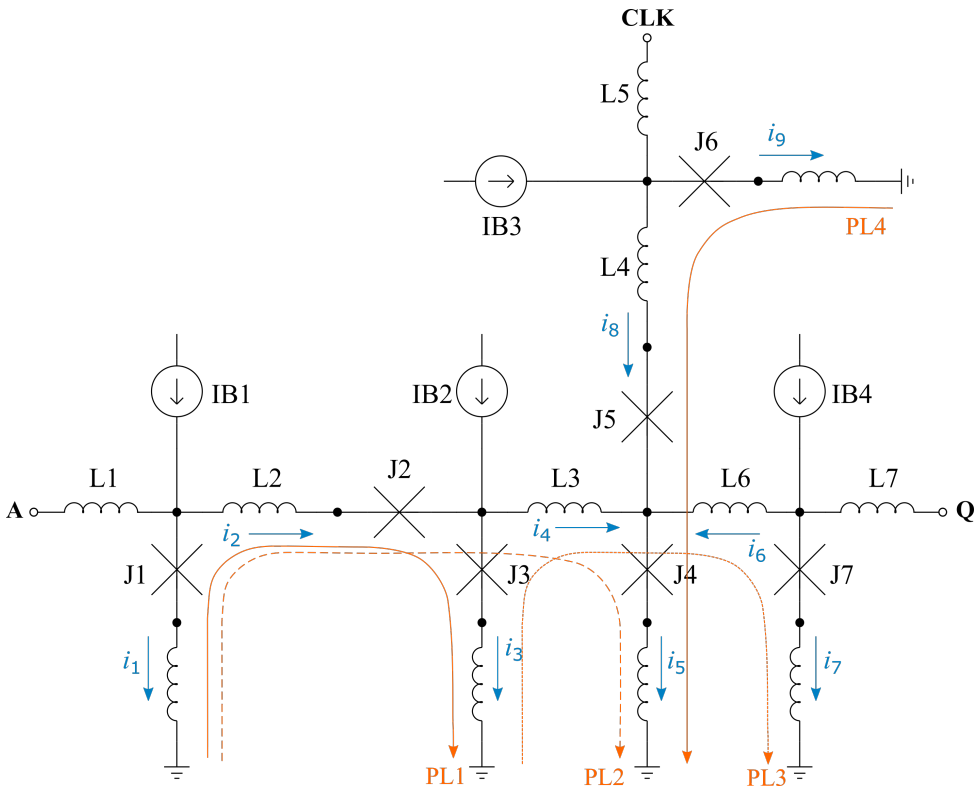

Figure E.1: Phase loops through RSFQ DFF cell.

the phase change through the loop PL1 for the set state is described through

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \tag{E.1}$$

The phase change described in (E.1) can be rewritten to construct the function in (2.39) and is valid for both the reset and set states. The phase through the loop PL2 for the set state is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) = 0 \tag{E.2}$$

The phase change described through (E.2) can be rewritten to construct the function in (2.43). The phase change through the PL3 loop can be expressed as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_6) + \arcsin\left(\frac{i_7}{I_{c7}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p7}i_7) = 0 \tag{E.3}$$

The phase change described through (E.3) can be rewritten to construct the function within (2.44). The phase through the loop PL4 is depicted through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p6}i_9) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_8) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) = 0 \tag{E.4}$$

The phase change described in (E.4) can be rewritten to construct the function in (2.42) and is valid for both the reset and set states.

RSFQ OR2 cell

This section provides comprehensive phase-based equations for all conditions of the set state for the RSFQ OR2 cell as shown in Fig. 2.15. The OR2 cell goes into the set state under three conditions:

1. An input pulse at **A** is received without an input pulse at **CLK**,
2. An input pulse at **B** is received without an input pulse at **CLK**, or
3. Input pulses at both **A** and **B** are received without an input pulse at **CLK**.

Condition 1: Input at A

If there is an input pulse at **A**, then junctions J_1, J_2, J_6 and J_8 will switch and undergo a 2π phase shift.

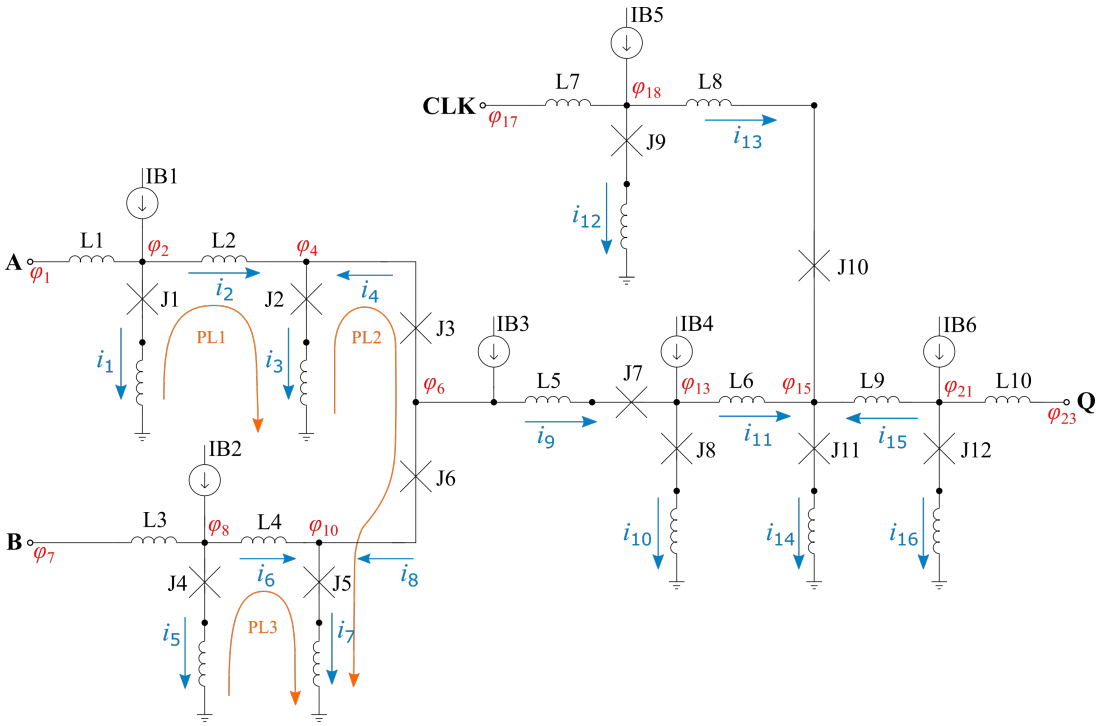

Figure E.2: Phase loops through RSFQ OR2 cell: Part 1.

Referring to Fig. E.2, the phase change through loop PL1 can be described as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 2\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0 \tag{E.5}$$

The phase over J1 is taken as a negative 2π phase shift within (E.5) as the phase shift is in the opposite direction as the loop direction. The phase over J2 is a positive 2π phase shift within (E.5) as loop direction enters the same side of the JJ as the defined current

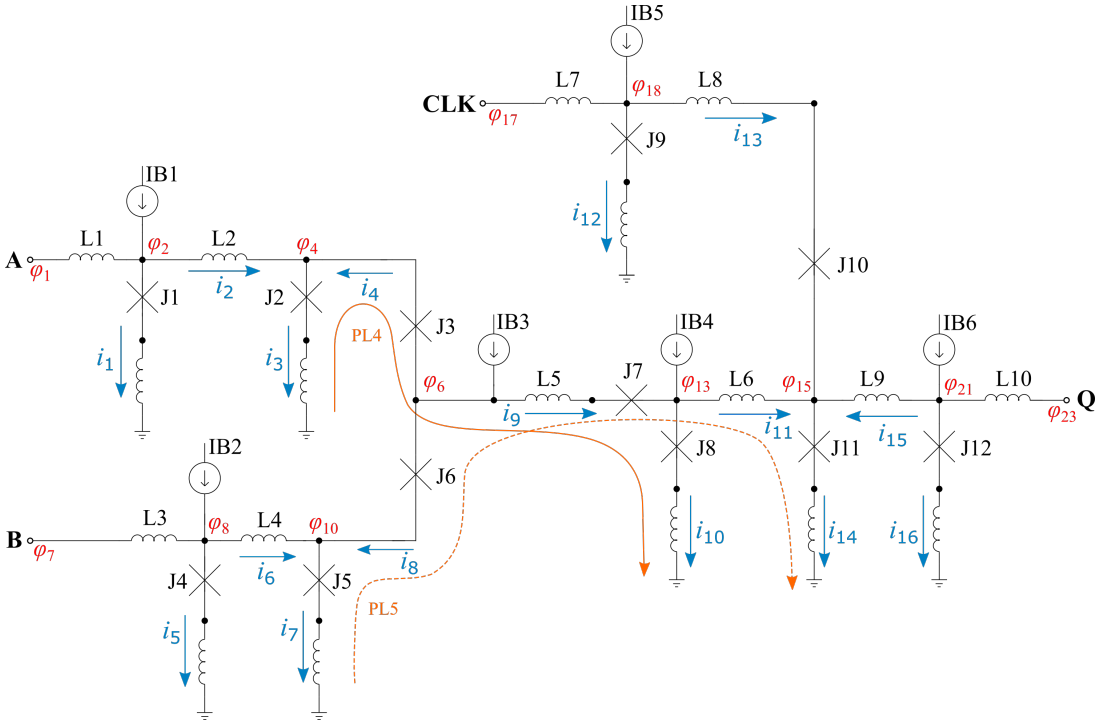

Figure E.3: Phase loops through RSFQ OR2 cell: Part 2.

flow within the JJ. (2.54) is therefore an equivalent function to (E.5). Considering the phase change through loop PL2:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \arcsin\left(\frac{i_8}{I_{c6}}\right) + 2\pi + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.6}$$

The 2π phase shifts within (E.6) cancel out which leads to the function described in (2.55). The phase change through loop PL3 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_6) + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.7}$$

It is found that (E.7) can be represented by the function constructed in (2.56). Analysing the phase change through loop PL4 in Fig. E.3:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{10}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{10}) = 0 \tag{E.8}$$

The 2π phase shifts within (E.8) cancel out due to the differing orientations of the phase shifts. (E.8) can therefore be written as an equivalent function to (2.57). The phase

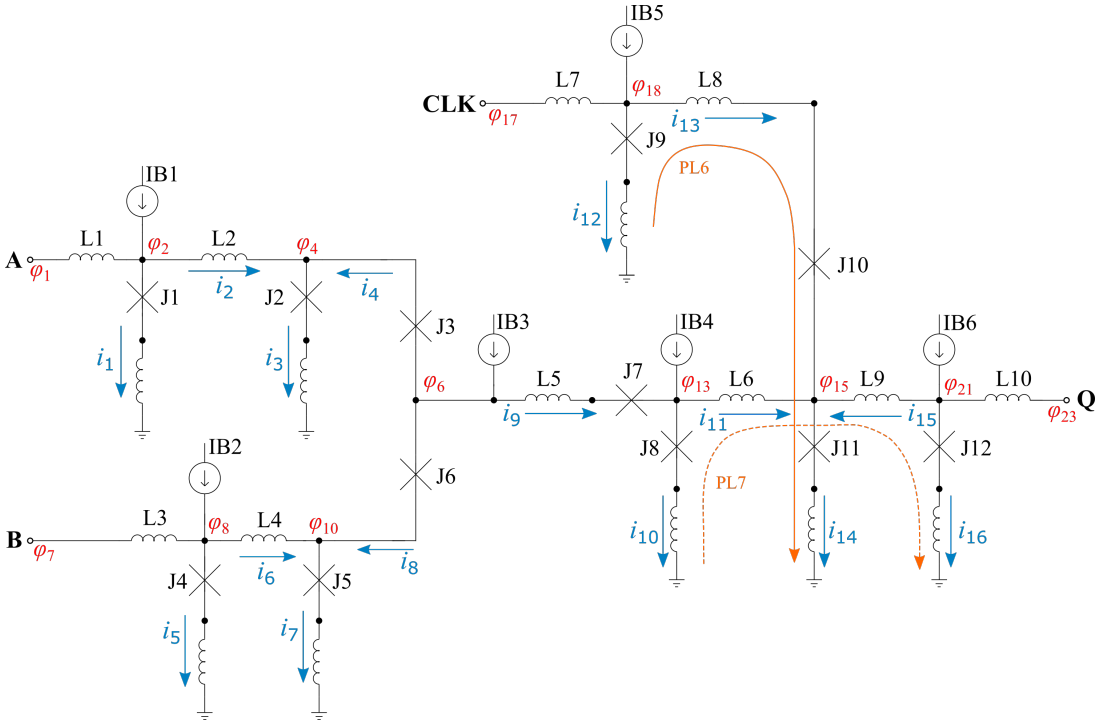

Figure E.4: Phase loops through RSFQ OR2 cell: Part 3.

change through loop PL5 is now analysed:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_7) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - \arcsin\left(\frac{i_8}{I_{c6}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.9}$$

Arranging (E.9) in terms of a function leads to (2.61). The phase change through loop PL6 in Fig. E.4 can be evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{12}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{13}) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.10}$$

It is found that rewriting (E.10) in terms of a function is equivalent to (2.59). The phase change through loop PL7 can be written as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c12}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p12}i_{16}) = 0 \tag{E.11}$$

Rewriting (E.11) in terms of a function leads to (2.62).

Condition 2: Input at B

If there is an input pulse at **B**, then junctions J_4, J_5, J_3 and J_8 will switch and undergo a 2π phase shift. Referring to Fig. E.2, the phase change through loop PL1 for the second condition can be described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_3}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0 \tag{E.12}$$

Writing (E.12) in terms of a function leads to (2.54). Considering the phase change through loop PL2:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \arcsin\left(\frac{i_8}{I_{c6}}\right) + 2\pi + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.13}$$

The 2π phase shifts within (E.13) cancel out leading to the function characterised in (2.55). The phase change through loop PL3 is represented through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_6) + 2\pi + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.14}$$

The 2π phase shifts within (E.14) balances out leading to the function expressed in (2.56). Analysing the phase change through loop PL4 in Fig. E.3:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{10}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{10}) = 0 \tag{E.15}$$

The 2π phase shifts within (E.15) are neutralised due to the differing orientations of the phase shifts. (E.15) can therefore be written as an equivalent function to (2.57). Analysing the phase change through loop PL5 leads to:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_7) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - 2\pi - \arcsin\left(\frac{i_8}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.16}$$

Arranging (E.16) in terms of a function leads to (2.61). The phase change through loop PL6 in Fig. E.4 can be evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{12}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{13}) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.17}$$

Characterising (E.17) in terms of a function leads to (2.59). The phase change through loop PL7 can be written as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c12}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p12}i_{16}) = 0 \tag{E.18}$$

Rewriting (E.18) in terms of a function leads to (2.62).

Condition 3: Input at A and B

If there is an input pulse at **A** and **B**, then junctions J_1, J_2, J_3, J_4, J_5, J_6, J_7 and J_8 will switch and undergo a 2π phase shift. Referring to Fig. E.2, the phase change through loop PL1 for the third condition can be described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 2\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0 \tag{E.19}$$

Writing (E.19) in terms of a function leads to (2.54). Considering the phase change through loop PL2:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \arcsin\left(\frac{i_8}{I_{c6}}\right) + 2\pi + 2\pi + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.20}$$

The 2π phase shifts within (E.20) cancel out leading to the function characterised in (2.55). The phase change through loop PL3 is represented through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_6) + 2\pi + \arcsin\left(\frac{i_7}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_7) = 0 \tag{E.21}$$

The 2π phase shifts within (E.21) balances out leading to the function expressed in (2.56). Analysing the phase change through loop PL4 in Fig. E.3:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + 2\pi + \arcsin\left(\frac{i_9}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{10}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{10}) = 0 \tag{E.22}$$

The 2π phase shifts within (E.22) are neutralised due to the differing orientations of the phase shifts. (E.22) can therefore be written as an equivalent function to (2.57). Analysing the phase change through loop PL5 leads to:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_7) - \arcsin\left(\frac{i_7}{I_{c5}}\right) - 2\pi - \arcsin\left(\frac{i_8}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_9) + 2\pi + \arcsin\left(\frac{i_9}{I_{c7}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.23}$$

Arranging (E.23)) in terms of a function leads to (2.61). The phase change through loop PL6 in Fig. E.4 can be evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{12}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{13}) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \arcsin\left(\frac{i_{14}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{14}) = 0 \tag{E.24}$$

Characterising (E.24) in terms of a function leads to (2.59). The phase change through loop PL7 can be written as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{11}) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c12}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p12}i_{16}) = 0 \tag{E.25}$$

Rewriting (E.25) in terms of a function leads to (2.62).

RSFQ XOR cell

This section provides comprehensive phase-based equations for all conditions of the set state for the RSFQ XOR cell as shown in Fig. 2.21. The XOR cell has two set states:

Set A: An input pulse at **A** is received without an input pulse at **B** or **CLK**.

Set B: An input pulse at **B** is received without an input pulse at **A** or **CLK**.

Set A state – Single input pulse

If there is an input pulse at **A**, then junctions J_1 and J_2 will switch and undergo a 2π phase shift. A fluxon is then stored within the J_2-J_3-J_7-J_{10} loop. The phase change loops which are analysed for the XOR cell are illustrated within Fig. E.5 and E.6. The equation describing the phase change through the PL1 loop is as follows:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 2\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0 \tag{E.26}$$

Rewriting (E.26) leads to the function described in (2.73). This function for the phase change through PL1 is therefore valid for both the reset and set states. The phase change through loop PL2 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0 \tag{E.27}$$

Rewriting (E.27) leads to the function described in (2.74). This function for the phase change through PL2 is therefore valid for both the reset and set states. The phase change through loop PL3 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0 \tag{E.28}$$

Rewriting (E.28) leads to the function described in (2.79). The phase change through loop PL4 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0 \tag{E.29}$$

Rewriting (E.29) leads to the function described in (2.80). The phase change through loop PL5 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{16}) = 0 \tag{E.30}$$

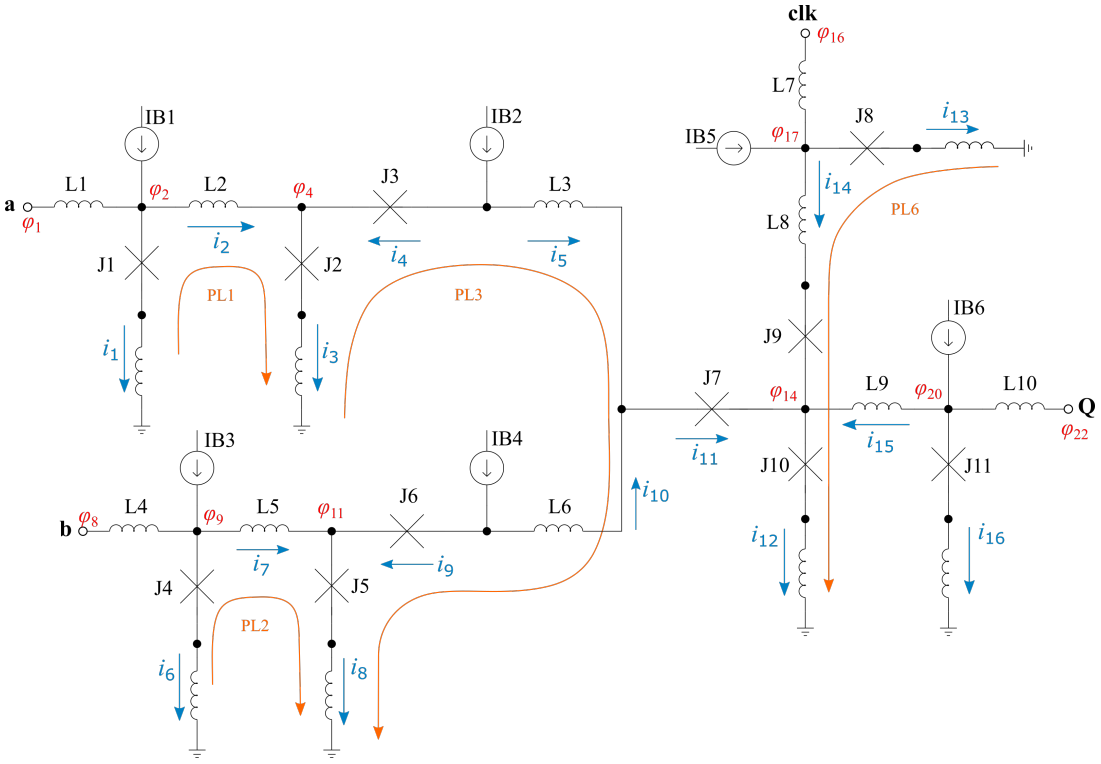

Figure E.5: Phase loops through RSFQ XOR cell: Part 1.

Rewriting (E.30) leads to the function described in (2.77). This function for the phase change through PL5 is therefore valid for both the reset and set states. The phase change through loop PL6 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0 \tag{E.31}$$

Rewriting (E.31) leads to the function described in (2.78). This function for the phase change through PL5 is therefore valid for both the reset and set states.

Set A state – Multiple input pulses

Multiple input pulses at **A** leads to additional JJs switching within the XOR cell. If a fluxon is already stored within the J_2-J_3-J_7-J_{10} loop and an additional pulse is received at **A**, then junctions J_1, J_2, J_6 and J_7 will switch and undergo a 2π phase shift. Referring to Fig. E.5, the phase change through PL1 for multiple input pulses at **a** is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 4\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 4\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0 \tag{E.32}$$

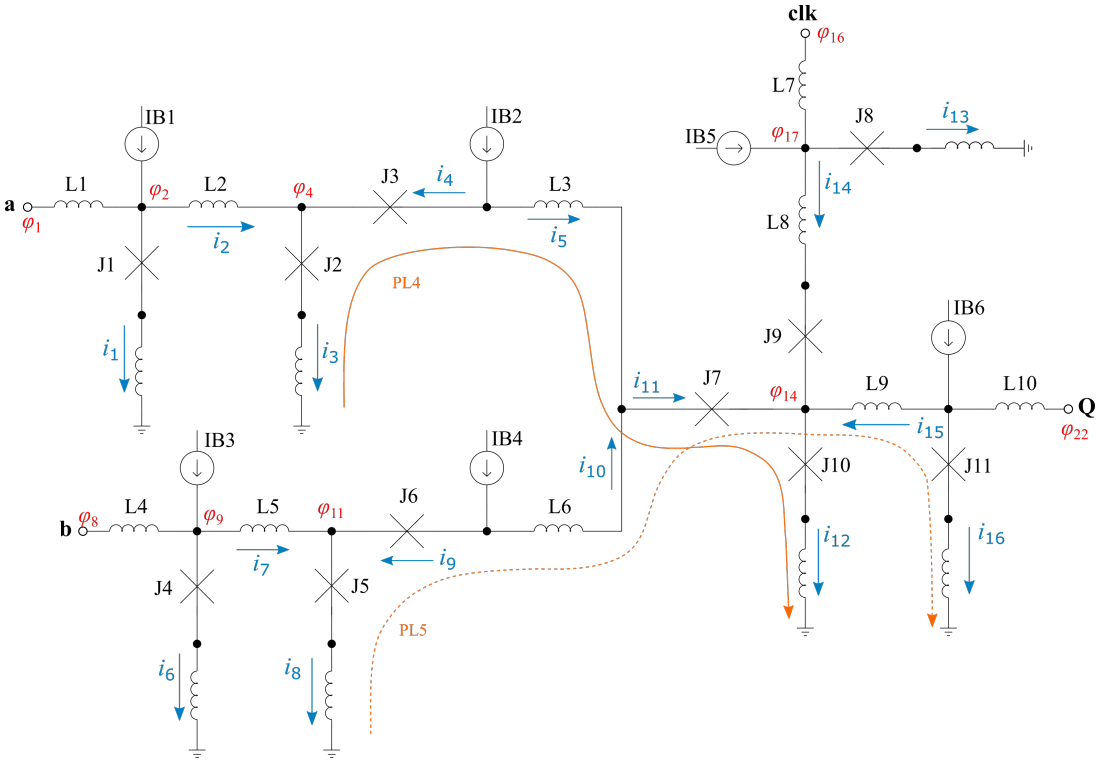

Figure E.6: Phase loops through RSFQ XOR cell: Part 2.

Rewriting (E.32) reverts to the phase change described in (E.26). The phase change through the PL2 loop is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0 \tag{E.33}$$

The phase change described through (E.33) is therefore equal to (E.27) and (2.74). The phase change through loop PL3 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 4\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + 2\pi + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0 \tag{E.34}$$

Rewriting (E.34) leads to the same phase change described in (E.28). The phase change through PL4 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 4\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0 \tag{E.35}$$

Rewriting (E.35) leads to the same phase change described in (E.29). The phase change through PL5 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + 2\pi \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{16}) = 0\end{aligned} \tag{E.36}$$

The phase change described through (E.36) is therefore equal to (E.30) and (2.77). The phase change through PL6 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.37}$$

The phase change described through (E.37) is therefore equal to (E.31) and the function in (2.78).

Set B state – Single input pulse

If there is an input pulse at **B**, then junctions J_4 and J_5 will switch and undergo a 2π phase shift. A fluxon is then stored within the J_5-J_6-J_7-J_{10} loop. Referring to Fig. E.5, the phase change through PL1 for an input pulse at **b** is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0\end{aligned} \tag{E.38}$$

The phase change described through (E.38) is therefore equal to (2.73). The function described in (2.73) is therefore valid for both conditions for the XOR set state. The phase change through PL2 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + 2\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.39}$$

The phase change described through (E.39) is therefore equal to (2.74). The function described in (2.74) is therefore valid for both conditions for the XOR set state. The phase change through PL3 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + 2\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.40}$$

Rewriting (E.40) leads to (2.81). The phase change through PL4 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.41}$$

The phase change described through (E.41) is therefore equal to (2.76). The function described in (2.76) is therefore valid for both conditions for the XOR set state. The phase change through PL5 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - 2\pi - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11} i_{16}) = 0\end{aligned} \tag{E.42}$$

Rewriting (E.42) leads to (2.82). The phase change through PL6 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10} i_{12}) = 0\end{aligned} \tag{E.43}$$

The phase change described through (E.43) is therefore equal to (2.78). The function described in (2.78) is therefore valid for both conditions for the XOR set state.

Set B state – Multiple input pulses

Multiple input pulses at **B** leads to additional JJs switching within the XOR cell. If a fluxon is already stored within the J_5-J_6-J_7-J_{10} loop and an additional pulse is received at **B**, then junctions J_3, J_4, J_5 and J_7 will switch and undergo a 2π phase shift. Referring to Fig. E.5, the phase change through PL1 for multiple input pulses at **b** is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_3}{I_{c2}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2} i_3) = 0\end{aligned} \tag{E.44}$$

Rewriting (E.44) leads to (E.38). The phase change through loop PL2 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 4\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + 4\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5} i_8) = 0\end{aligned} \tag{E.45}$$

The function described in (E.45) is therefore equal to (E.39). The phase change through loop PL3 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + 4\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5} i_8) = 0\end{aligned} \tag{E.46}$$

Rewriting (E.46) leads to (E.40). The phase change through loop PL4 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \arcsin\left(\frac{i_4}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) + 2\pi \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10} i_{12}) = 0\end{aligned} \tag{E.47}$$

The function in (E.47) can be rewritten as (E.41). The phase change through loop PL5 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - 4\pi - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + 2\pi \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{16}) = 0\end{aligned} \tag{E.48}$$

Rewriting (E.48) leads to (E.42). The phase change through loop PL6 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.49}$$

The function described through (E.49) is therefore equal to (E.43).

Reset state – Input pulse at A and B

The XOR cell transitions from the set to reset state when input pulses from both **a** and **b** are present before the arrival of a clock input at **clk**. Junctions J_1 and J_2 will switch and undergo a 2π phase shift when a pulse arrives at **a**. Similarly J_4 and J_5 will switch when a pulse arrives at **b**. Junction J_7 will switch when input pulses arrived at both **a** and **b** before a clock pulse. The phase change through PL1 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 2\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0\end{aligned} \tag{E.50}$$

The function in (E.50) is equal to (E.26) and can be rewritten as (2.73). The phase change through PL2 can be written as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + 2\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.51}$$

Rewriting (E.51) leads to the function described in (2.74). The phase change described in PL3 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + \arcsin\left(\frac{i_9}{I_{c6}}\right) + 2\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.52}$$

Rewriting (E.52) leads to the function described in (2.75). The phase change through PL4 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.53}$$

Rewriting (E.53) leads to the function described in (2.76). The phase change described in PL5 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - 2\pi - \arcsin\left(\frac{i_9}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) \\ + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{16}) = 0\end{aligned} \tag{E.54}$$

It is seen that (E.54) leads to the function in (2.77). The phase change through PL6 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.55}$$

Rewriting (E.55) yields the function described in (2.78).

Reset state – Input pulse at A and CLK

The XOR cell transitions from the set to the reset state when a clock input signal arrives at **clk** after an input is received at either **a** or **b**. For this analysis, the phase equations for this transition is evaluated for a pulse received at **a**. The phase change through PL1 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + 2\pi + \arcsin\left(\frac{i_3}{I_{c2}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) = 0\end{aligned} \tag{E.56}$$

The phase change described in (E.56) can be rewritten to yield (2.73). The phase change through PL2 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_8}{I_{c5}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.57}$$

Rewriting (E.57) leads to the function described in (2.74). The phase change through the PL3 loop is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) + 2\pi + \arcsin\left(\frac{i_9}{I_{c6}}\right) + \arcsin\left(\frac{i_8}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_8) = 0\end{aligned} \tag{E.58}$$

The phase change described through (E.57) can be rewritten to construct the function in (2.74). The phase change through PL4 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_5) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.59}$$

The phase change described in (E.59) can be rewritten to yield (2.76). The phase change through PL5 is now evaluated as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_8) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \arcsin\left(\frac{i_9}{I_{c6}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_{10}) \\ + \arcsin\left(\frac{i_{11}}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{15}) + 2\pi + \arcsin\left(\frac{i_{16}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{16}) = 0\end{aligned} \tag{E.60}$$

Rewriting (E.60) leads to the function described in (2.77). The phase change through the PL6 loop is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p8}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c9}}\right) \\ + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{12}) = 0\end{aligned} \tag{E.61}$$

The phase changed described in (E.61) can be rewritten to construct the function in (2.78).

RSFQ AND2 cell

This section provides comprehensive phase-based equations for all conditions of the set state for the RSFQ AND2 cell as shown in Fig. 2.29. The AND2 cell has three set states:

Set A: An input pulse at **A** is received without an input pulse at **B** or **CLK**.

Set B: An input pulse at **B** is received without an input pulse at **A** or **CLK**.

Set AB: Input pulses at **A** and **B** are received without an input pulse at **CLK**.

Set A - Input pulse at A

The AND2 cell transitions to the set state A state when an input signal is received at **a**. The input at **a** causes junctions J_1 and J_3 to switch and undergo a 2π phase shift. Fig. E.7 shows how the phase loops PL1 to PL5 are defined for the AND2 cell. The phase

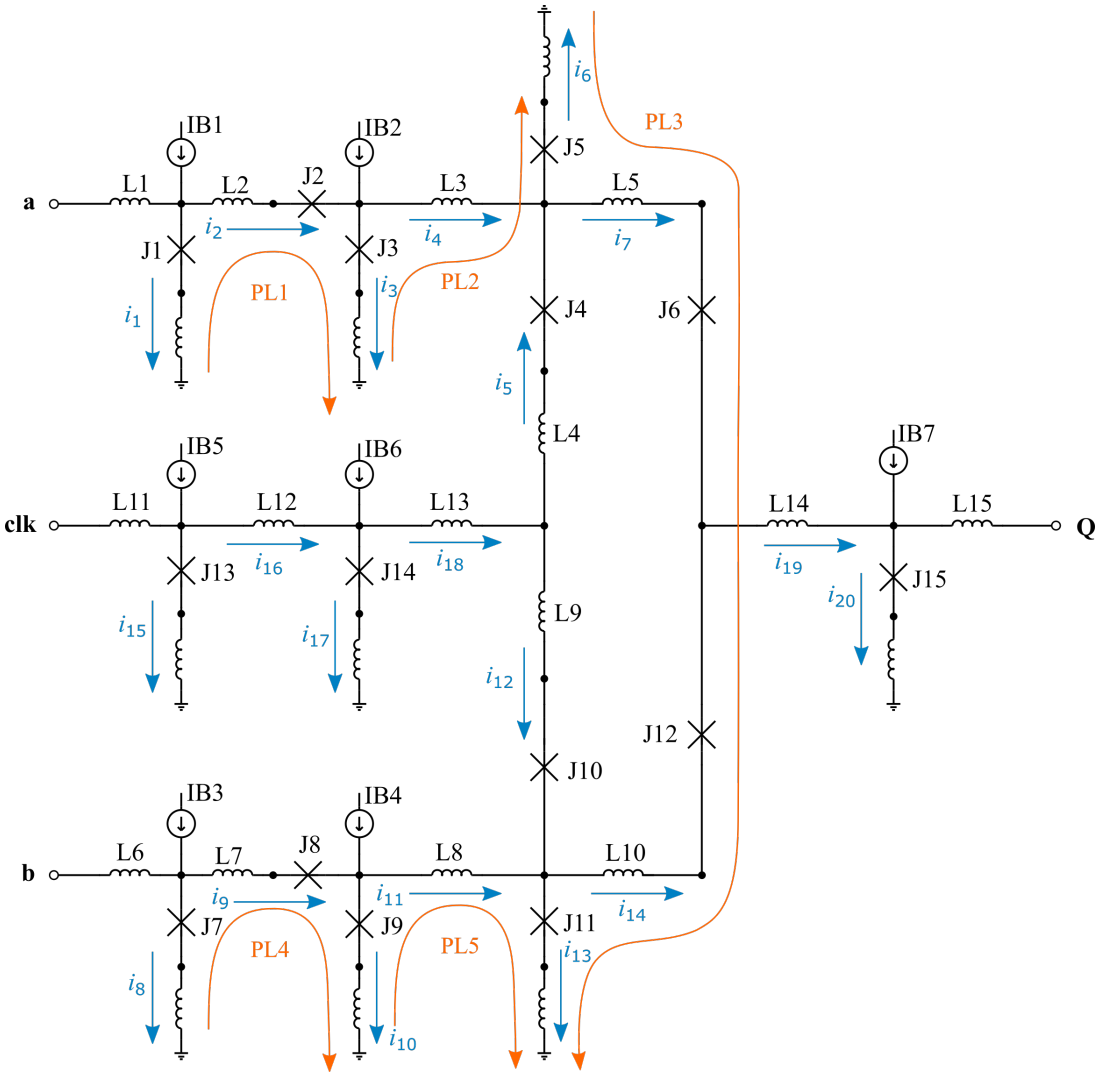

Figure E.7: Phase loops through RSFQ AND2 cell: Part 1.

change through PL1 can be evaluated as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \tag{E.62}$$

The phase change described in (E.62) can be rewritten to construct the function in (2.94). The phase change through PL2 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0 \tag{E.63}$$

Rewriting (E.63) leads to the function described through (2.103). The phase change through PL3 is now evaluated as:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_7}{I_{c6}}\right) - \arcsin\left(\frac{i_{14}}{I_{c12}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.64}$$

The equation in (E.64) can be rewritten to yield the function in (2.96). Evaluating the phase change through PL4 leads to:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p7}i_8) - \arcsin\left(\frac{i_8}{I_{c7}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \arcsin\left(\frac{i_9}{I_{c8}}\right) + \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9}i_{10}) = 0 \tag{E.65}$$

The phase change described in (E.65) can be rewritten to form (2.97). The phase change through PL5 can be described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{11}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.66}$$

Rewriting (E.66) yields the function described through (2.98). The definitions of the phase loops PL6 and PL7 are found in Fig. E.8. The phase change through the PL6 loop is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.67}$$

The equation in (E.67) can be rewritten to form the function in (2.99). Evaluating the phase change through PL7 yields:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p13}i_{15}) - \arcsin\left(\frac{i_{15}}{I_{c13}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{12}i_{16}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0 \tag{E.68}$$

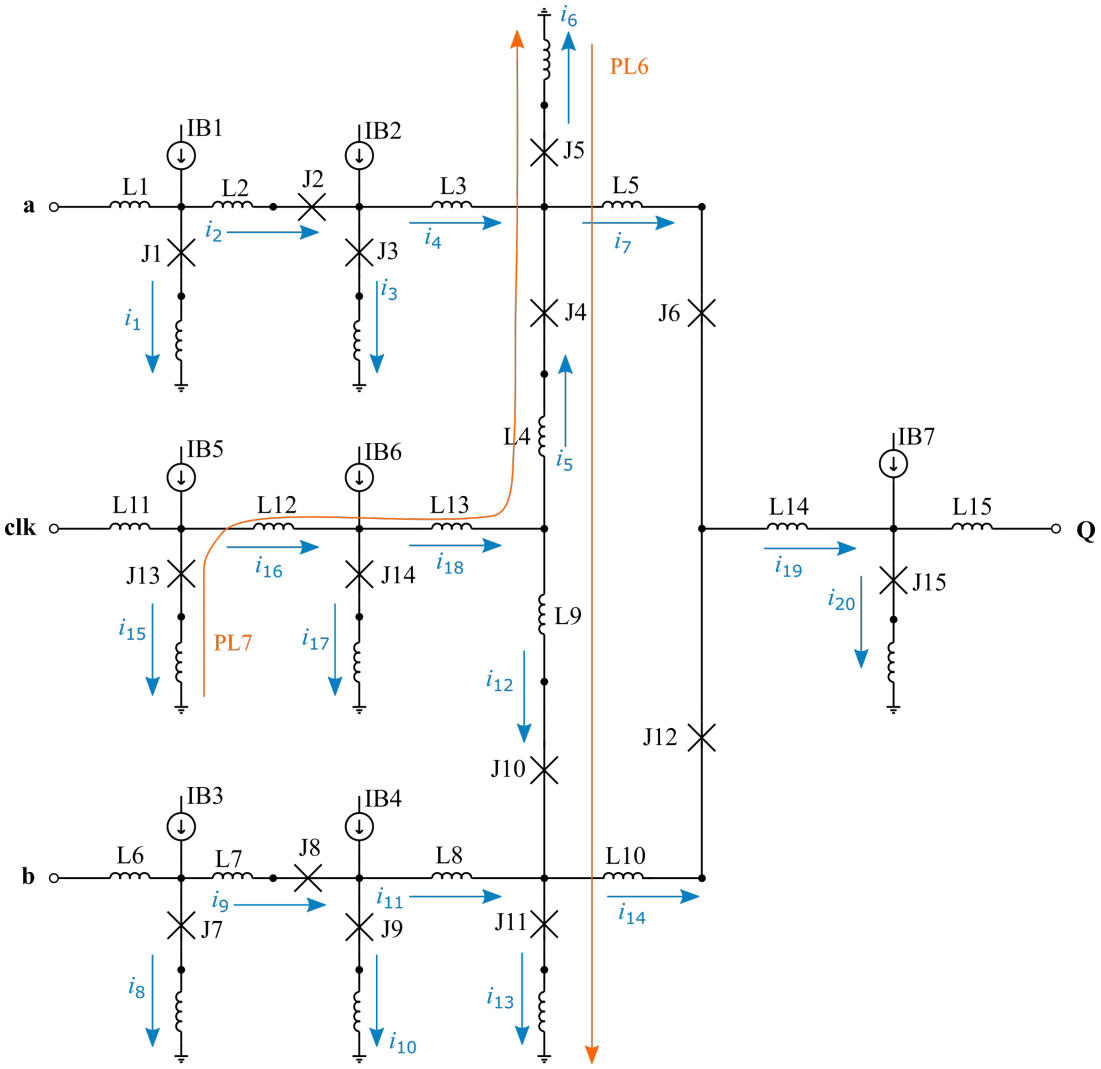

Figure E.8: Phase loops through RSFQ AND2 cell: Part 2.

Rewriting (E.68) leads to the function described through (2.100). Fig. E.9 shows the definitions of the PL8 and PL9 phase loops. The phase change through the PL8 loop is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p14}i_{17}) - \arcsin\left(\frac{i_{17}}{I_{c14}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.69}$$

The phase change described in (E.69) can be rewritten to construct (2.101). The phase change through PL9 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p11}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c12}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{14}i_{19}) + \arcsin\left(\frac{i_{20}}{I_{c15}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p15}i_{20}) = 0\end{aligned} \tag{E.70}$$

The equation in (E.70) can be rewritten to yield the function described in (2.102).

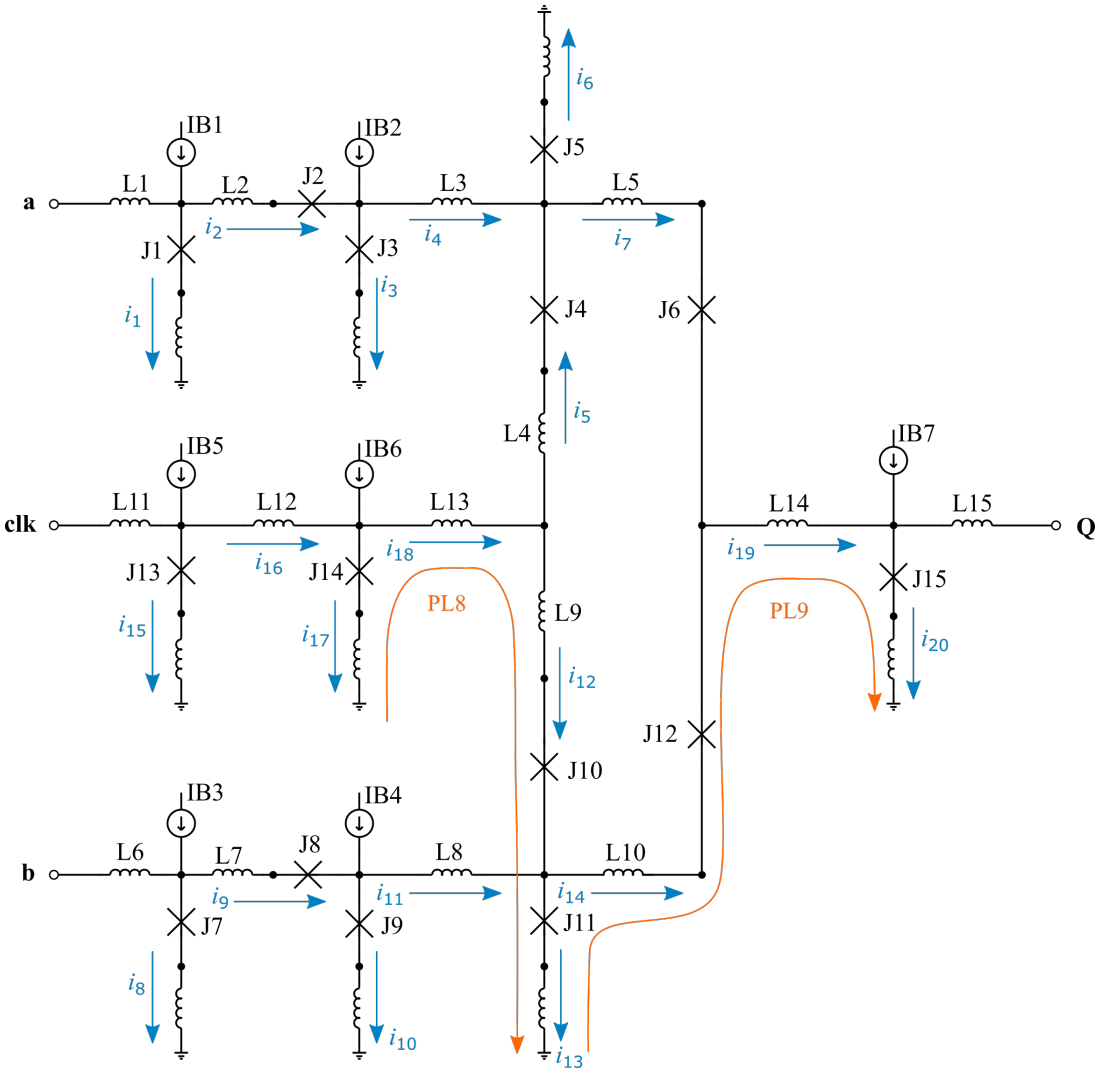

Figure E.9: Phase loops through RSFQ AND2 cell: Part 3.

Set B - Input pulse at B

The AND2 cell transitions to the set B state when an input pulse is received at **b**. The pulse at **b** causes J_7 and J_9 to switch and undergo a 2π phase shift. The phase change through the PL1 loop within the set B state is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \tag{E.71}$$

The phase change described in (E.71) can be rewritten to form (2.94). The phase change through PL2 is evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0 \tag{E.72}$$

The equation in (E.72) can be rewritten to yield the function in (2.95). The phase change through the PL3 loop can be described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_7}{I_{c6}}\right) - \arcsin\left(\frac{i_{14}}{I_{c12}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.73}$$

Rewriting (E.73) yields (2.96). The phase change through PL4 is evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p7}i_8) - \arcsin\left(\frac{i_8}{I_{c7}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \arcsin\left(\frac{i_9}{I_{c8}}\right) + 2\pi + \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9}i_{10}) = 0 \tag{E.74}$$

The equation in (E.74) can be rewritten to construct (2.97). Evaluating the phase change through PL5 yields:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c9}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{11}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.75}$$

Rewriting (E.75) leads to the function described in (2.104). The phase change through PL6 is described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0 \tag{E.76}$$

The phase change described in (E.76) can be rewritten to yield (2.99). The phase change through PL7 can be described as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p13}i_{15}) - \arcsin\left(\frac{i_{15}}{I_{c13}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{12}i_{16}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0\end{aligned} \tag{E.77}$$

Rewriting (E.77) leads to the function described in (2.100). Evaluating the phase change through PL8 yields:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p14}i_{17}) - \arcsin\left(\frac{i_{17}}{I_{c14}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.78}$$

The equation in (E.78) can be rewritten to form (2.101). Finally, the phase change through PL9 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p11}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c12}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{14}i_{19}) + \arcsin\left(\frac{i_{20}}{I_{c15}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p15}i_{20}) = 0\end{aligned} \tag{E.79}$$

The phase changed in (E.79) can be rewritten to yield (2.102).

Set AB - Input pulse at A and B

The AND2 cell transitions to the set AB state when input pulses are observed at both the **a** and **b** ports. Junctions J_1, J_3, J_7 and J_9 will switch and undergo a 2π phase change under this condition. The phase change through PL1 can be described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \\ + 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0\end{aligned} \tag{E.80}$$

Rewriting (E.80) leads to the function described in (2.94). The function in (2.94) is therefore valid for the reset, set A, set B and set AB states. The phase change through PL2 is evaluated through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \arcsin\left(\frac{i_6}{I_{c5}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0\end{aligned} \tag{E.81}$$

The equation in (E.81) can be rewritten to yield (2.103). The phase change described through (2.103) is therefore valid for both the set A and set AB states. The phase change through PL3 is evaluated as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_7) + \arcsin\left(\frac{i_7}{I_{c6}}\right) \\ - \arcsin\left(\frac{i_{14}}{I_{c12}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.82}$$

Rewriting (E.82) yields the function described through (2.96). The phase change represented through (2.96) is therefore valid for the reset, set A, set B and set AB states. The phase change through PL4 is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p7}i_8) - \arcsin\left(\frac{i_8}{I_{c7}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \arcsin\left(\frac{i_9}{I_{c8}}\right) \\ + 2\pi + \arcsin\left(\frac{i_{10}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9}i_{10}) = 0\end{aligned} \tag{E.83}$$

The equation in (E.83) can be rewritten to form (2.97). The phase change represented through (2.97) is therefore valid for the reset, set A, set B and set AB states. Evaluating the phase change through PL5 yields:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p9}i_{10}) - \arcsin\left(\frac{i_{10}}{I_{c9}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{11}) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.84}$$

Rewriting (E.84) leads to (2.104). The function in (2.104) is therefore valid for both the set B and set AB states. The phase change through loop PL6 can be described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p5}i_6) - \arcsin\left(\frac{i_6}{I_{c5}}\right) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.85}$$

The phase change described in (E.85) can be rewritten to form (2.99). The function in (2.99) is therefore valid for the reset, set A, set B and set AB states. The phase change through the PL7 loop is described through:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p13}i_{15}) - \arcsin\left(\frac{i_{15}}{I_{c13}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{12}i_{16}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \arcsin\left(\frac{i_5}{I_{c4}}\right) + \arcsin\left(\frac{i_6}{I_{c5}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p5}i_6) = 0\end{aligned} \tag{E.86}$$

Rewriting (E.86) yields (2.100). The function in (2.100) is therefore valid for the reset, set A, set B and set AB states. The phase change through the PL8 loop is evaluated as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p14}i_{17}) - \arcsin\left(\frac{i_{17}}{I_{c14}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{13}i_{18}) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_{12}) \\ + \arcsin\left(\frac{i_{12}}{I_{c10}}\right) + \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{13}) = 0\end{aligned} \tag{E.87}$$

The phase change described through (E.87) can be rewritten to yield (2.101). The function described in (2.101) is therefore valid for the reset, set A, set B and set AB states. Finally, the phase change through PL9 is evaluated as:

$$\begin{aligned}\left(\frac{2\pi}{\Phi_0}\right)(-L_{p11}i_{13}) - \arcsin\left(\frac{i_{13}}{I_{c11}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{14}) + \arcsin\left(\frac{i_{14}}{I_{c12}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{14}i_{19}) + \arcsin\left(\frac{i_{20}}{I_{c15}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p15}i_{20}) = 0\end{aligned} \tag{E.88}$$

The phase change described through (E.88) can be rewritten to yield (2.102). The function in (2.102) is therefore valid for the reset, set A, set B and set AB states.

RSFQ NOT cell

This section provides comprehensive phase-based equations for all conditions of the start-up, set and reset states for the RSFQ NOT cell as shown in Fig. 2.33. The NOT cell is analysed for the following states:

Set state – Single input: The set state when a single input is received at the **a** port.

Set to Reset state: The transition from the set state to the reset state. An input pulse is received at the **a** port followed by an input pulse at **clk** to reset the circuit.

Reset state – Single input: A single input is received at the **clk** port when the circuit is in the reset state.

Set state – Single input at A

The NOT cell transitions into the set state when an input pulse arrives at **a**. The input pulse causes junctions J_1, J_2 and J_7 to switch and undergo a 2π phase shift. The phase loops PL1 to PL3 are defined within Fig. E.10. The phase change through the PL1 loop

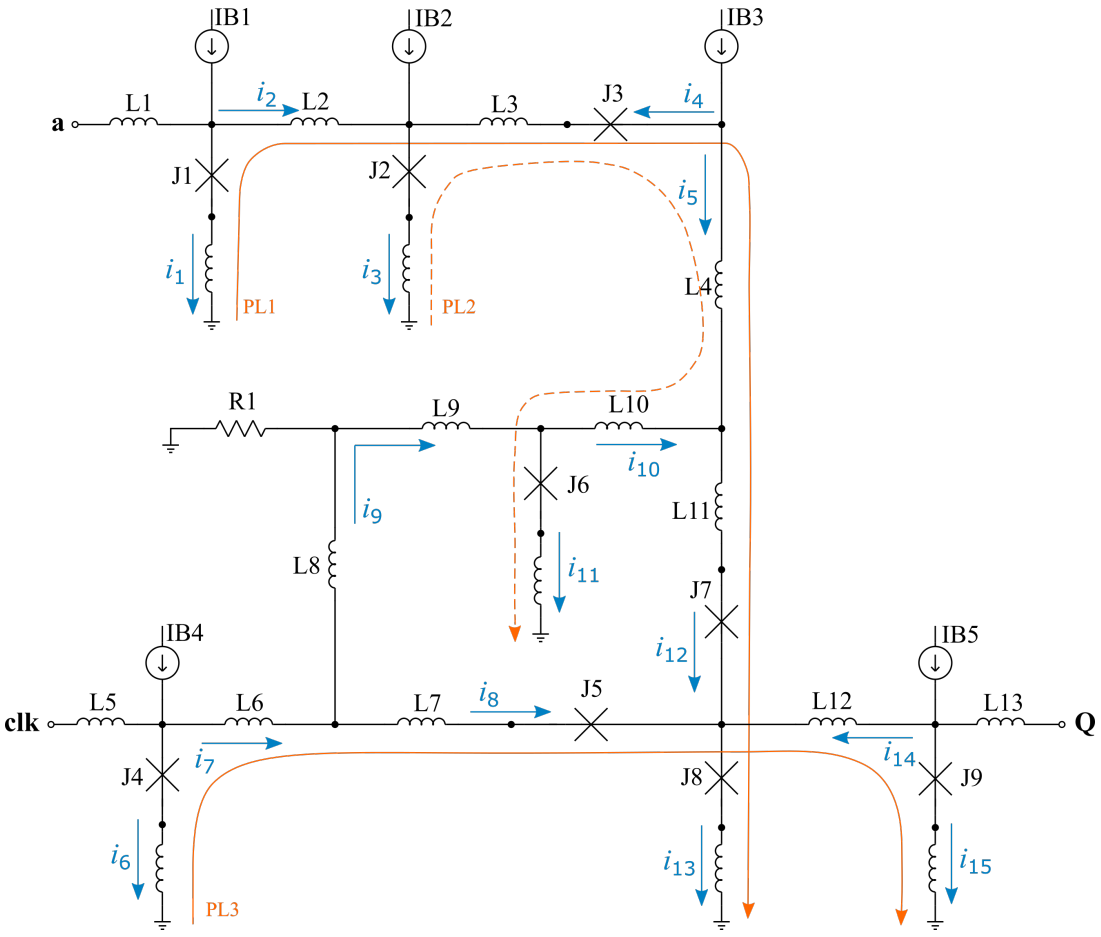

Figure E.10: Phase loops through RSFQ NOT cell: Part 1.

is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) - \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{13}) = 0 \tag{E.89}$$

Rewriting (E.89) leads to (2.114). The function described in (2.114) is therefore valid for both the reset and set states. The phase change through PL2 can be evaluated through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) = 0 \tag{E.90}$$

The phase change described in (E.90) can be rewritten to yield (2.120). Evaluating the phase change through PL3 leads to:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_8) + \arcsin\left(\frac{i_8}{I_{c5}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{12}i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9}i_{15}) = 0 \tag{E.91}$$

Rewriting (E.91) yields (2.116). The function describing the phase change in (2.116) is therefore valid for both the reset and set states. Fig. E.11 shows the definitions for the phase loops PL4 and PL5. The phase through the PL4 loop is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_9) + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) = 0 \tag{E.92}$$

The phase change in (E.92) can be rewritten to construct (2.117). The function within (2.117) is thus valid for both the reset and set states. The phase change through PL5 is evaluated through:

$$\left(\frac{2\pi}{\Phi_0}\right)(L_8 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_8) = 0 \tag{E.93}$$

Rewriting (E.93) yields (2.121). Fig. E.12 shows how the phase loop PL6 is defined for the NOT cell. The phase change through PL6 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{13}) = 0 \tag{E.94}$$

The phase change described in (E.94) can be rewritten to yield (2.122).

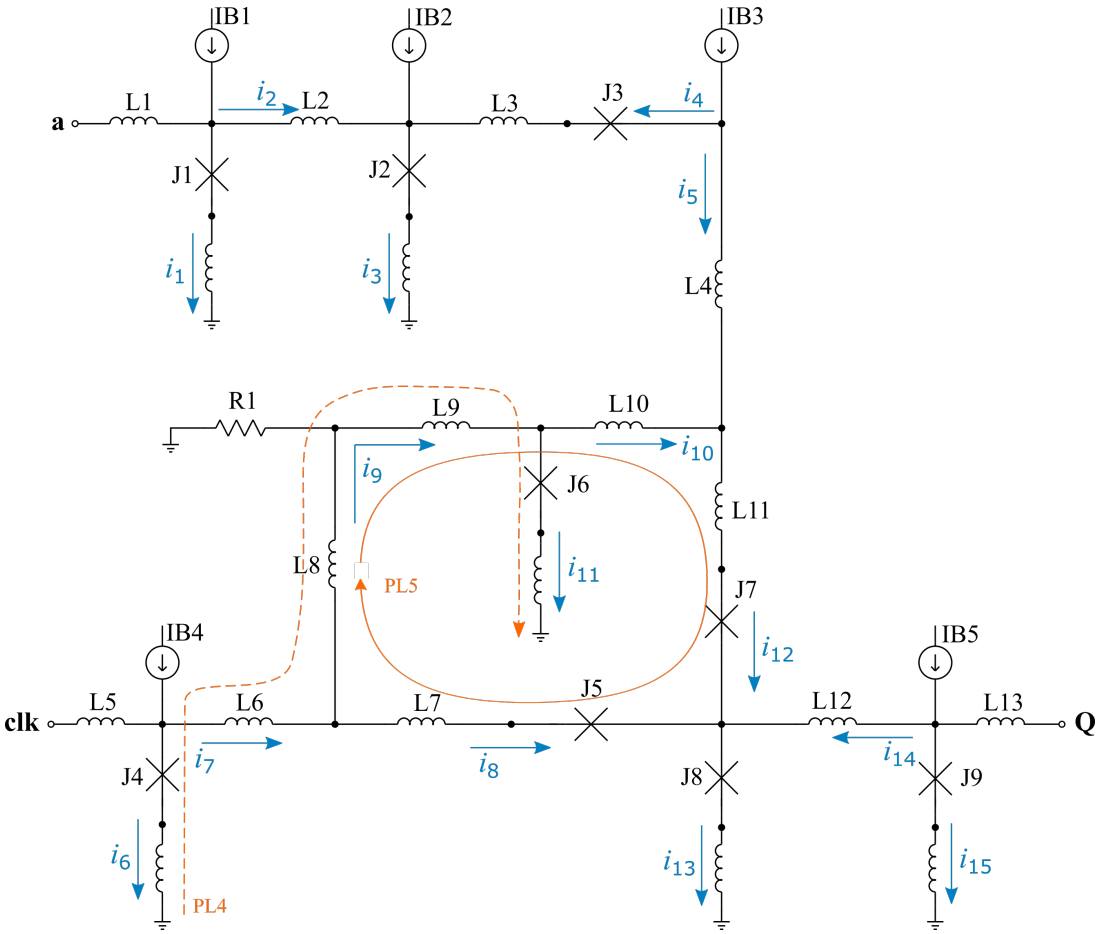

Figure E.11: Phase loops through RSFQ NOT cell: Part 2.

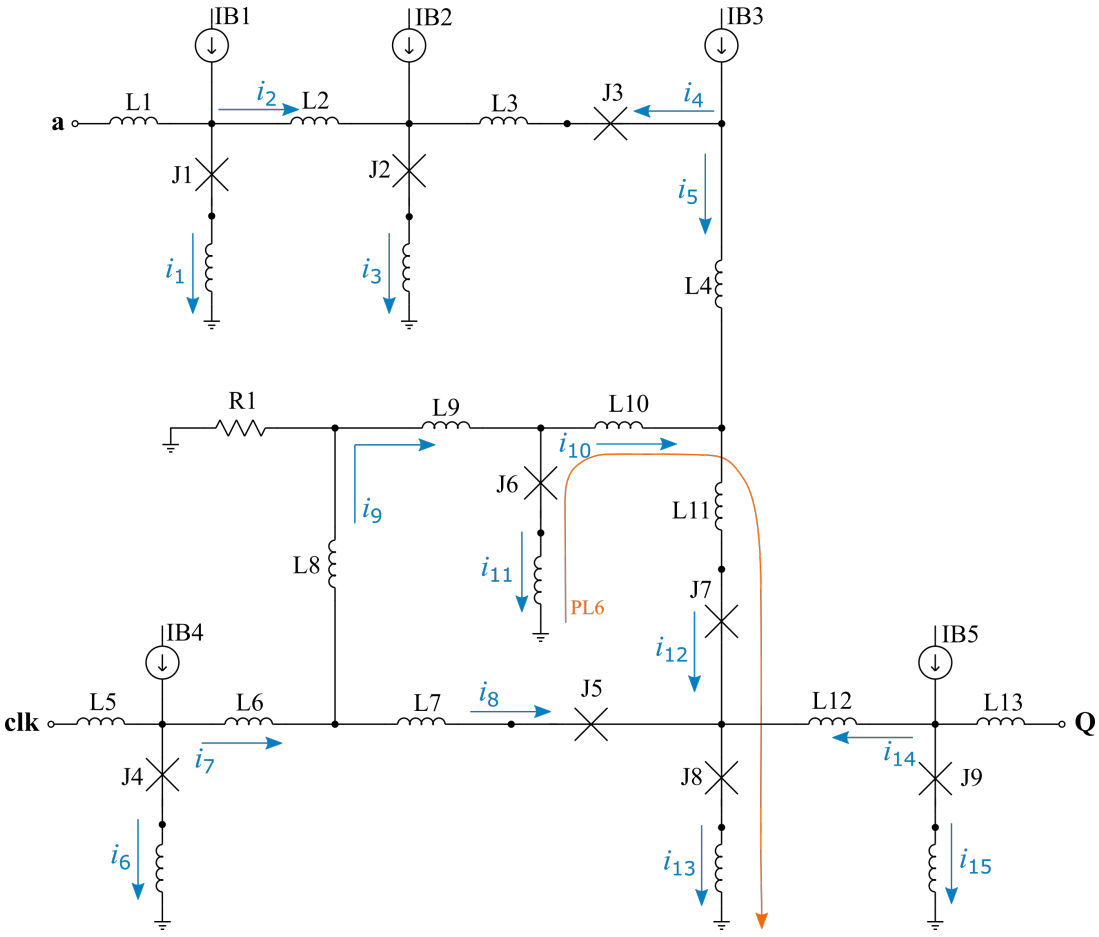

Figure E.12: Phase loops through RSFQ NOT cell: Part 3.

Set to Reset state – Input at A followed by input at CLK

The NOT cell transitions from the set to the reset state when an input signal is received at the **clk** port. The clock pulse causes junctions J_4, J_5 and J_6 to switch and undergo a 2π phase shift. It should be noted that the phase shifts caused by the original input pulse at **a** should also be considered within the equations describing the phase change.

The phase change through PL1 is described through:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) - \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) \\ &- \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11} i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) \\ &\qquad + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8} i_{13}) = 0 \end{aligned} \tag{E.95}$$

Rewriting (E.95) yields (2.114). The function described through (2.114) is thus valid for both the reset and set states. The phase change through PL2 is evaluated through:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - 2\pi - \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \arcsin\left(\frac{i_4}{I_{c3}}\right) \\ &+ \left(\frac{2\pi}{\Phi_0}\right)(L_4 i_5) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10} i_{10}) + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6} i_{11}) = 0 \end{aligned} \tag{E.96}$$

The phase change described in (E.96) can be rewritten to construct (2.115). The phase change through the PL3 loop is described through:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_8) \\ &+ 2\pi + \arcsin\left(\frac{i_8}{I_{c5}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{12} i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9} i_{15}) = 0 \end{aligned} \tag{E.97}$$

The equation in (E.97) can be rewritten to yield (2.116). The function within (2.116) is thus valid for both the reset and set states. Evaluating the phase change through PL4 leads to:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_9) \\ &\qquad + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_9) + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6} i_{11}) = 0 \end{aligned} \tag{E.98}$$

Rewriting (E.98) leads to the function described in (2.117). The phase-based equation in (2.117) is therefore valid for both the reset and set states. The phase change through PL5 can be described through:

$$\begin{aligned} &\left(\frac{2\pi}{\Phi_0}\right)(L_8 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_9 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10} i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11} i_{12}) \\ &\qquad + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - 2\pi - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_8) = 0 \end{aligned} \tag{E.99}$$

Rewriting (E.99) yields the function described in (2.118). The phase change through the PL6 loop is evaluated through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c6}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{13}) = 0 \tag{E.100}$$

The phase change described through (E.100) can be rewritten to construct (2.119).

Reset state – Single input at CLK

The NOT cell generates an output pulse at **Q** if a clock input is received at **clk** when the cell is within the reset state. The input clock pulse causes the junctions J_4, J_6, J_8 and J_9 to switch and undergo a 2π phase shift. The phase change through PL1 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2i_2) - \left(\frac{2\pi}{\Phi_0}\right)(L_3i_4) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4i_5) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{13}) = 0 \tag{E.101}$$

Rewriting (E.101) leads to (2.114). The phase change through PL2 is evaluated as:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p2}i_3) - \arcsin\left(\frac{i_3}{I_{c2}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_3i_4) - 2\pi - \arcsin\left(\frac{i_4}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_4i_5) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) = 0 \tag{E.102}$$

The phase change described in (E.102) can be rewritten to construct (2.120). The phase change through the PL3 loop can be described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_7i_8) + \arcsin\left(\frac{i_8}{I_{c5}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{12}i_{14}) + 2\pi + \arcsin\left(\frac{i_{15}}{I_{c9}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p9}i_{15}) = 0 \tag{E.103}$$

Rewriting (E.103) leads to the function in (2.116). Evaluating the phase change through the PL4 loop yields:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_6) - \arcsin\left(\frac{i_6}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_6i_7) + \left(\frac{2\pi}{\Phi_0}\right)(L_8i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_9i_9) + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) = 0 \tag{E.104}$$

The phase change described in (E.104) can be rewritten to construct (2.117). The phase change through the PL5 loop can be described through:

$$\left(\frac{2\pi}{\Phi_0}\right)(L_8i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_9i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) - \arcsin\left(\frac{i_8}{I_{c5}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7i_8) = 0 \tag{E.105}$$

Rewriting (E.105) leads to the construction of (2.118). Lastly, the phase change through PL6 is evaluated through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c6}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{12}) \\ + \arcsin\left(\frac{i_{12}}{I_{c7}}\right) + 2\pi + \arcsin\left(\frac{i_{13}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{13}) = 0 \end{aligned} \tag{E.106}$$

The phase change described in (E.106) can be rewritten to yield (2.119).

RSFQ NDRO cell

This section provides comprehensive phase-based equations for all conditions of the start-up, set and reset states for the RSFQ NDRO cell as shown in Fig. 2.37. The NDRO cell is analysed for the following states:

Start-up state: The start-up state of the cell when no inputs have been received at the **a**, **b** or **clk** ports.

Reset to Set state: The set state when a single signal input is received at the **a** port.

Set state – Clock input: The set state when a single clock input is received at the **clk** port.

Set to Reset state: The transition from the set state to the reset state. An input pulse is received at the **a** port followed by an input pulse at **b** to reset the circuit.

Reset state – Clock input: A single input is received at the **clk** port when the circuit is in the reset state.

Start-up state

The phase-based equations for the NDRO cell for the start-up state is considered. The start-up state assumes that no input pulses have been received and that no junctions have switched. The phase change loops which are analysed for the NDRO cell are illustrated within Fig. E.13 and E.14. The phase change through the PL1 loop is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \\ + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \end{aligned} \tag{E.107}$$

Rewriting (E.107) leads to the function described in (2.132). The phase change through PL2 is written as:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) \\ + \arcsin\left(\frac{i_7}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) = 0 \end{aligned} \tag{E.108}$$

Rewriting (E.108) leads to the function described in (2.133). The phase change through PL3 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_6) + \arcsin\left(\frac{i_6}{I_{c5}}\right) \\ -\left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) \\ + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \end{aligned} \tag{E.109}$$

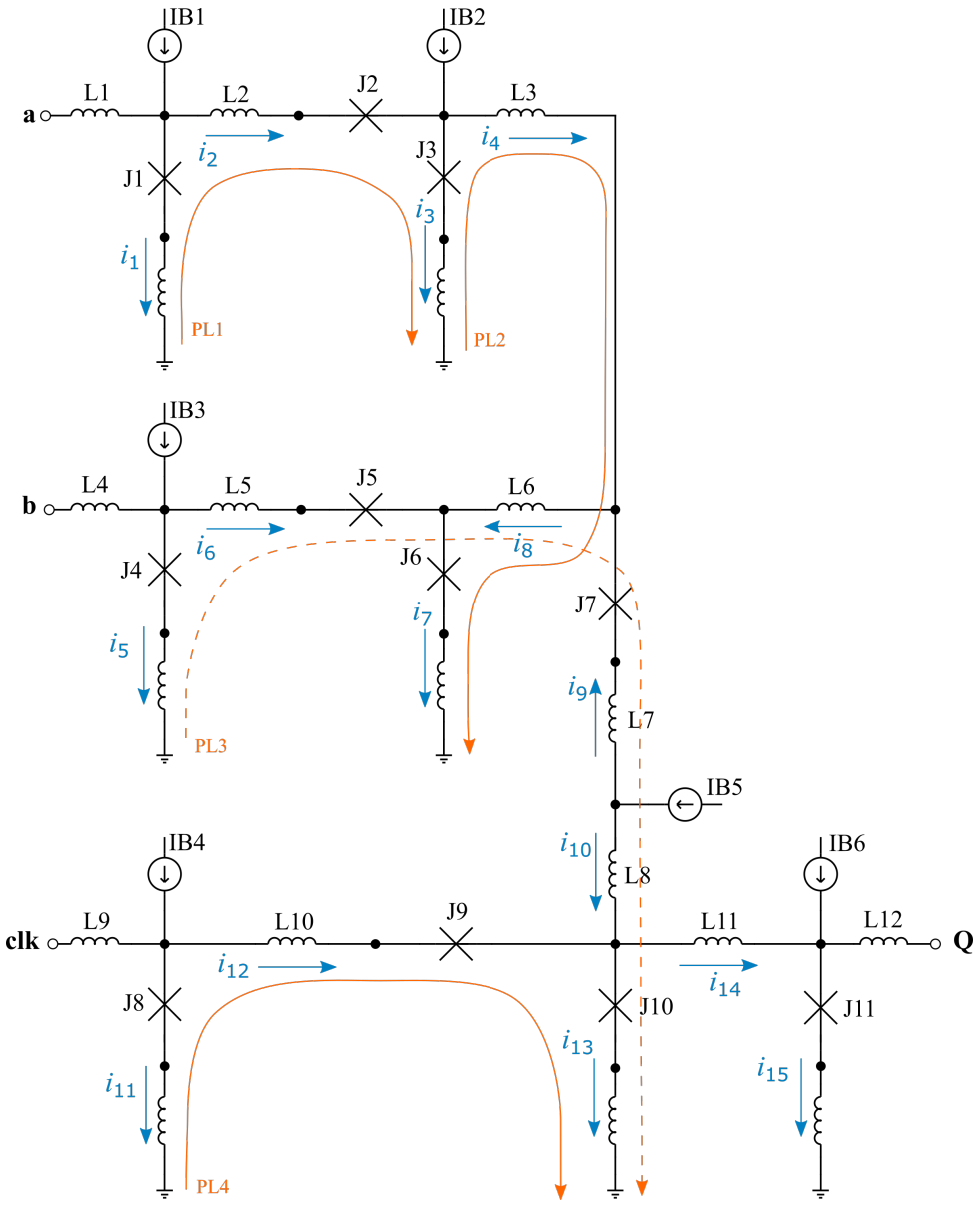

Figure E.13: Phase loops through RSFQ NDRO cell: Part 1.

The function in (E.109) can be rewritten to derive (2.134). The phase change through PL4 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \tag{E.110}$$

Rewriting (E.110) leads to the function described in (2.135). The phase change loops PL5 and PL6 is illustrated in Fig. E.14. The phase change through PL5 can be written

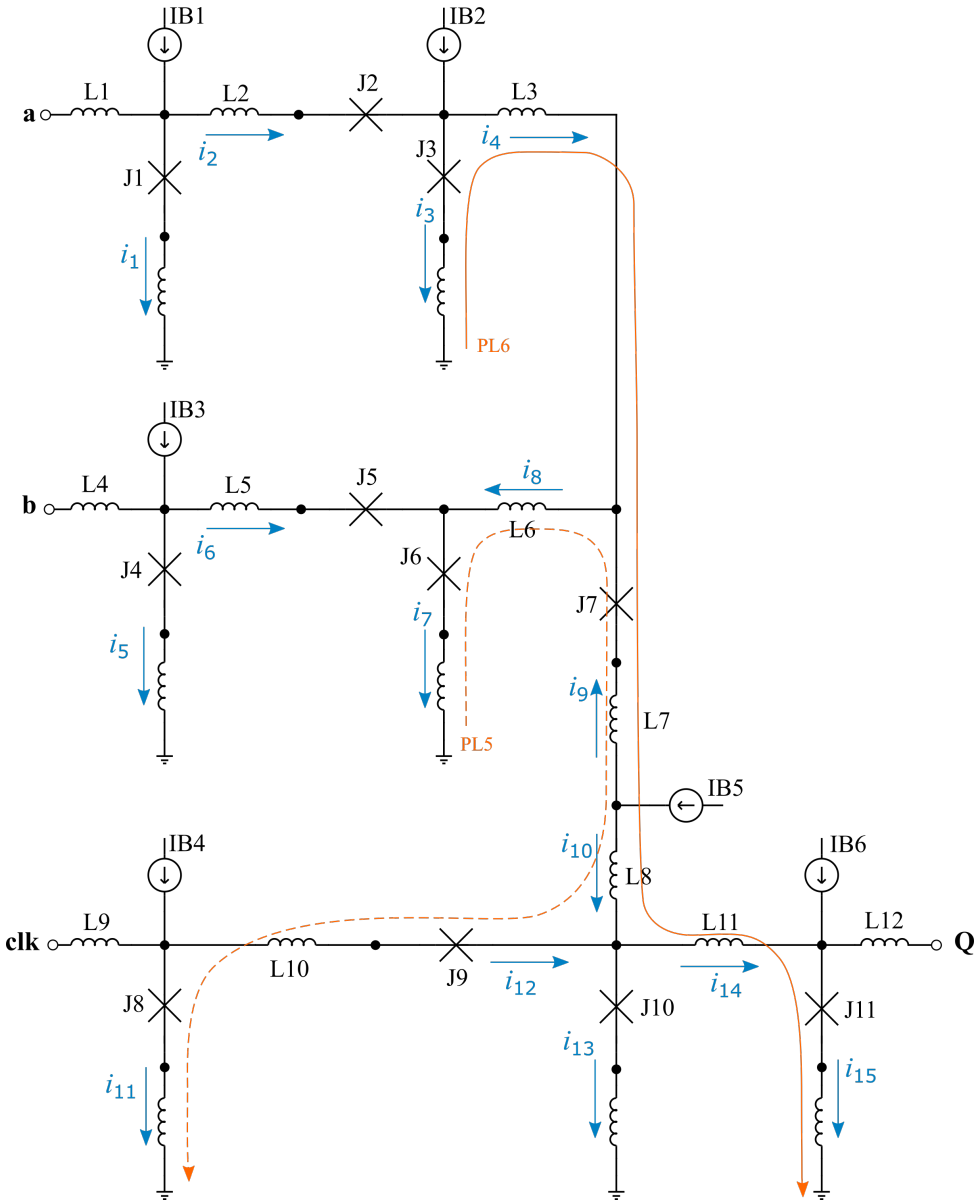

Figure E.14: Phase loops through RSFQ NDRO cell: Part 2.

as:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) - \arcsin\left(\frac{i_7}{I_{c6}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right)$$
$$-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10} i_{12}) \tag{E.111}$$
$$+ \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8} i_{11}) = 0$$

The phase change described in (E.111) can be rewritten to derive the function in (2.136).The phase change through PL6 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \arcsin\left(\frac{i_9}{I_{c7}}\right)$$
$$-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11} i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right) \tag{E.112}$$
$$+ \left(\frac{2\pi}{\Phi_0}\right)(L_{p11} i_{15}) = 0$$

Rewriting (E.112) leads to the function described in (2.137).

Set state – Single input

The NDRO cell goes into the set state when an input is received at **a**. This input pulse causes junctions J_1 and J_3 to switch and undergo a 2π phase shift. The phase change loops PL1 to PL6 for the NDRO within the set state is now discussed. The phase change through the PL1 loop is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right)$$
$$+ 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3} i_3) = 0 \tag{E.113}$$

The two 2π phase changes within (E.113) cancels out and leads to the function described in (2.132). The function in (2.132) is therefore valid for both the set and reset states of the NDRO cell. The phase change through PL2 is written as:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8)$$
$$+ \arcsin\left(\frac{i_7}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6} i_7) = 0 \tag{E.114}$$

Rewriting (E.114) leads to the function described in (2.138). The phase change through PL3 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_6) + \arcsin\left(\frac{i_6}{I_{c5}}\right)$$
$$-\left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) \tag{E.115}$$
$$+ \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10} i_{13}) = 0$$

The function in (E.115) can be rewritten to derive (2.134). The function in (2.134) is therefore valid for both the set and reset states of the NDRO cell. The phase change through PL4 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \tag{E.116}$$

Rewriting (E.116) leads to the function described in (2.135). The function in (2.135) is therefore valid for both the set and reset states of the NDRO cell. The phase change loops PL5 and PL6 is illustrated in Fig. E.14. The phase change through PL5 can be written as:

$$\begin{aligned}&-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) - \arcsin\left(\frac{i_7}{I_{c6}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_6i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right)\\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8i_{10}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12})\\ &+ \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) = 0\end{aligned} \tag{E.117}$$

The phase change described in (E.117) can be rewritten to derive the function in (2.136). The function in (2.136) is therefore valid for both the set and reset states of the NDRO cell. The phase change through PL6 is described through:

$$\begin{aligned}&-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3i_4) - \arcsin\left(\frac{i_9}{I_{c7}}\right)\\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right)\\ &+ \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{15}) = 0\end{aligned} \tag{E.118}$$

Rewriting (E.118) leads to the function described in (2.139).

Set state – Clock input

The NDRO cell generates an output pulse when a clock input is received within the set state. The input pulse at **clk** causes junctions J_7, J_8, J_{10} and J_{11} to switch and undergo a 2π phase shift. The phase loops shown in Fig. E.13 and E.14 change due to these switching junctions. It should be noted that the phase loops also consider the phase changes due to the original input pulse at **a**. The phase change through the PL1 loop is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) + 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \tag{E.119}$$

The function in (E.119) is therefore equal to (E.113) and can be rewritten to form (2.132). The phase change through PL2 is written as:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) + \arcsin\left(\frac{i_7}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) = 0 \tag{E.120}$$

Rewriting (E.120) leads to (E.114) and can be written in terms of the function described in (2.138). The phase change through PL3 is described through:

$$\begin{aligned}&-\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_6) + \arcsin\left(\frac{i_6}{I_{c5}}\right)\\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10})\\ &+ 2\pi + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0\end{aligned} \tag{E.121}$$

The function in (E.121) is equal to (E.115) and can be rewritten to derive (2.134). The phase change through PL4 is described through:

$$-\left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) + 2\pi + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \tag{E.122}$$

Rewriting (E.122) leads to (E.116) and can be written as the function described in (2.135). The phase change loops PL5 and PL6 is illustrated in Fig. E.14. The phase change through PL5 can be written as:

$$\begin{aligned}&-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) - \arcsin\left(\frac{i_7}{I_{c6}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right)\\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12})\\ &+ 2\pi + \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) = 0\end{aligned} \tag{E.123}$$

The phase change described in (E.123) is equal to (E.117) and can be rewritten to derive the function in (2.136).The phase change through PL6 is described through:

$$\begin{aligned}&-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right)\\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11}i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right)\\ &+ 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11}i_{15}) = 0\end{aligned} \tag{E.124}$$

Simplifying (E.124) leads to (E.118) and can be rewritten to derive the function described in (2.139).

Set to Reset state

The NDRO cell transitions from the set to the reset state when an input is received at **b**. This input pulse causes junctions J_4, J_6 and J_7 to switch and undergo a 2π phase shift. The phase change within the loops shown in Fig. E.13 and E.14 are now evaluated for the transition from set state to reset state. It should be noted that the 2π phase changes within the cell due to the original input pulse at **a** should also be considered within the analysis. The phase change through the PL1 loop is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \\ + 2\pi + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) = 0 \end{aligned} \tag{E.125}$$

The phase change described in (E.125) can be rewritten to derive the function described in (2.132). The phase change through PL2 is written as:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) \\ + 2\pi + \arcsin\left(\frac{i_7}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) = 0 \end{aligned} \tag{E.126}$$

The phase change in (E.126) is therefore equal to (E.108) and rewriting these equations leads to the function described in (2.133). The phase change through PL3 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_6) + \arcsin\left(\frac{i_6}{I_{c5}}\right) \\ -\left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) + 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) \\ + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \end{aligned} \tag{E.127}$$

The function in (E.127) can be rewritten to derive (2.134). The phase change through PL4 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12}) + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10}i_{13}) = 0 \end{aligned} \tag{E.128}$$

Rewriting (E.128) leads to the function described in (2.135). The phase change loops PL5 and PL6 is illustrated in Fig. E.14. The phase change through PL5 can be written as:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) - \arcsin\left(\frac{i_7}{I_{c6}}\right) - 2\pi - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) + 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right) \\ -\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10}i_{12}) \\ + \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) = 0 \end{aligned} \tag{E.129}$$

The phase change described in (E.129) is equal to (E.111) and can be rewritten to derive the function in (2.136).The phase change through PL6 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + 2\pi - \arcsin\left(\frac{i_9}{I_{c7}}\right) \\ -\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11} i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right) \\ + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11} i_{15}) = 0 \end{aligned} \tag{E.130}$$

Rewriting (E.130) results in the function described in (2.137).

Reset state – Clock input

The NDRO cell within the reset state does not generate an output pulse at **Q** when a clock input is received at **clk**. The phase change loops are illustrated within Fig. E.13 and E.14. The phase change through the PL1 loop is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p1}i_1) - \arcsin\left(\frac{i_1}{I_{c1}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_2 i_2) + \arcsin\left(\frac{i_2}{I_{c2}}\right) \\ + \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p3} i_3) = 0 \end{aligned} \tag{E.131}$$

Rewriting (E.131) leads to the function described in (2.132). The phase change through PL2 is written as:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) + \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) \\ + \arcsin\left(\frac{i_7}{I_{c6}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p6} i_7) = 0 \end{aligned} \tag{E.132}$$

Rewriting (E.132) leads to the function described in (2.133). The phase change through PL3 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p4}i_5) - \arcsin\left(\frac{i_5}{I_{c4}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_5 i_6) + \arcsin\left(\frac{i_6}{I_{c5}}\right) \\ -\left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) \\ + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10} i_{13}) = 0 \end{aligned} \tag{E.133}$$

The function in (E.133) can be rewritten to derive (2.134). The phase change through PL4 is described through:

$$\begin{aligned} -\left(\frac{2\pi}{\Phi_0}\right)(L_{p8}i_{11}) - \arcsin\left(\frac{i_{11}}{I_{c8}}\right) - 2\pi + \left(\frac{2\pi}{\Phi_0}\right)(L_{10} i_{12}) + 2\pi + \arcsin\left(\frac{i_{12}}{I_{c9}}\right) \\ + \arcsin\left(\frac{i_{13}}{I_{c10}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p10} i_{13}) = 0 \end{aligned} \tag{E.134}$$

Rewriting (E.134) leads to the function described in (2.135). The phase change through PL5 can be written as:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p6}i_7) - \arcsin\left(\frac{i_7}{I_{c6}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_6 i_8) - \arcsin\left(\frac{i_9}{I_{c7}}\right) \\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) - 2\pi - \arcsin\left(\frac{i_{12}}{I_{c9}}\right) - \left(\frac{2\pi}{\Phi_0}\right)(L_{10} i_{12}) \\ &\qquad + 2\pi + \arcsin\left(\frac{i_{11}}{I_{c8}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_{p8} i_{11}) = 0 \end{aligned} \tag{E.135}$$

The phase change described in (E.135) can be rewritten to derive the function in (2.136).The phase change through PL6 is described through:

$$\begin{aligned} &-\left(\frac{2\pi}{\Phi_0}\right)(L_{p3}i_3) - \arcsin\left(\frac{i_3}{I_{c3}}\right) + \left(\frac{2\pi}{\Phi_0}\right)(L_3 i_4) - \arcsin\left(\frac{i_9}{I_{c7}}\right) \\ &-\left(\frac{2\pi}{\Phi_0}\right)(L_7 i_9) + \left(\frac{2\pi}{\Phi_0}\right)(L_8 i_{10}) + \left(\frac{2\pi}{\Phi_0}\right)(L_{11} i_{14}) + \arcsin\left(\frac{i_{15}}{I_{c11}}\right) \\ &\qquad + \left(\frac{2\pi}{\Phi_0}\right)(L_{p11} i_{15}) = 0 \end{aligned} \tag{E.136}$$

Rewriting (E.136) leads to the function described in (2.137).

Appendix F

Current Distribution Simulation Results for Designed RSFQ Cell Library

RSFQ OR2 cell

Table F.1: Comparison between calculated and simulated values for current distribution for the RSFQ OR2 circuit set state with input at **a**.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	158.127650671	159.857927599	−1.0824 %
i_2	16.872349328	17.485305889	−3.5056 %
i_3	119.086005817	119.535166788	−0.3758 %
i_4	102.213656489	102.049860899	0.1605 %
i_5	158.127650671	158.151897677	−0.0153 %
i_6	16.872349328	16.848102322	0.1439 %
i_7	119.086005817	119.172221458	−0.0723 %
i_8	102.213656489	102.324119136	−0.1080 %
i_9	45.572687021	45.626019963	−0.1169 %
i_{10}	74.431392455	74.477276096	−0.0616 %
i_{11}	221.141294565	221.148743867	−0.0034 %
i_{12}	182.798389500	182.799723528	−0.0007 %
i_{13}	−7.798389500	−7.799723528	−0.0171 %
i_{14}	203.255036589	203.259432901	−0.0022 %
i_{15}	−10.087868476	−10.089587437	−0.0170 %
i_{16}	185.087868476	185.089587437	−0.0009 %

Table F.2: Comparison between calculated and simulated values for current distribution for the RSFQ OR2 circuit set state with input at **b**.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	158.127650671	158.151897677	−0.0153 %
i_2	16.872349328	16.848102322	0.1439 %
i_3	119.086005817	119.172221458	−0.0723 %
i_4	102.213656489	102.324119136	−0.1080 %
i_5	158.127650671	159.857927599	−1.0824 %
i_6	16.872349328	17.485305889	−3.5056 %
i_7	119.086005817	119.535166788	−0.3758 %
i_8	102.213656489	102.049860899	0.1605 %
i_9	45.572687021	45.626019963	−0.1169 %
i_{10}	74.431392455	74.477276096	−0.0616 %
i_{11}	221.141294565	221.148743867	−0.0034 %
i_{12}	182.798389500	182.799723528	−0.0007 %
i_{13}	−7.798389500	−7.799723528	0.0171 %
i_{14}	203.255036589	203.259432901	−0.0022 %
i_{15}	−10.087868476	−10.089587437	0.0170 %
i_{16}	185.087868476	185.089587437	−0.0009 %

RSFQ AND2 cell

Table F.3: Comparison between calculated and simulated values for current distribution for the RSFQ AND2 circuit reset state.

	Calculated (μA)	Simulated (μA)	% Difference
i_1	171.074529352	171.074529382	−1.735E-8 %
i_2	3.925470647	3.925470617	7.562E-7 %
i_3	159.062413967	159.062414033	−4.103E-8 %
i_4	19.863056679	19.863056584	4.780E-7 %
i_5	25.291038378	25.291038337	1.602E-7 %
i_6	61.743351937	61.743351765	2.794E-7 %
i_7	−16.589256879	−16.589256842	2.234E-7 %
i_8	171.074529352	171.074529382	−1.735E-8 %
i_9	3.925470647	3.925470617	7.562E-7 %
i_{10}	159.062413967	159.062414033	−4.103E-8 %
i_{11}	19.863056679	19.863056584	4.780E-7 %
i_{12}	25.291038378	25.291038337	1.602E-7 %
i_{13}	61.743351937	61.743351765	2.794E-7 %
i_{14}	−16.589256879	−16.589256842	2.233E-7 %
i_{15}	163.067709095	163.067709159	−3.922E-8 %
i_{16}	11.932290904	11.932290840	5.360E-7 %
i_{17}	136.350214147	136.350214164	−1.252E-8 %
i_{18}	−33.178513759	−33.178513685	2.234E-7 %
i_{19}	50.582076756	50.582076675	1.602E-7 %
i_{20}	141.821486240	141.821486314	−5.226E-8 %

Table F.4: Comparison between calculated and simulated values for current distribution for the RSFQ AND2 circuit set A state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	138.021006878	152.428793392	−9.4521 %
i_2	36.978993121	40.552023403	−8.8110 %
i_3	−0.986494835	2.094630122	−147.0964 %
i_4	212.965487956	213.457393280	−0.2304 %
i_5	−22.119593912	−22.254600366	−0.6066 %
i_6	182.035773640	182.320182520	−0.1560 %
i_7	8.810120403	8.882610393	−0.8161 %
i_8	171.639953156	171.641600110	−0.0010 %
i_9	3.360046843	3.358399889	0.0490 %
i_{10}	161.420543122	161.427382249	−0.0042 %
i_{11}	16.939503721	16.931017640	0.0501 %
i_{12}	41.490133128	41.536588519	−0.1118 %
i_{13}	79.985606451	80.038043100	−0.0655 %
i_{14}	−21.555969601	−21.570436940	−0.0671 %
i_{15}	170.292512285	170.313589124	−0.0124 %
i_{16}	4.707487714	4.686410875	0.4497 %
i_{17}	160.336948498	160.404422722	−0.0421 %
i_{18}	19.370539215	19.281988152	0.4592 %
i_{19}	−12.745849198	−12.687826547	0.4573 %
i_{20}	162.254150801	162.312173452	−0.0357 %

Table F.5: Comparison between calculated and simulated values for current distribution for the RSFQ AND2 circuit set B state.

	Calculated (μA)	Simulated (μA)	% Calculation Error
i_1	171.639953156	171.390802289	0.1454 %
i_2	3.360046843	3.291854804	2.0715 %
i_3	161.420543122	161.372238362	0.0299 %
i_4	16.939503721	16.919616441	0.1175 %
i_5	41.490133128	41.539175035	−0.1181 %
i_6	79.985606451	80.030630604	−0.0563 %
i_7	−21.555969601	−21.571839127	−0.0736 %
i_8	138.021006878	152.428775037	−9.4521 %
i_9	36.978993121	40.552058835	−8.8111 %
i_{10}	−0.986494835	2.094466753	−147.1000 %
i_{11}	212.965487956	213.457592081	−0.2305 %
i_{12}	−22.119593912	−22.255441168	−0.6104 %
i_{13}	182.035773640	182.319291696	−0.1555 %
i_{14}	8.810120403	8.882859216	−0.8189 %
i_{15}	170.292512285	170.313173575	−0.0121 %
i_{16}	4.707487714	4.686826424	0.4408 %
i_{17}	160.336948498	160.403092556	−0.0421 %
i_{18}	19.370539215	19.283733867	0.4501 %
i_{19}	−12.745849198	−12.688979910	0.4482 %
i_{20}	162.254150801	162.311020089	−0.0350 %

Appendix G

Margin Analysis of Designed RSFQ Cell Library

RSFQ JTL

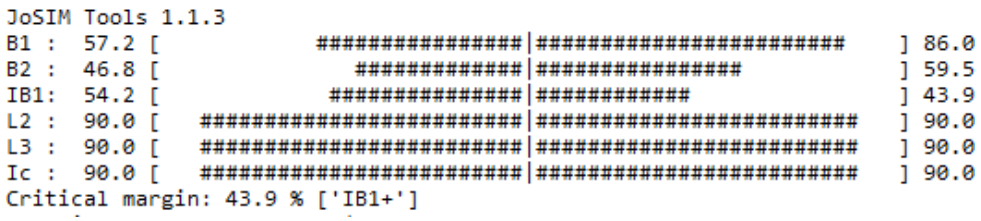

Figure G.1: Margin analysis of the designed RSFQ JTL cell.

RSFQ SPLIT

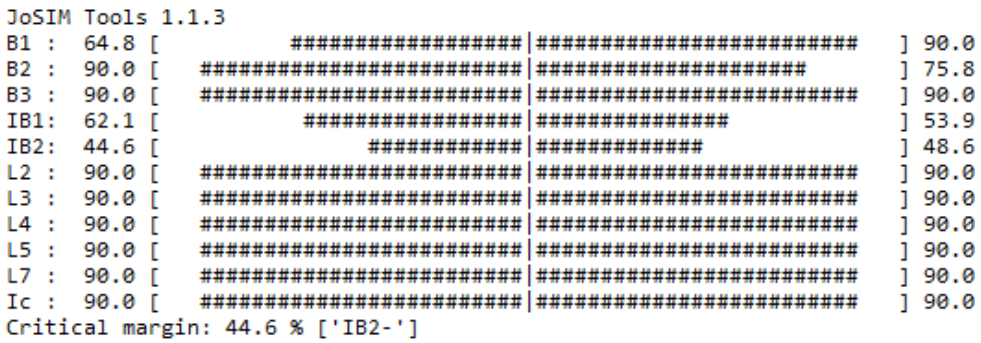

Figure G.2: Margin analysis of the designed RSFQ SPLIT cell.

RSFQ MERGE

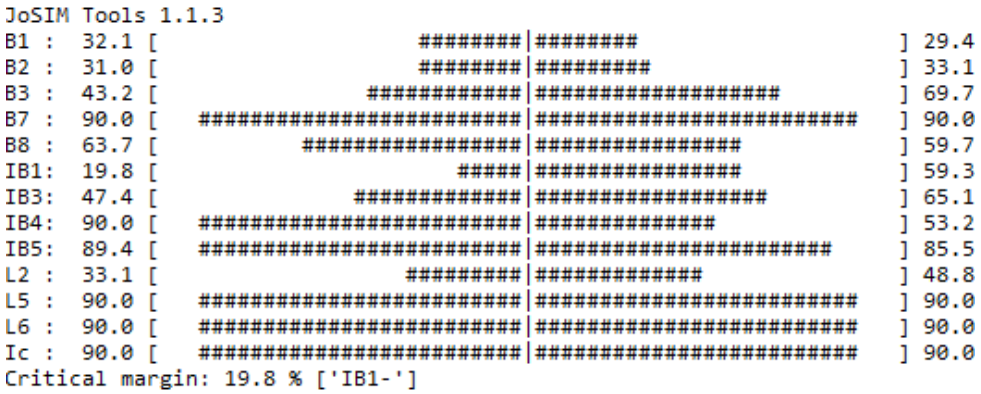

Figure G.3: Margin analysis of the designed RSFQ MERGE cell.

RSFQ DFF

Figure G.4: Margin analysis of the tuned RSFQ DFF cell.

RSFQ OR2

Figure G.5: Margin analysis of the tuned RSFQ OR2 cell.

RSFQ XOR

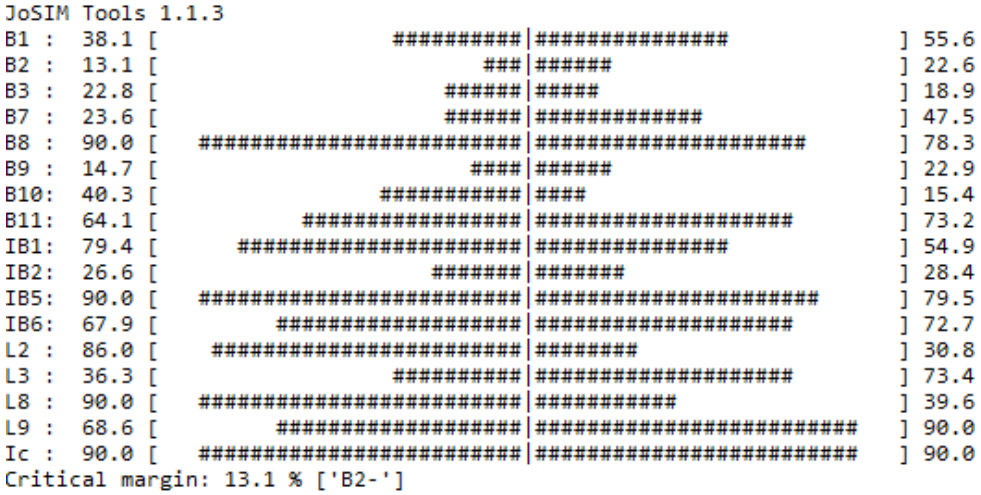

Figure G.6: Margin analysis of the tuned RSFQ XOR cell.

RSFQ AND2

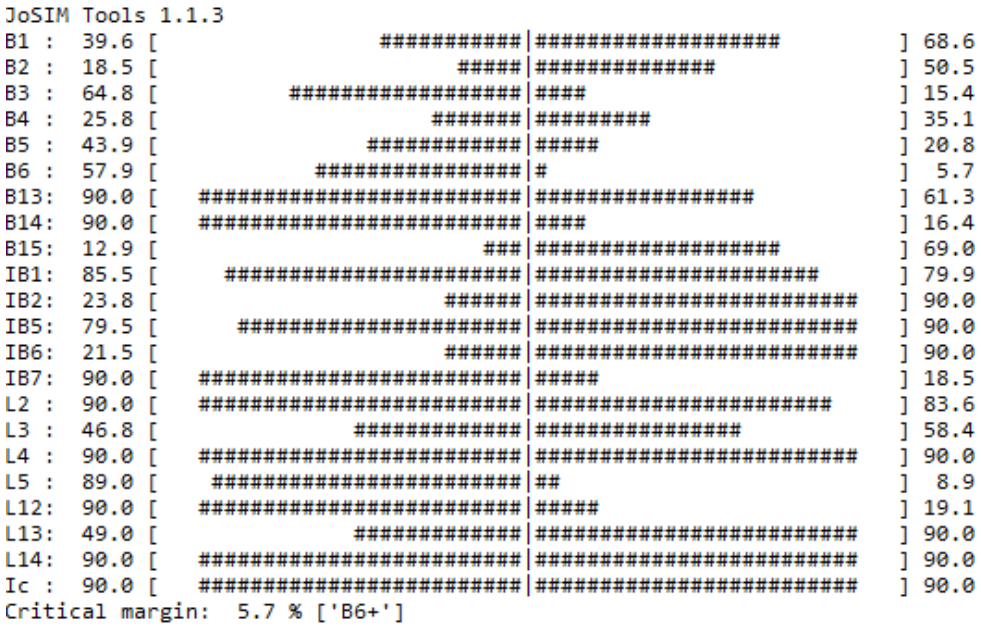

Figure G.7: Margin analysis of the designed RSFQ AND2 cell.

RSFQ NOT

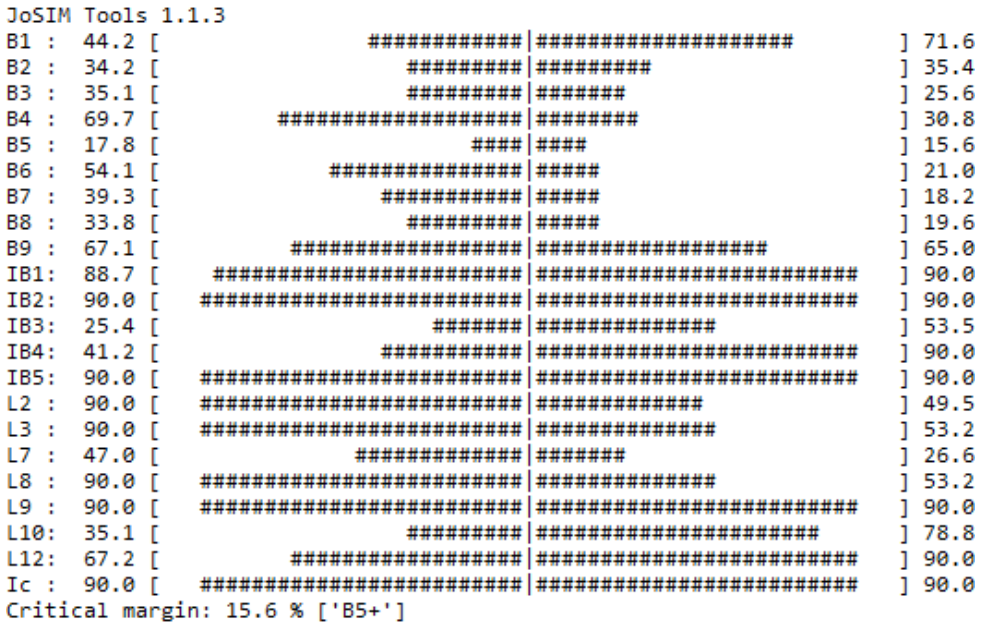

Figure G.8: Margin analysis of the tuned RSFQ NOT cell.

RSFQ NDRO

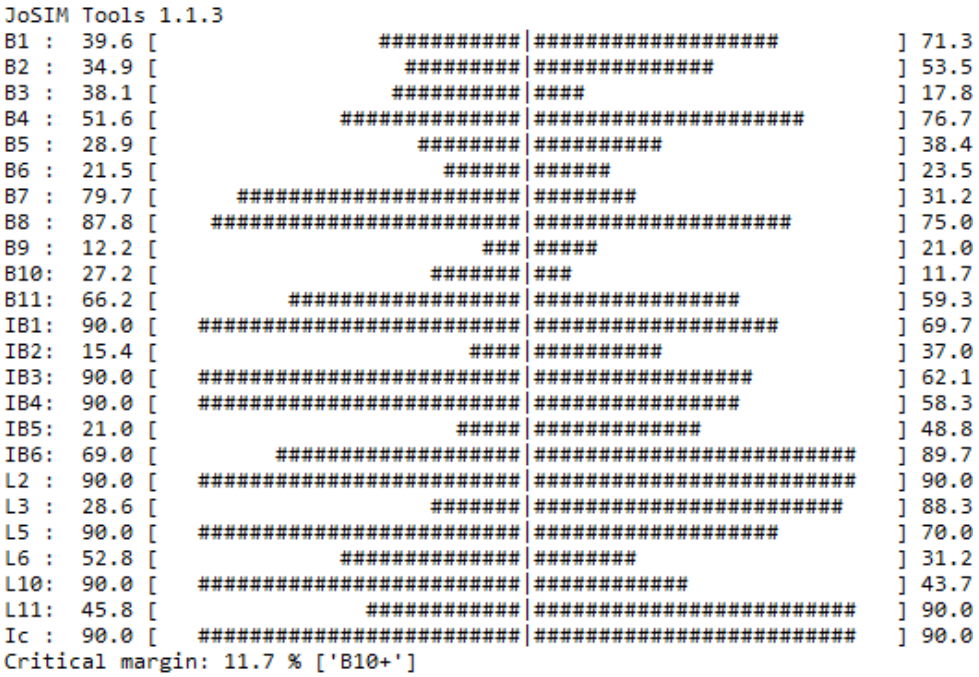

Figure G.9: Margin analysis of the tuned RSFQ NDRO cell.

Appendix H

Integrated Circuit Test Manual for SUMLL01-MRC

- L. Schindler, K. Jackman and C. J. Fourie

The test manual for SUMLL01-MRC is presented in this appendix. It includes all information for test structures regarding pin placement, bias current and expected output patterns. The work was a collaborative effort between all the authors. The effort regarding the design of the RSFQ test circuits was mainly my own. The flux trapping experiments were designed by K. Jackman and C. J. Fourie.

IARPA SuperTools Project

Integrated Circuit Test Manual

Chip: SUMLL01-MRC

Submitted by

Stellenbosch University (ColdFlux Team)

Authors:

Coenrad Fourie
Kyle Jackman
Lieze Schindler

Date: June 23, 2019

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1. Introduction

1.1 Copyright and permissions

This work was supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120. This integrated circuit was designed as part of the ColdFlux project under the SuperTools program.

2. Description of chip

2.1 Die layout

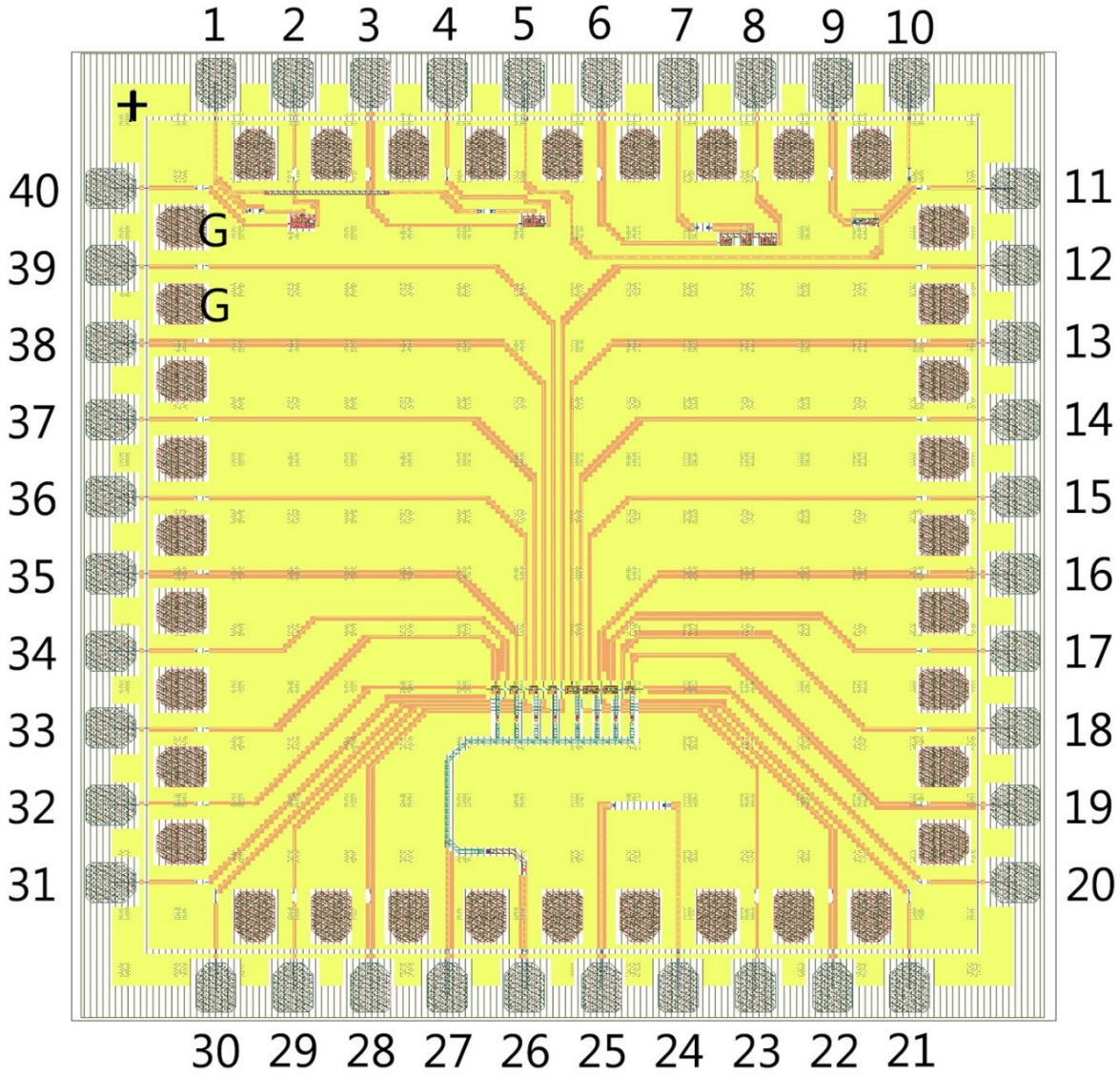

Figure 2.1: GDS layout view of die.

2.2 Pin assignment table

Table 2.1: Chip pin numbers.

Pin	Experiment	Description
1	RSFQ01,RSFQ02	DC bias: 1.91 mA
2	RSFQ01	Output voltage: 0 - 100 µV
3	RSFQ02	Signal input current (0 – 600 µA)
4	RSFQ02	Output voltage: 0 - 100 µV
5	RSFQ03	Tuning input current: ± 100 µA
6	PTLTXRX01	Signal input current (0 – 600 µA)
7	PTLTXRX01	DC bias input: 1.96 mA
8	PTLTXRX01	Output voltage: 0 - 100 µV
9	RSFQ03	Signal input current (0 – 600 µA)
10	RSFQ03	DC bias input: 1.768 mA
11	RSFQ03	Output voltage: 0 - 100 µV
12	FLUX05	$I_{mod-out}$ (modulation current)
13	FLUX05	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
14	FLUX06	$I_{mod-out}$ (modulation current)
15	FLUX06	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
16	FLUX07	$I_{mod-out}$ (modulation current)
17	FLUX07	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
18	FLUX08	$I_{mod-out}$ (modulation current)
19	FLUX08	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
20	FLUX08	I_{mod-in} (modulation current)
21	FLUX07	I_{mod-in} (modulation current)
22	FLUX06	I_{mod-in} (modulation current)
23	FLUX05	I_{mod-in} (modulation current)
24	HEATER	First terminal for heater (50 Ω)
25	HEATER	Second terminal for heater (50 Ω)
26	FLUX01 – FLUX08	$I_{coil_{in}}$ for all flux linkage experiments
27	FLUX01 – FLUX08	$I_{coil_{out}}$ for all flux linkage experiments
28	FLUX04	I_{mod-in} (modulation current)
29	FLUX03	I_{mod-in} (modulation current)
30	FLUX02	I_{mod-in} (modulation current)
31	FLUX01	I_{mod-in} (modulation current)
32	FLUX01	$I_{mod-out}$ (modulation current)
33	FLUX02	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
34	FLUX02	$I_{mod-out}$ (modulation current)
35	FLUX02	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
36	FLUX03	$I_{mod-out}$ (modulation current)
37	FLUX03	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
38	FLUX04	$I_{mod-out}$ (modulation current)
39	FLUX04	$I_{bias}/V_{measure}$ (bias current and voltage measurement)
40	RSFQ01	Signal input current (0 – 600 µA)

3. Experiments

The chip can be heated (for defluxing purposes) through the 50 Ω heater resistor between pins 24 and 25.
The resistor in layer R5 is 10 µm wide.
A voltage of 4 V over the resistor is expected to provide proper heating, but experimentation may be necessary.
NB: The current limit is not known.
Zero magnetic field means the shielded test environment (smaller than 500 nT is sufficient).

3.1 RSFQ01: Skyplane-shielded RSFQ cells in magnetic field (low frequency test)

3.1.1 Aim

Test functionality of skyplane-shielded RSFQ cells and obtain magnetic field operating limits.

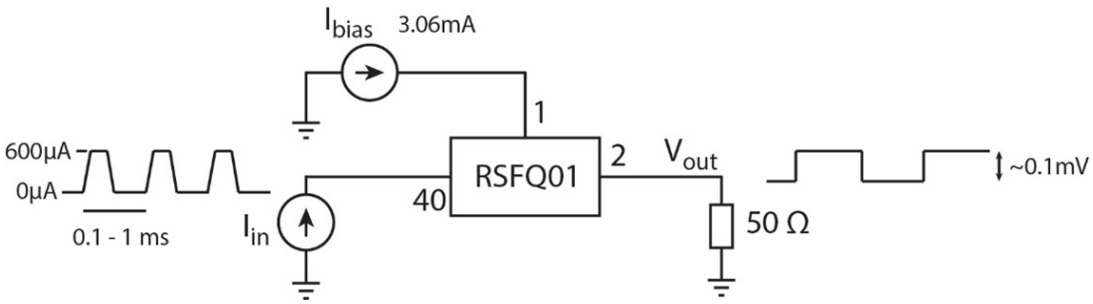

Figure 3.1: Test setup for RSFQ01 that shows required sources, pin numbers and signal shapes.

3.1.2 Pins

Table 3.1: Pin numbers for RSFQ01.

Pin	Description
1	Bias input current: 3.06 mA, with about ±20% margin.
2	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load, at exactly half the frequency of the input signal.
40	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.

3.1.3 Test sequence

Apply 3.06 mA of bias current to pin 1 to bias the circuit (it is shared with RSFQ02).

Apply an input pulse train as a current varying between 0 and 600 µA (adjustable by approximately 20%) to pin 40. This is a low frequency test, and a pulse frequency of 1 kHz to 10 kHz will be sufficient for testing purposes. **The upper frequency limit is not known, as it is a function of the test environment and the input line on the die. It may be tested.**

The output voltage at pin 2, measured into a 50 Ω load, should have exactly half the frequency of the input pulse train if the circuit functions correctly, with amplitude of approximately 100 µV.

Measurements required to adjust simulation tools, models and cell designs.

Operational verification:

1. Output voltage amplitude at zero tuning current and zero magnetic field.
2. Bias margins on pin 1 in zero magnetic field.
3. Maximum input signal frequency at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.2 RSFQ02: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.2.1 Aim

Test functionality of skyplane-shielded RSFQ input and output cells and obtain magnetic field operating limits in three axial directions.

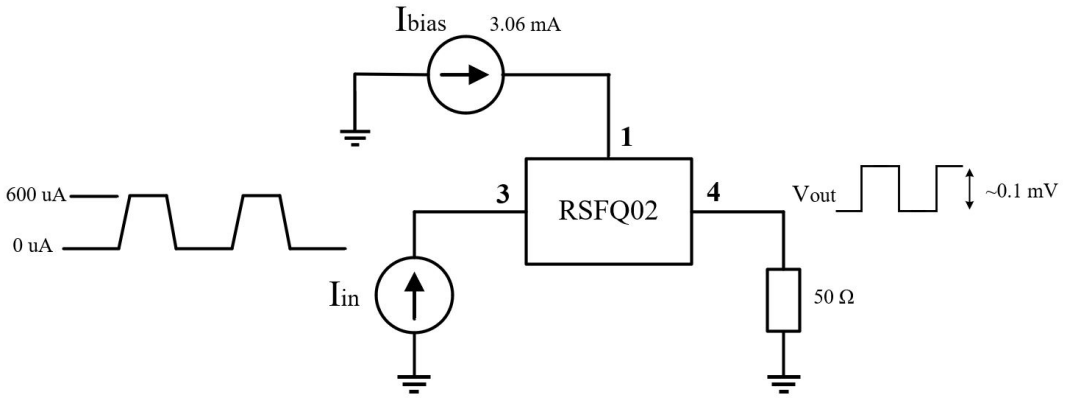

Figure 3.2: Test setup for RSFQ02 that shows required sources, pin numbers and signal shapes.

3.2.2 Pins

Table 3.2: Pin numbers for RSFQ02.

Pin	Description
1	Bias input current: 3.06 mA, with about ±20% margin.
3	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
4	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load, at exactly half the frequency of the input signal.

3.2.3 Test sequence

Apply 3.06 mA of bias current to pin 1 to bias the circuit (it is shared with RSFQ01). Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 3. The output voltage at pin 4, measured into a 50 Ω load, should have exactly half the frequency of the input pulse train if the circuit functions correctly. This voltage should vary between approximately 0 V and 100 μV.
Operational verification:

1. Output voltage amplitude at zero tuning current and zero magnetic field.
2. Bias margins on pin 1 in zero magnetic field.
3. Maximum input signal frequency at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.3 RSFQ03: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.3.1 Aim

Test functionality of unshielded RSFQ cells and obtain magnetic field operating limits.

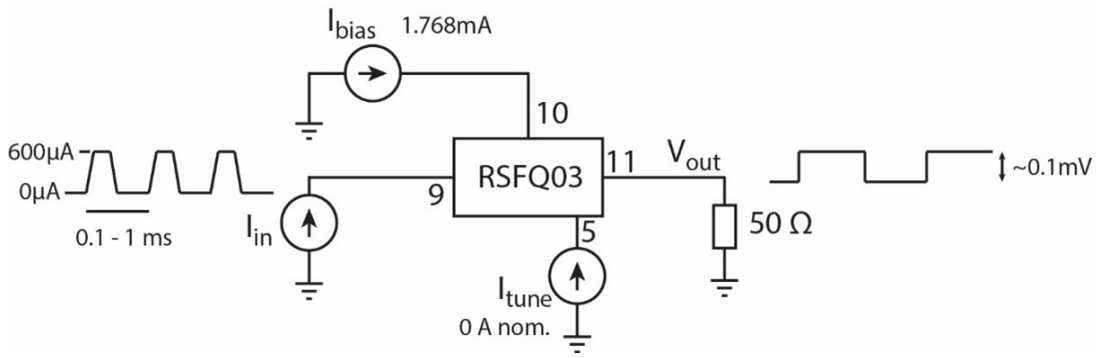

Figure 3.3: Test setup for RSFQ03 that shows required sources, pin numbers and signal shapes.

3.3.2 Pins

Table 3.3: Pin numbers for RSFQ03.

Pin	Description
5	Tuning input to maximize SFQ-DC converter output voltage swing. Nominally 0 A, adjustable over the approximate range ±100 μA.
9	Signal input current: 0 V for no input, pulsed to approximately 600 μA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
10	Bias input current: 1.768 mA, with about ±20 % margin.
11	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.3.3 Test sequence

Apply 1.77 mA of bias current to pin 10 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 9.

The output voltage at pin 11, measured into a 50 Ω load, should have exactly half the frequency of the input pulse train if the circuit functions correctly. This voltage should vary between approximately 0 V and 100 µV. **The amplitude of this output voltage can be adjusted to find the maximum with the application of a tuning current at pin 5. The tuning current, which is nominally 0 A, can be adjusted over the approximate range of ±100 μA.**

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero tuning current and zero magnetic field.
2. Maximum output voltage in zero magnetic field and tuning current required to achieve that.
3. Bias margins on pin 10 in zero magnetic field.
4. Maximum input signal frequency.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.4 PTLTXRX01: Skyplane-shielded RSFQ cells with integrated PTL transmitters and receivers in magnetic field (low frequency test)

3.4.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests the functionality of a NOT cell with integrated PTL drivers and receivers with PTL connections.

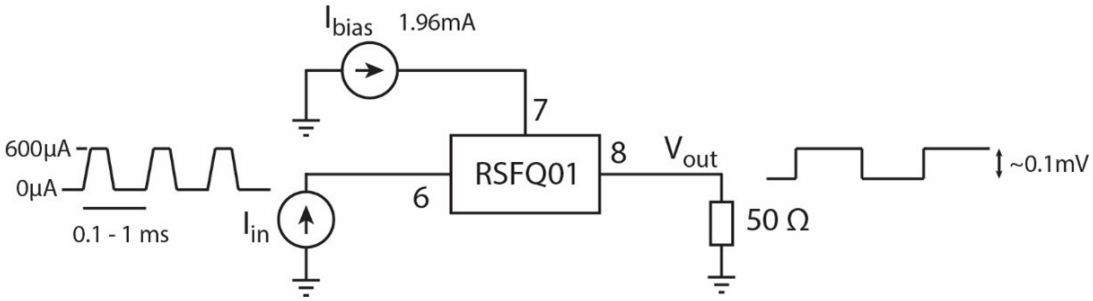

Figure 3.4: Test setup for PTLTXRX01 that shows required sources, pin numbers and signal shapes.

3.4.2 Pins

Table 3.4: Pin numbers for PTLTXRX01.

Pin	Description
7	Bias input current: 1.96 mA, with about ±20% margin.
6	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
8	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load, at exactly half the frequency of the input signal.

3.4.3 Test sequence

Apply 1.96 mA of bias current to pin 7 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 6. This is a low frequency test, and a pulse frequency of 1 kHz to 10 kHz will be sufficient for testing purposes. The output voltage at pin 8, measured into a 50 Ω load, should have exactly half the frequency of the input pulse train if the circuit functions correctly. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero tuning current and zero magnetic field.
2. Bias margins on pin 7 in zero magnetic field.
3. Maximum input signal frequency at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.5 FLUX01 to FLUX08: Flux linkage experiments

3.5.1 Aim

Measure inductance of SQUID loops with various hole structures, change in critical current due to trapped flux in holes near the SQUIDs, and coupling of holes and excitation coils to SQUID loops.

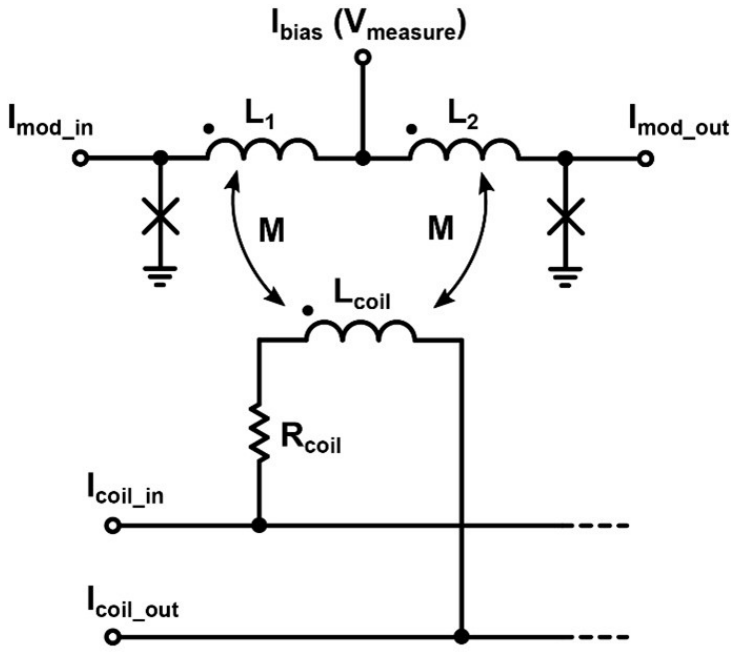

Figure 3.5: Generic circuit description for flux linkage tests.

3.5.2 Pins

Table 3.5: Pin descriptions for each of the eight flux linkage experiments (FLUX01 to FLUX08).

Pin	Description
$I_{bias}(V_{measure})$	Bias input current for SQUID, as well as voltage measurement in voltage mode.
I_{mod-in}	One terminal for modulation current source (isolated from common ground).
$I_{mod-out}$	Other terminal for modulation current source (isolated from common ground).
$I_{coil-in}$	One terminal for flux excitation coil (isolated from common ground).
$I_{coil-out}$	Other terminal for flux excitation coil (isolated from common ground).

Table 3.6: Pin numbers for the eight flux linkage experiments (FLUX01 to FLUX08).

Experiment	$I_{bias}/V_{measure}$	I_{mod-in}	$I_{mod-out}$	$I_{coil_{in}}$	$I_{coil_{out}}$
FLUX01	33	31	32	26	27
FLUX02	35	30	34	26	27
FLUX03	37	29	36	26	27
FLUX04	39	28	38	26	27
FLUX05	13	23	12	26	27
FLUX06	15	22	14	26	27
FLUX07	17	21	16	26	27
FLUX08	19	20	18	26	27

3.5.3 Test sequence (similar for each of the eight flux linkage experiments)

Measure I-V curve through I_{Bias} pin to obtain critical current of the SQUID in zero field. There is a 50 Ω resistor in series with the bias pin, so that the measured voltage includes the voltage drop over the resistor.

Zero the bias current, apply approximately 0.5 mA through $I_{coil-in}$ and $I_{coil-out}$ to add flux through the hole near the SQUID, heat cycle the chip to trap flux if applicable, zero the coil current, and repeat the I-V curve measurement to measure the change in critical current caused by trapped flux. Repeat this step for coil currents in increments of 0.5 mA over the range -20 mA to +20 mA.

Measure the self-inductance L1 + L2. Apply a bias current at I_{bias} that exceeds 500 μA to drive the SQUID into voltage mode. Measure the voltage at the $I_{bias}/V_{measure}$ pin. Apply a swept modulation current between pins I_{mod-in} and $I_{mod-out}$ and obtain the

modulation period at the $I_{bias}/V_{measure}$. This will provide the inductance. Measure the mutual inductance between the coil and the SQUID loop. Zero the modulation current at $I_{mod-in}/I_{mod-out}$, drive the SQUID into voltage mode by applying a current at I_{bias} that exceeds 500 μA, and sweep the coil current between $I_{coil-in}$ and $I_{coil-out}$. Measure the voltage modulation at $I_{bias}/V_{measure}$ to obtain the modulation period and thus the mutual inductance between the L_{coil} and (L1 + L2).

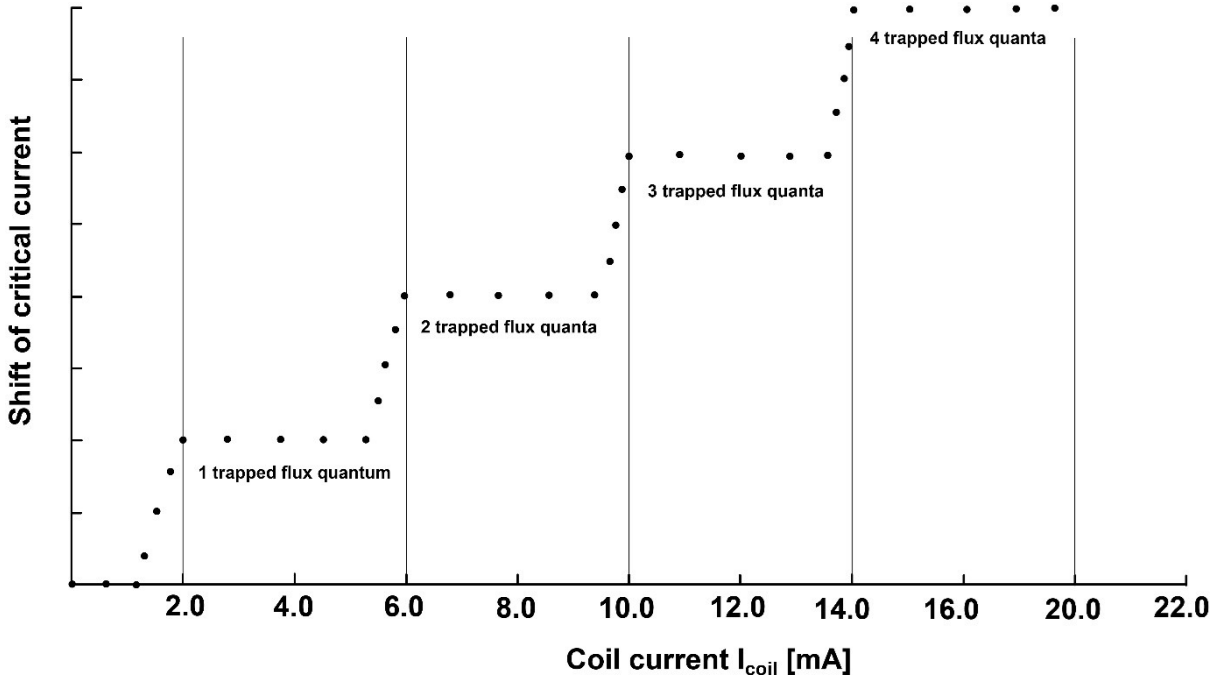

Figure 3.6: Example of expected shift in SQUID critical current as a function of coil current at cool-down, as detailed in Y. Yamanashi, H. Imai, and N. Yoshikawa, "Influence of magnetic flux trapped in moats on superconducting integrated circuit operation," IEEE Trans. Appl. Supercond., vol. 28, 1301105, 2018.

Measurements required to adjust simulation tools, models and cell designs for each of the eight flux linkage experiments:

1. Nominal critical current at zero cool-down magnetic field.
2. Critical current shift as a function of cool-down magnetic field (applied through coil in steps of 0.5 mA over the range −20 mA to 20 mA).
3. Self-inductance of SQUID loop (L1 + L2) by modulation of I_{mod}.
4. Mutual inductance between flux linkage coil and SQUID loop by modulation of I_{coil}.

Appendix I

Integrated Circuit Test Manual for SUMLL02-MRC

- L. Schindler, K. Jackman and C. J. Fourie

The test manual for SUMLL02-MRC is presented in this appendix. It includes all information for test structures regarding pin placement, bias current and expected output patterns. The work was a collaborative effort between all the authors. The effort regarding the design of the RSFQ test circuits was mainly my own. The flux trapping experiments were designed by K. Jackman and C. J. Fourie.

IARPA SuperTools Project

Integrated Circuit Test Manual

Chip: SUMLL02-MRC

Submitted by

Stellenbosch University (ColdFlux Team)

Authors:

Coenrad Fourie
Kyle Jackman
Lieze Schindler

Date: 23 October 2019

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1. Introduction

1.1 Copyright and permissions

This work was supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120.

1.2 Objectives

This integrated circuit was designed as part of the ColdFlux project under the SuperTools program to test model accuracy and tool performance. Primary tests include:

1. RSFQ cell operating margins as a function of applied magnetic field to verify the correctness of margin analyses and EM compact model extraction.

2. Bias-dependent delay timing measurements to verify correctness of JoSIM models and TimEx timing parameter extraction.

3. Flux trapping experiments with defined flux paths to improve on the experiments first included on the test chip SUMLL01-MRC, with the aim of verifying TetraHenry and InductEx models for currents induced by trapped flux.

Secondary tests, available as a result of the layout of the primary tests, include:

1. Verification of successful pulse transfer over passive transmission line interconnects used for signal routing in ColdFlux circuits.

2. Verification of operation of RSFQ cell library circuits - thus confirming correctness of schematics and layouts.

1.3 Unresolved verification

The experiments on this test chip do not support the following tests and verification:

1. Setup and hold timing for any circuits.
2. Passive transmission line reflections or characteristic impedance extraction.
3. Phase velocity on passive transmission lines.

2. Description of chip

2.1 Die layout

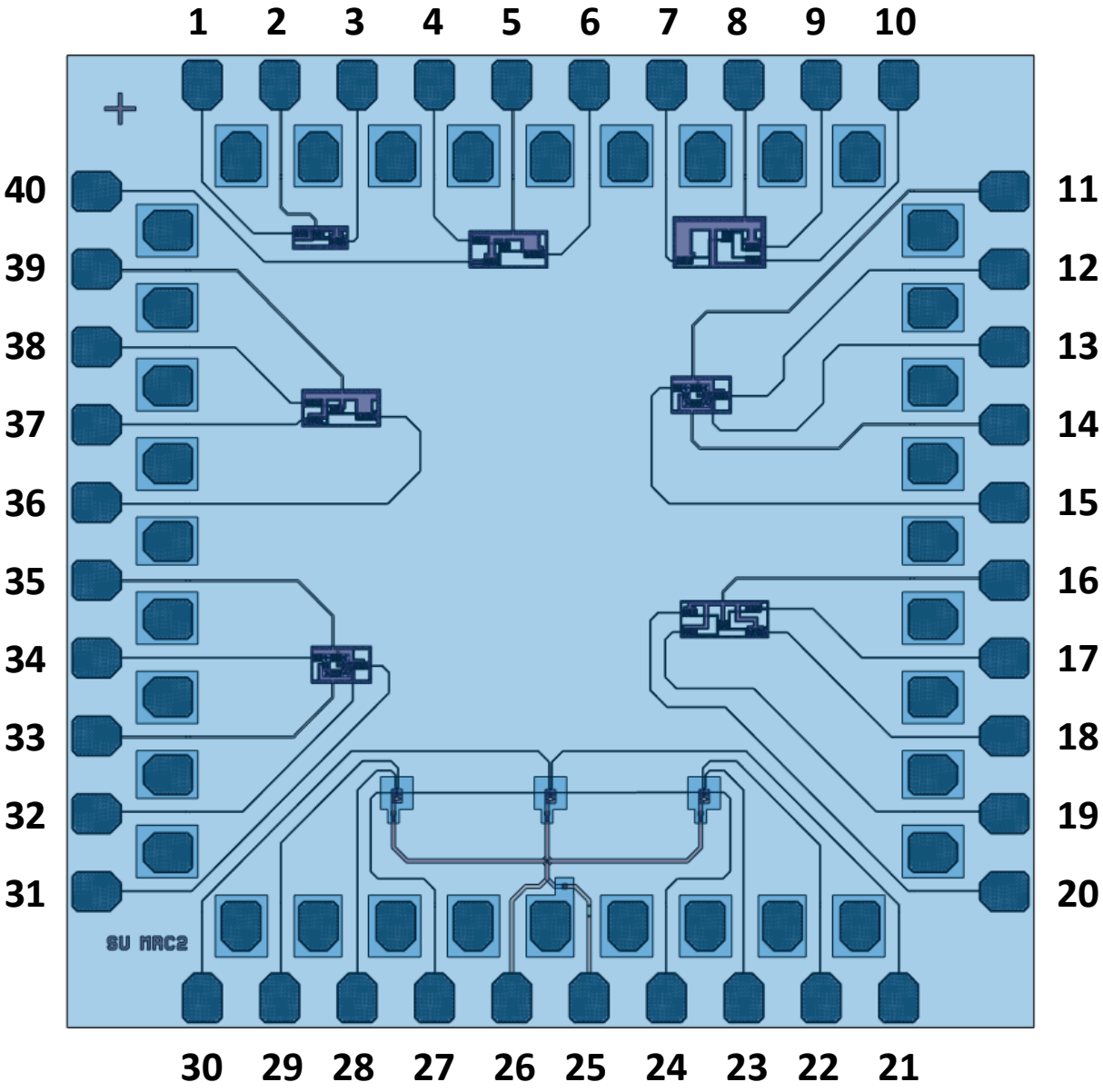


Figure 2.1: GDS layout view of die.

2.2 Pin assignment table

Table 2.1: Chip pin numbers.

Pin	Experiment	Description
1	RSFQ01	Signal input current (0 – 600 µA)
2	RSFQ01	DC bias: 1.91 mA
3	RSFQ01	Output voltage: 0 - 100 µV
4	RSFQ02	Signal input current (0 – 600 µA)
5	RSFQ02	DC bias: 4.36 mA
6	RSFQ02	Output voltage: 0 - 100 µV
7	RSFQ03	Output voltage: 0 - 100 µV
8	RSFQ03	DC bias input: 4.01 mA
9	RSFQ03	Signal input current (0 – 600 µA)
10	RSFQ03	Signal input current (0 – 600 µA)
11	TIMING02	DC bias input: 4.73 mA
12	TIMING02	Output voltage: 0 - 100 µV
13	TIMING02	Tuning input current: ± 87.5 µA
14	TIMING02	Tuning DC bias input: 2.10 mA
15	TIMING02	Signal input current (0 – 600 µA)
16	RSFQ05	DC bias input: 5.62 mA
17	RSFQ05	Signal input current (0 – 600 µA)
18	RSFQ05	Output voltage: 0 - 100 µV
19	RSFQ05	Signal input current (0 – 600 µA)
20	RSFQ05	Signal input current (0 – 600 µA)
21	FLUX02	$V_{measure}$ (bias current of SQUID 2)
22	FLUX01	I_{bias} (voltage measurement of SQUID 1)
23	FLUX01	$V_{measure}$ (bias current of SQUID 1)
24	FLUX01 – FLUX03	$I_{mod_{out}}$ (modulation current)
25	FLUX01 – FLUX03	$I_{coil_{out}}$ for all flux linkage experiments
26	FLUX01 – FLUX03	$I_{coil_{in}}$ for all flux linkage experiments
27	FLUX01 – FLUX03	$I_{mod_{in}}$ (modulation current)
28	FLUX03	I_{bias} (voltage measurement of SQUID 3)
29	FLUX03	$V_{measure}$ (bias current of SQUID 3)
30	FLUX02	I_{bias} (bias current of SQUID 2)
31	TIMING01	Output voltage: 0 - 100 µV
32	TIMING01	Tuning input current: ± 87.5 µA
33	TIMING01	Tuning DC bias input: 1.750 mA
34	TIMING01	Signal input current (0 – 600 µA)
35	TIMING01	DC bias input: 4.73 mA
36	RSFQ04	Output voltage: 0 - 100 µV
37	RSFQ04	Signal input current (0 – 600 µA)
38	RSFQ04	Signal input current (0 – 600 µA)
39	RSFQ04	DC bias input: 4.38 mA
40	RSFQ02	Signal input current (0 – 600 µA)

3. Experiments

3.1 RSFQ01: Skyplane-shielded RSFQ cells in magnetic field (low frequency test)

3.1.1 Aim

Test functionality of skyplane-shielded RSFQ cells and obtain magnetic field operating limits. The test circuit is a basic JTL with an integrated PTL driver and receiver with PTL connections.

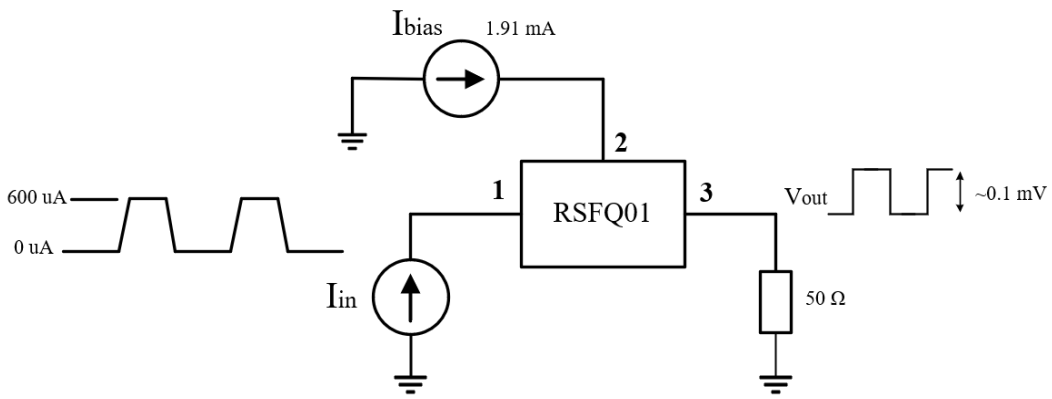


Figure 3.1: Test setup for RSFQ01 that shows required sources, pin numbers and signal shapes.

3.1.2 Pins

Table 3.1: Pin numbers for RSFQ01.

Pin	Description
2	Bias input current: 1.91 mA, with about ±20% margin.
3	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load, at exactly half the frequency of the input signal.
1	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.

3.1.3 Test sequence

Apply 1.91 mA of bias current to pin 2 to bias the circuit. Apply an input pulse train as a current varying between 0 and 600 µA (adjustable by approximately 20%) to pin 1. This is a low frequency test, and a pulse frequency of 1 kHz to 10 kHz will be sufficient for testing purposes. **The upper frequency limit is not known, as it is a function of the test environment and the input line on the die. It may be tested.**

The output voltage at pin 3, measured into a 50 Ω load, should have exactly half the frequency of the input pulse train if the circuit functions correctly, with amplitude of approximately 100 µV.

Measurements required to adjust simulation tools, models and cell designs.

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 2 in zero magnetic field.
3. Maximum input signal frequency at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.2 RSFQ02: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.2.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests a DFF (or DRO) with integrated PTL drivers and receivers connected through PTLs to the test bench.

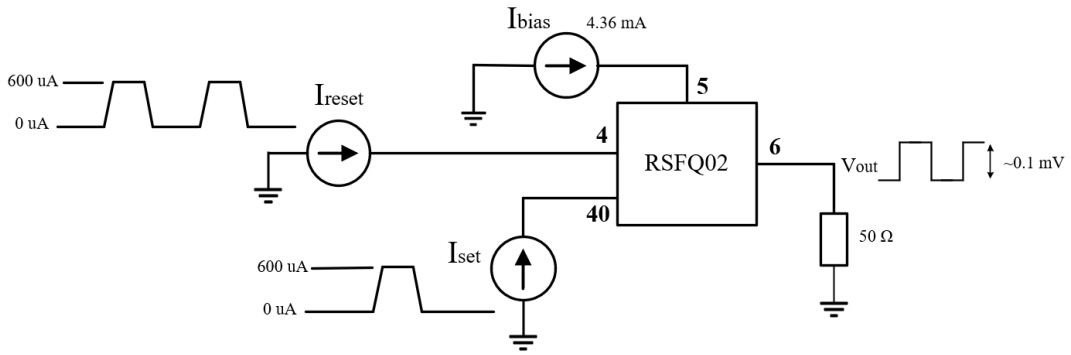


Figure 3.2: Test setup for RSFQ02 that shows required sources, pin numbers and signal shapes.

3.2.2 Pins

Table 3.2: Pin numbers for RSFQ02.

Pin	Description
4	Reset signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
40	Set signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
5	Bias input current: 4.36 mA, with about ±20 % margin.
6	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.2.3 Test sequence

Apply 4.36 mA of bias current to pin 5 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 4. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 40. The following test pattern (also illustrated in Fig. 3.3) is required to test all possible instances: no set signal before reset signal arrives, set signal before reset signal arrives, and two set signals before reset signal arrives. The output voltage at pin 6, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 5 in zero magnetic field.

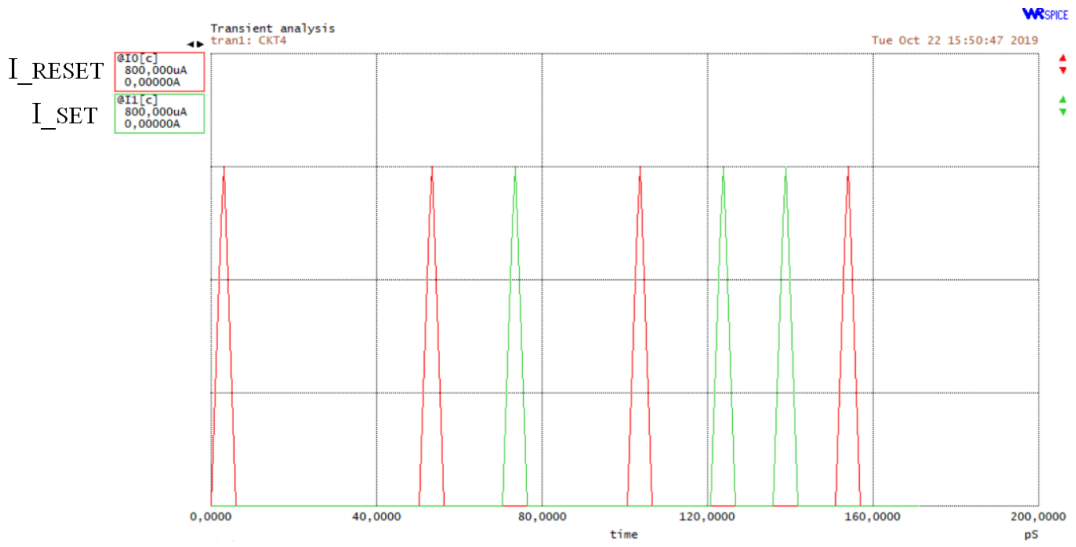


Figure 3.3: Example test pattern required to test RSFQ02, RSFQ03 and RSFQ04. The simulation pattern is only provided as a visual guide and the timing can be adjusted.

3. Maximum reset signal frequency.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.3 RSFQ03: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.3.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuits tests the functionality of a DFF with integrated PTL drivers and receivers with PTL connections. The test is similar to RSFQ02, but includes PTLs with corners to investigate the effect on circuit functionality.

3.3.2 Pins

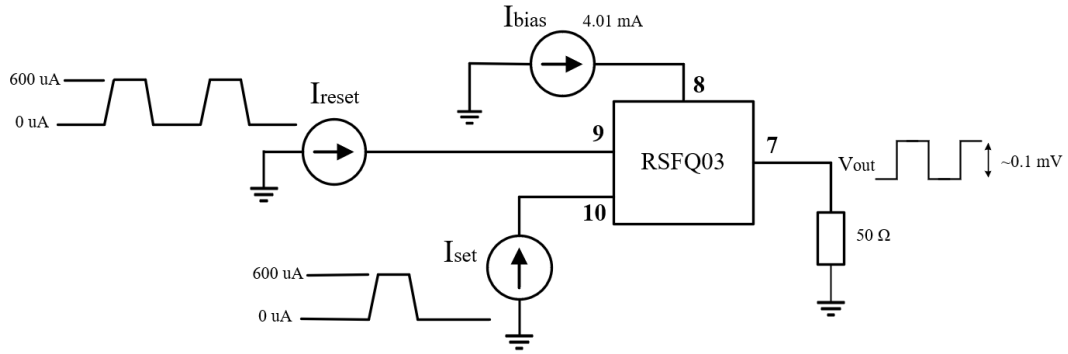


Figure 3.4: Test setup for RSFQ03 that shows required sources, pin numbers and signal shapes.

Table 3.3: Pin numbers for RSFQ03.

Pin	Description
9	Reset signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
10	Set signal input current:0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
8	Bias input current: 4.01 mA, with about ±20 % margin.
7	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.3.3 Test sequence

Apply 4.01 mA of bias current to pin 8 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 9. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 10. The following test pattern (also illustrated in Fig. 3.3) is required to test all possible instances: no set signal before reset signal arrives, set signal before reset signal arrives, and two set signals before reset signal arrives. The output voltage at pin 7, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 8 in zero magnetic field.
3. Maximum reset signal frequency.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.4 RSFQ04: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.4.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests the functionality of a NOT cell with integrated PTL drivers and receivers with PTL connections.

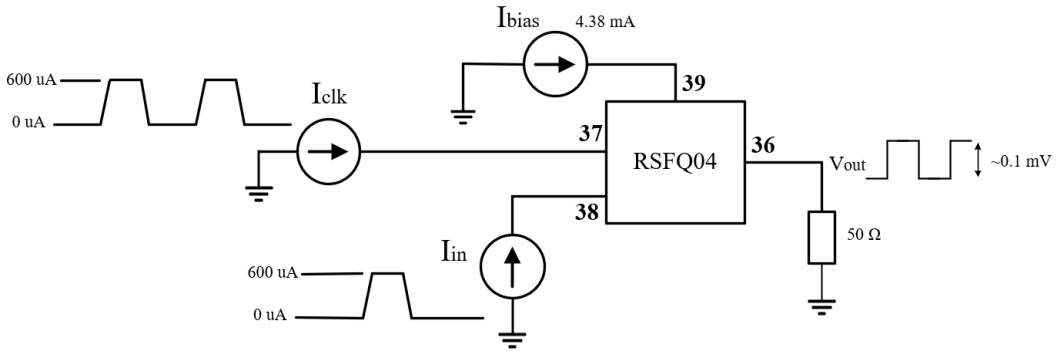


Figure 3.5: Test setup for RSFQ04 that shows required sources, pin numbers and signal shapes.

3.4.2 Pins

Table 3.4: Pin numbers for RSFQ04.

Pin	Description
37	Clock signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
38	Signal input current:0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
39	Bias input current: 4.38 mA, with about ±20 % margin.
36	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.4.3 Test sequence

Apply 4.38 mA of bias current to pin 39 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 37. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 38. The following test pattern (also illustrated in Fig. 3.3) is required to test all possible instances: no set signal before reset signal arrives, set signal before reset signal arrives, and two set signals before reset signal arrives. The output voltage at pin 36, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 39 in zero magnetic field.
3. Maximum reset signal frequency.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.5 RSFQ05: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.5.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests the functionality of the OR2 cell with integrated PTL drivers and receivers with PTL connections.

3.5.2 Pins

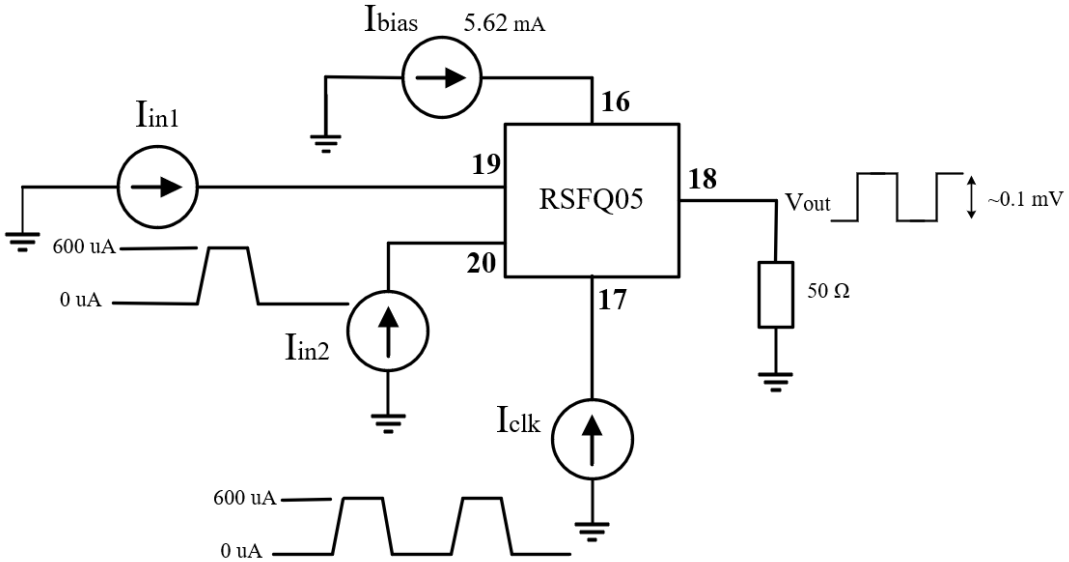


Figure 3.6: Test setup for RSFQ05 that shows required sources, pin numbers and signal shapes.

Table 3.5: Pin numbers for RSFQ05.

Pin	Description
19	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
20	Signal input current:0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
17	Clock signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
16	Bias input current: 5.62 mA, with about ±20 % margin.
18	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.5.3 Test sequence

Apply 5.62 mA of bias current to pin 16 to bias the circuit. Apply a clock input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 17. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 19 for input signal 1. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 20 for input signal 2. An example test pattern is shown in Fig. 3.7 and includes all possible combinations to analyse circuit functionality. The output voltage at pin 18, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.

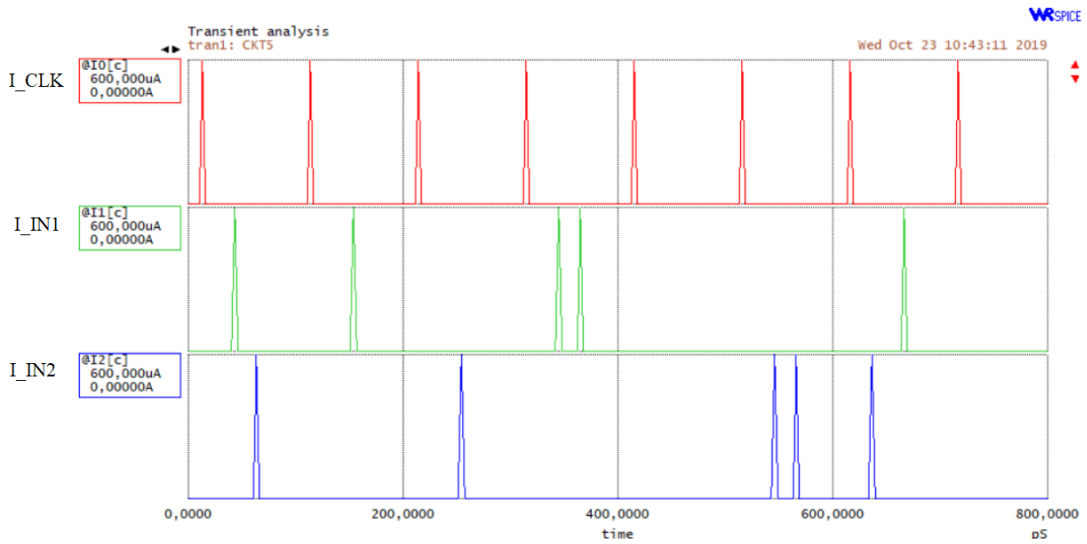


Figure 3.7: Example test pattern required to test RSFQ05. The simulation pattern is only provided as a visual guide and the timing can be adjusted.

2. Bias margins on pin 16 in zero magnetic field.
3. Maximum reset signal frequency.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.6 TIMING01: Timing analysis of RSFQ cells (low frequency test)

3.6.1 Aim

Evaluate the time delay of individual RSFQ cells. The circuit analyses the time delay of a JTL circuit by comparing the time delay of 4 abutted JTLs to 5 abutted JTLs. A single input line is split within the circuit and each SFQ pulse is transmitted to the abutted JTLs. The bias line of the 5 abutted JTLs can be tuned until the time delay is the same as that of 4 abutted JTLs. A JJ comparator was designed to only produce an output SFQ pulse if two pulses reach the cell within 0.5 ps of each other.

3.6.2 Pins

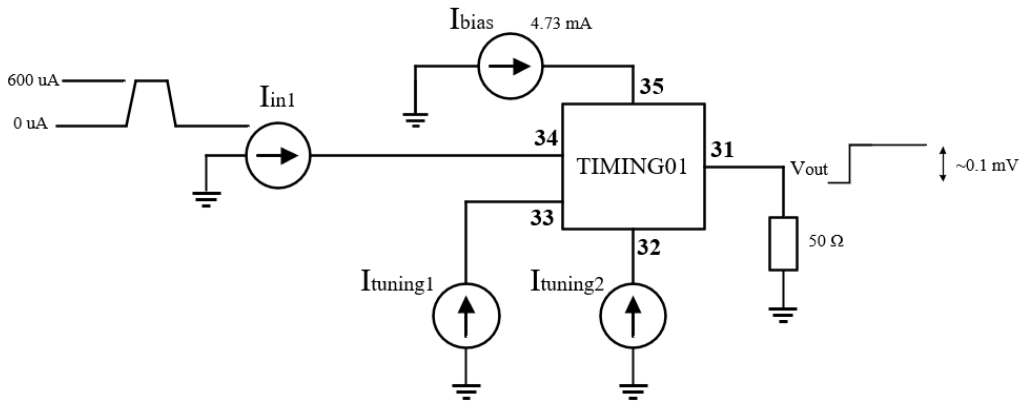


Figure 3.8: Test setup for TIMING01 that shows required sources, pin numbers and signal shapes.

Table 3.6: Pin numbers for TIMING01.

Pin	Description
34	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
32	Tuning pin with nominal current 0.0875 mA. This pin controls the biasing current for the JJ comparator.
33	Tuning bias input current: 1.75 mA. This pin controls the biasing current to the 5 abutted JTLs. The pin is used to tune the output delay until the output delay for the 5 abutted JTLs match the output delay of the 4 abutted JTLs.
35	Bias input current: 4.73 mA with about ±20 % margin.
31	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.6.3 Test sequence

Apply 4.73 mA of bias current to pin 31, 1.75 mA of bias current to pin 33 and 0.0875 mA of bias current to pin 32 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 34. The output voltage at pin 31, measured into a 50 Ω load, should have a change of voltage (either 0 V to 100 uV or 100 uV to 0 V) if the time delay of the 5 abutted JTLs are within 0.5 ps of the 4 abutted JTLs. Tuning pin 33 can be used to increase the biasing current to the 5 abutted JTLs, decreasing the time delay of these cells. Tuning pin 32 can be used to tune the biasing current of the decision JJ within the JJ comparator if a change of output at pin 34 can not be achieved when expected or when a change in output at pin 34 is observed in incorrect conditions.

If the time delay of the 5 abutted JTLs are within a 0.5 ps tolerance to the time delay of the 4 abutted JTLs, the frequency measured onto a 50 Ω resistor at output pin 31 should be exactly half of the input frequency at pin 34. If the time delay is not within the specified tolerance, there should be no change in output voltage measured over a 50 Ω resistor at pin 31.

Measurements required to extract delay times of RSFQ cells and to adjust simulation tools, models and cell designs

Operational verification:

1. No output voltage amplitude at nominal tuning current and zero magnetic field.
2. Maximum output voltage in zero magnetic field and tuning current, at pin 32 and pin 33, required to achieve that.
3. Tuning bias margins on pin 33 in zero magnetic field
4. Tuning bias margins on pin 32 in zero magnetic field when pin 33 is tuned to produce an output voltage measured over a 50 Ω resistor at pin 31.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.7 TIMING02: Timing analysis of RSFQ cells (low frequency test)

3.7.1 Aim

Evaluate the time delay of individual RSFQ cells in conjunction with TIMING01. The circuit analyses the time delay of a JTL circuit by comparing the time delay of 4 abutted JTLs to 6 abutted JTLs. A single input line is split within the circuit and each SFQ pulse is transmitted to the abutted JTLs. The bias line of the 6 abutted JTLs can be tuned until the time delay is the same as that of 4 abutted JTLs. A JJ comparator was designed to only produce an output SFQ pulse if two pulses reach the cell within 0.5 ps of each other.

3.7.2 Pins

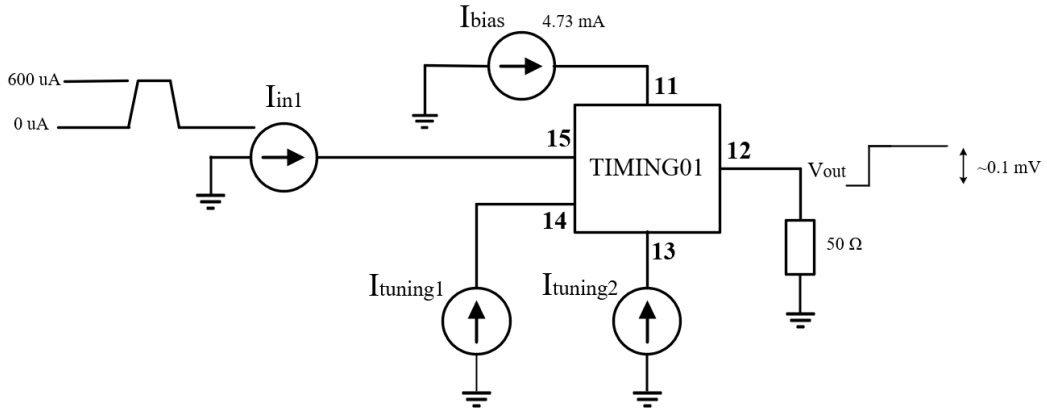


Figure 3.9: Test setup for TIMING02 that shows required sources, pin numbers and signal shapes.

Table 3.7: Pin numbers for TIMING02.

Pin	Description
15	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
13	Tuning pin with nominal current 0.0875 mA. This pin controls the biasing current for the JJ comparator.
14	Tuning bias input current: 2.10 mA. This pin controls the biasing current to the 5 abutted JTLs. The pin is used to tune the output delay until the output delay for the 5 abutted JTLs match the output delay of the 4 abutted JTLs.
11	Bias input current: 4.73 mA with about ±20 % margin.
12	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.7.3 Test sequence

Apply 4.73 mA of bias current to pin 11, 2.10 mA of bias current to pin 14 and 0.0875 mA of bias current to pin 13 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 15. The output voltage at pin 12, measured into a 50 Ω load, should have a change of voltage (either 0 V to 100 uV or 100 uV to 0 V) if the time delay of the 6 abutted JTLs are within 0.5 ps of the 4 abutted JTLs. Tuning pin 14 can be used to increase the biasing current to the 6 abutted JTLs, decreasing the time delay of these cells. Tuning pin 13 can be used to tune the biasing current of the decision JJ within the JJ comparator if a change of output at pin 12 can not be achieved when expected or when a change in output at pin 12 is observed in incorrect conditions.

If the time delay of the 6 abutted JTLs are within a 0.5 ps tolerance to the time delay of the 4 abutted JTLs, the frequency measured onto a 50 Ω resistor at output pin 12 should be exactly half of the input frequency at pin 15. If the time delay is not within the specified tolerance, there should be no change in output voltage measured over a 50 Ω resistor at pin 12.

Measurements required to extract delay times of RSFQ cells and to adjust simulation tools, models and cell designs

Operational verification:

1. No output voltage amplitude at nominal tuning current and zero magnetic field.
2. Maximum output voltage in zero magnetic field and tuning current, at pin 13 and pin 14, required to achieve that.
3. Tuning bias margins on pin 14 in zero magnetic field
4. Tuning bias margins on pin 13 in zero magnetic field when pin 14 is tuned to produce an output voltage measured over a 50 Ω resistor at pin 12.

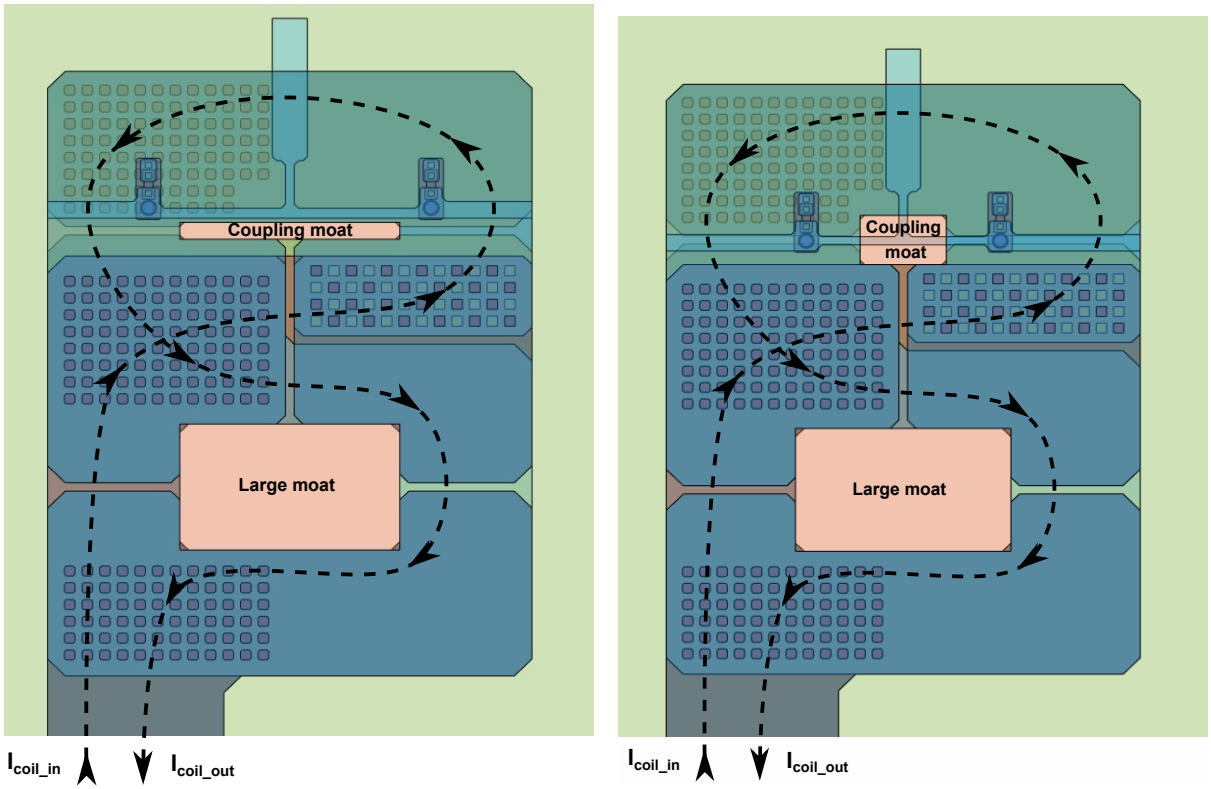
Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.8 FLUX01 to FLUX03: Flux linkage experiments

3.8.1 Aim

Measure inductance of the SQUID loops, change in critical current due to trapped flux in holes near the SQUIDs, and coupling of holes and excitation coils to SQUID loops. Each flux linkage experiment uses a coil above and below the ground plane and forces the flux to trap inside the 'Coupling' moat and the 'Large' moat shown in Fig. 3.10. Figure 3.11 shows the circuit diagram of a single flux linkage test circuit.



(a) Flux linkage structure FLUX02. (b) Flux linkage structure FLUX03.

Figure 3.10: Two of Flux linkage experiments with different coupling moats. The flux through the 'coupling moat' will also thread through the 'large moat'. This will prevent the flux from trapping in surrounding moats.

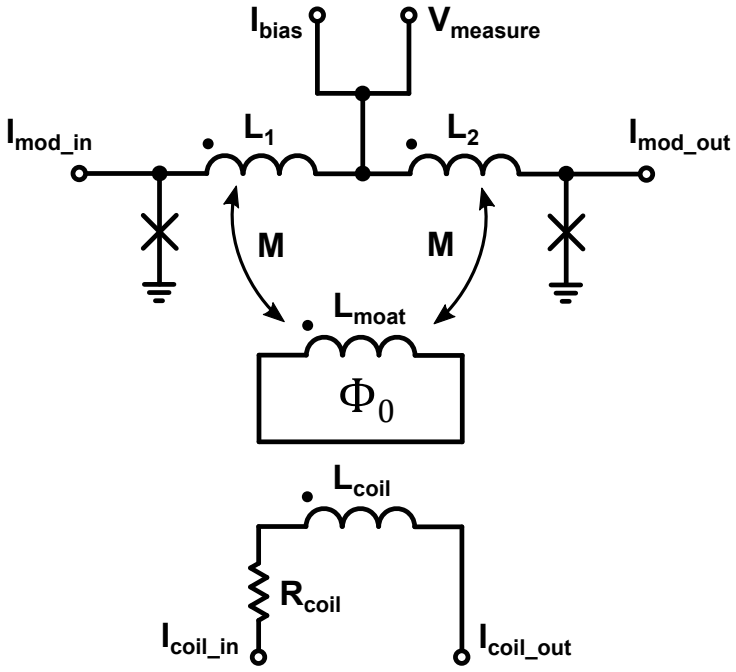


Figure 3.11: Generic circuit description for flux linkage tests.

3.8.2 Pins

Table 3.8: Pin descriptions for each of the three flux linkage experiments (FLUX01, FLUX02 and FLUX03).

Pin	Description
I_{bias}	Bias input current for SQUID.
$V_{measure}$	Voltage measurement in voltage mode.
$I_{mod_{in}}$	One terminal for modulation current source (isolated from common ground).
$I_{mod_{out}}$	Other terminal for modulation current source (isolated from common ground).
$I_{coil_{in}}$	One terminal for flux excitation coil (isolated from common ground).
$I_{coil_{out}}$	Other terminal for flux excitation coil (isolated from common ground).

Table 3.9: Pin numbers for the three flux linkage experiments (FLUX01, FLUX02 and FLUX03).

Experiment	I_{bias}	$V_{measure}$	$I_{mod_{in}}$	$I_{mod_{out}}$	$I_{coil_{in}}$	$I_{coil_{out}}$
FLUX01	22	23	27	24	26	25
FLUX02	30	21	27	24	26	25
FLUX03	28	29	27	24	26	25

3.8.3 Test sequence (similar for each of the two flux linkage experiments)

Measure I-V curve through I_{bias} pin to obtain critical current of the SQUID in zero field. There is a 10 Ω resistor in series with the voltage pin ($V_{measure}$), so that the measured voltage includes the voltage drop over the resistor.

Zero the bias current, apply approximately 0.1 mA through $I_{coil_{in}}$ and $I_{coil_{out}}$ to add flux through the hole near the SQUID, heat cycle the chip to trap flux if applicable, zero the coil current, and repeat the I-V curve measurement to measure the change in critical current (I_c) caused by trapped flux. Repeat this step for coil currents in increments of 0.1 mA over the range 0 mA to 1.5 mA. The expected measured critical current (I_c) of the three flux linkage tests are shown in Fig. 3.12.

Measure the self-inductance (L1 + L2). Apply a bias current at I_{bias} that exceeds 500 µA to drive the SQUID into voltage mode. Measure the voltage at the $V_{measure}$ pin. Apply a swept modulation current between pins $I_{mod_{in}}$ and $I_{mod_{out}}$ and obtain the modulation period at the $V_{measure}$ pin. This will provide the self-inductance.

Measure the mutual inductance between the coil and the SQUID loop. Zero the modulation current at $I_{mod_{in}}$ and $I_{mod_{out}}$, drive the SQUID into voltage mode by applying a current at I_{bias} that exceeds 500 µA, and sweep the coil current between $I_{coil_{in}}$ and $I_{coil_{out}}$. Measure the voltage modulation at $V_{measure}$ to obtain the modulation period and thus the mutual inductance between the L_coil and (L1 + L2).

Measurements required to adjust simulation tools, models and cell designs for each of the 2 flux linkage experiments:

1. Nominal critical current at zero cool-down magnetic field.
2. Critical current shift as a function of cool-down magnetic field (applied through coil in steps of 0.1 mA over the range 0 mA to 1.5 mA).
3. Self-inductance of SQUID loop (L1 + L2) by modulation of I_{mod}.
4. Mutual inductance between flux linkage coil and SQUID loop by modulation of I_{coil}.

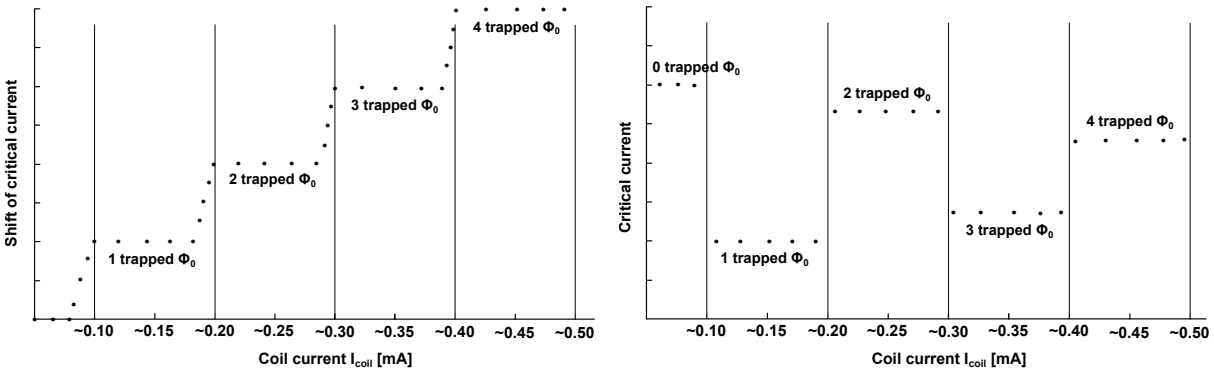


Figure 3.12: (Left) Example of expected shift in critical current (ΔI_c) of SQUID 1 and 2 (FLUX01 and FLUX02) as a function of coil current at cool-down, as detailed in [1]. (Right) Example of expected critical current (I_c) of SQUID 3 (FLUX03) as a function of coil current at cool-down.

References

[1] Y. Yamanashi, H. Imai, and N. Yoshikawa, "Influence of magnetic flux trapped in moats on superconducting integrated circuit operation," *IEEE Transactions on Applied Superconductivity*, vol. 28, no. 7, pp. 1–5, 2018.

Appendix J

Integrated Circuit Test Manual for SUMLL03

- L. Schindler, K. Jackman and C. J. Fourie

The test manual for SUMLL03 is presented in this appendix. It includes all information for test structures regarding pin placement, bias current and expected output patterns. The work was a collaborative effort between all the authors. The effort regarding the design of the RSFQ test circuits was mainly my own. The flux trapping experiments were designed by C. J. Fourie. The testing procedures for the flux trapping experiments are excluded from the test manual.

IARPA SuperTools Project

Integrated Circuit Test Manual

Chip: SUMLL03

Submitted by

Stellenbosch University (ColdFlux Team)

Authors:

Coenrad Fourie
Kyle Jackman
Lieze Schindler

Date: October 27, 2020

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1. Introduction

1.1 Copyright and permissions

This work was supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120.

1.2 Objectives

This integrated circuit was designed as part of the ColdFlux project under the SuperTools program to test model accuracy and tool performance. Primary tests include:

1. RSFQ cell operating margins as a function of applied magnetic field to verify the correctness of margin analyses and EM compact model extraction.

2. Bias-dependent delay timing measurements to verify correctness of JoSIM models and TimEx timing parameter extraction.

3. Flux trapping experiments with defined flux paths to improve on the experiments first included on the test chip SUMLL01-MRC, with the aim of verifying TetraHenry and InductEx models for currents induced by trapped flux.

Secondary tests, available as a result of the layout of the primary tests, include:

1. Verification of successful pulse transfer over passive transmission line interconnects used for signal routing in ColdFlux circuits.

2. Verification of operation of RSFQ cell library circuits - thus confirming correctness of schematics and layouts.

2. Description of chip

2.1 Die layout

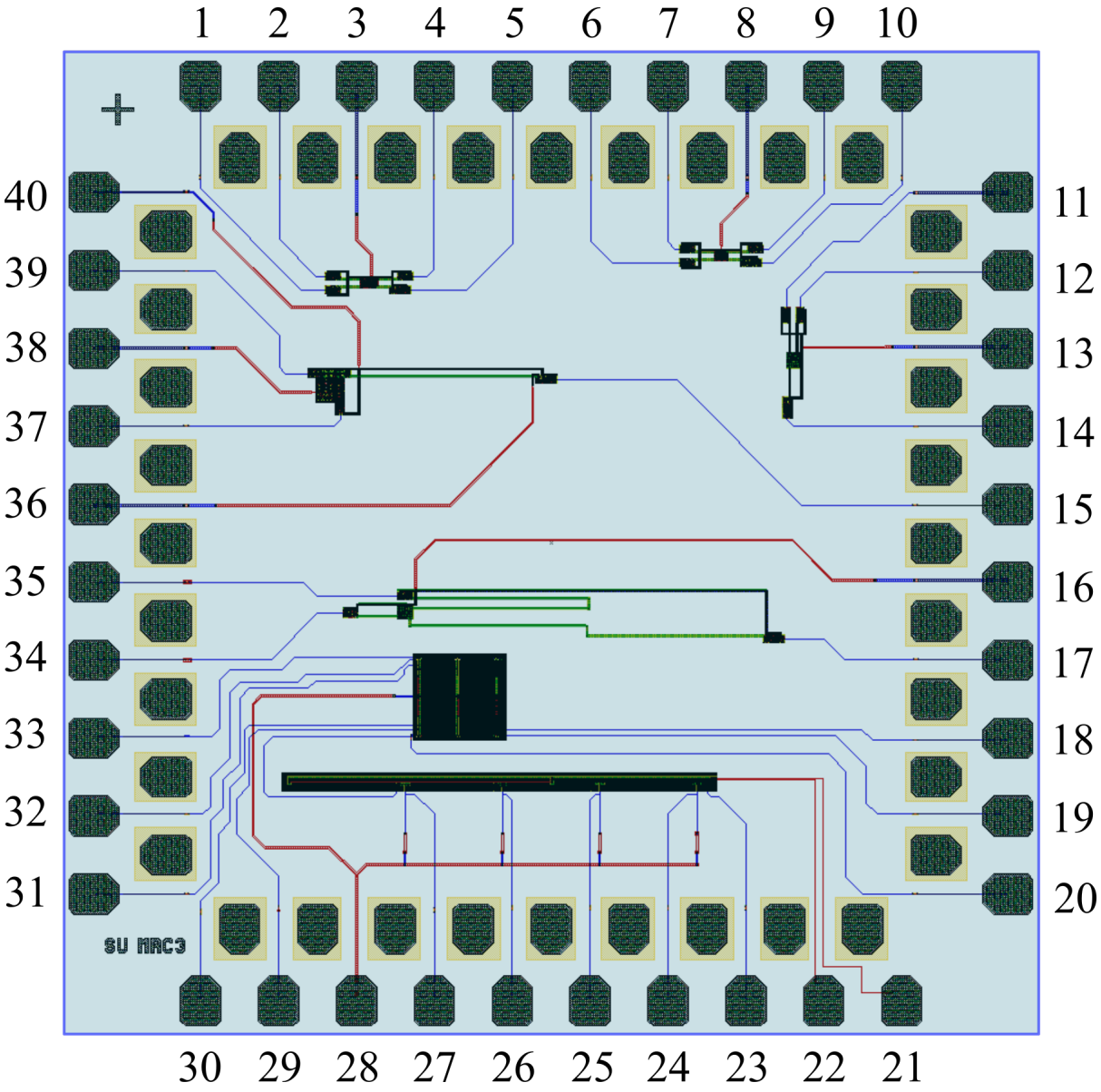

Figure 2.1: GDS layout view of die.

2.2 Pin assignment table

Table 2.1: Chip pin numbers.

Pin	Experiment	Description
1	RSFQ01	Signal input current (0 – 600 µA)
2	RSFQ01	Signal input current (0 – 600 µA)
3	RSFQ01	DC bias: 6.00 mA
4	RSFQ01	Signal input current (0 – 600 µA)
5	RSFQ01	Output voltage: 0 - 100 µV
6	RSFQ02	Signal input current (0 – 600 µA)
7	RSFQ02	Signal input current (0 – 600 µA)
8	RSFQ02	DC bias input: 5.72 mA
9	RSFQ02	Signal input current (0 – 600 µA)
10	RSFQ02	Output voltage: 0 - 100 µV
11	RSFQ03	Signal input current (0 – 600 µA)
12	RSFQ03	Signal input current (0 – 600 µA)
13	RSFQ03	DC bias input: 4.57 mA
14	RSFQ03	Output voltage: 0 - 100 µV
15	RES01	Output voltage: 0 - 100 µV
16	RSFQ04	DC bias input: 4.57 mA
17	RSFQ04	Output voltage: 0 - 100 µV
18	FLUX	
19	FLUX	
20	FLUX	
21	FLUX	
22	FLUX	
23	FLUX	
24	FLUX	
25	FLUX	
26	FLUX	
27	FLUX	
28	FLUX	
29	FLUX	
30	FLUX	
31	FLUX	
32	FLUX	
33	FLUX	
34	RSFQ04	Signal input current (0 – 600 µA)
35	RSFQ04	Signal input current (0 – 600 µA)
36	RES01	Tuning DC bias input: 0.155 mA
37	RES01	Output voltage: 0 - 100 µV
38	RES01	Tuning DC bias input: 3.50 mA
39	RES01	Signal input current (0 – 600 µA)
40	RES01	DC bias input: 6.86 mA

3. Experiments

3.1 RSFQ01: Skyplane-shielded RSFQ cells in magnetic field (low frequency test)

3.1.1 Aim

Test functionality of skyplane-shielded RSFQ cells and obtain magnetic field operating limits. The test circuit is a NDRO with an integrated PTL driver and receiver connected to PTLs.

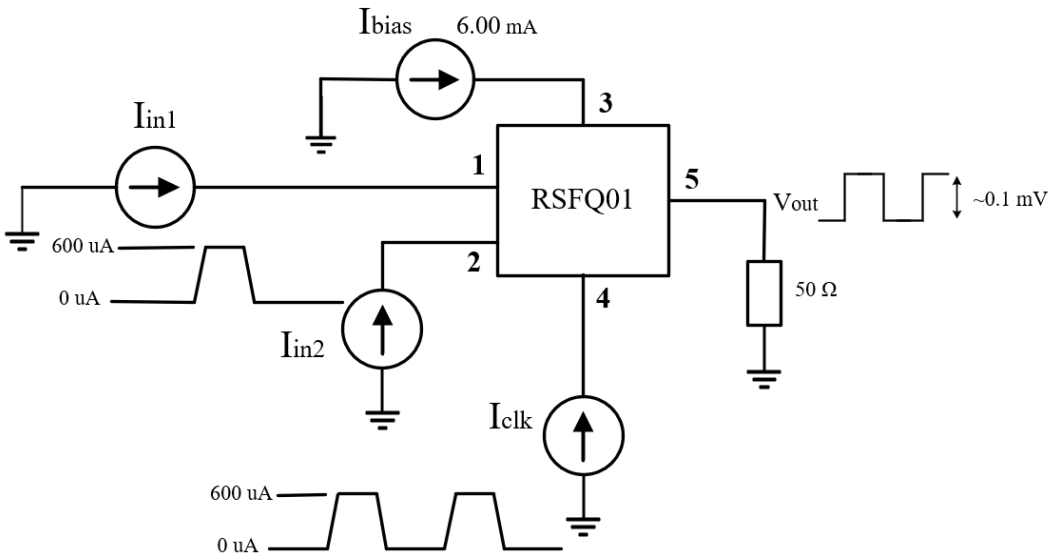

Figure 3.1: Test setup for RSFQ01 that shows required sources, pin numbers and signal shapes.

3.1.2 Pins

Table 3.1: Pin numbers for RSFQ01.

Pin	Description
1	Set signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
2	Reset signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
3	Bias input current: 6.00 mA, with about ±20% margin.
4	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
5	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.1.3 Test sequence

Apply 6.00 mA of bias current to pin 3 to bias the circuit. Apply an input pulse train as a current varying between 0 and 600 µA (adjustable by approximately 20%) to pin 4. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 1. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 2. This is a low frequency test, and a pulse frequency of 1 kHz to 10 kHz will be sufficient for testing purposes. **The upper frequency limit is not known, as it is a function of the test environment and the input line on the die. It may be tested.**

The output voltage at pin 5, measured into a 50 Ω load with amplitude of approximately 100 µV.

Measurements required to adjust simulation tools, models and cell designs.

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 3 in zero magnetic field.
3. Maximum input signal frequency on pin 4 at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

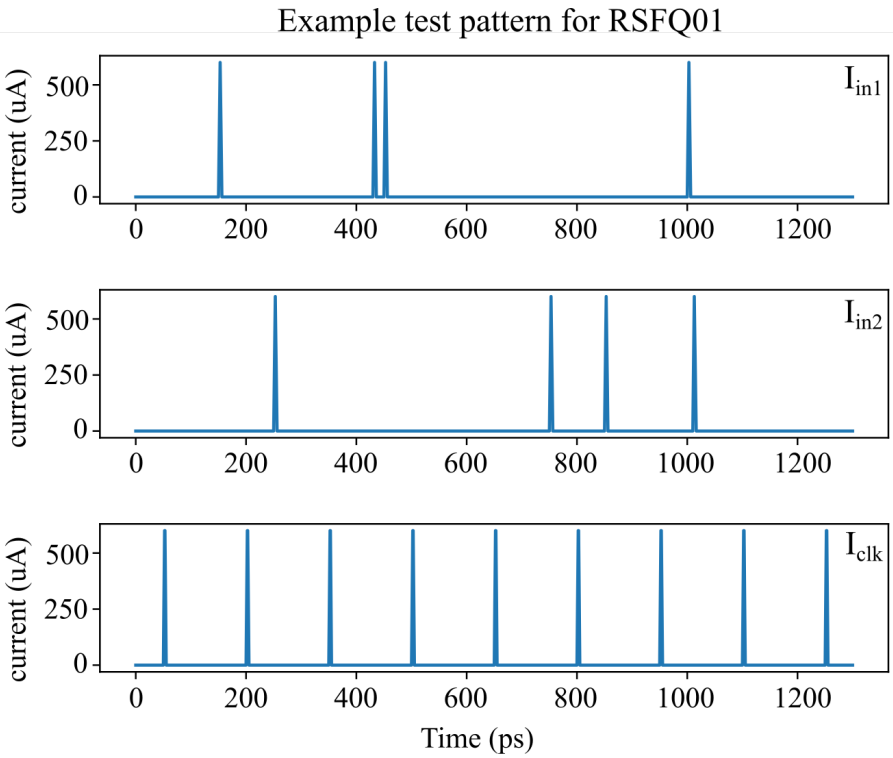

Figure 3.2: Example test pattern for RSFQ01.

3.2 RSFQ02: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.2.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests a XOR with integrated PTL drivers and receivers connected through PTLs to the test bench.

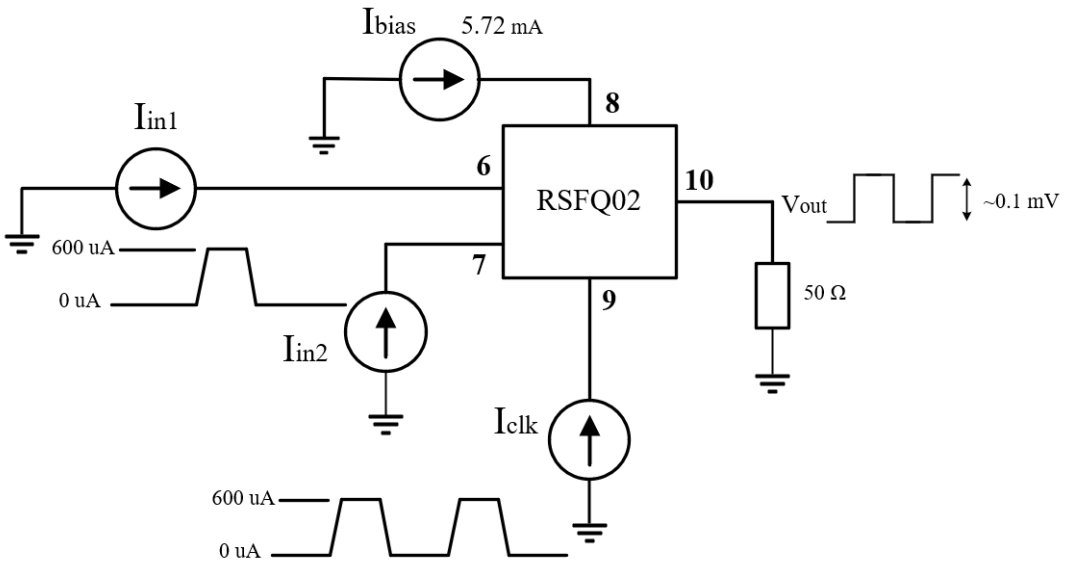

Figure 3.3: Test setup for RSFQ02 that shows required sources, pin numbers and signal shapes.

3.2.2 Pins

Table 3.2: Pin numbers for RSFQ02.

Pin	Description
6	Signal input current A: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
7	Signal input current B: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
8	Bias input current: 5.72 mA, with about ±20% margin.
9	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
10	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.2.3 Test sequence

Apply 5.72 mA of bias current to pin 8 to bias the circuit. Apply an input pulse train as a current varying between 0 and 600 µA (adjustable by approximately 20%) to pin 9. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 6. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 7. This is a low frequency test, and a pulse frequency of 1 kHz to 10 kHz will be sufficient for testing purposes. **The upper frequency limit is not known, as it is a function of the test environment and the input line on the die. It may be tested.**

The output voltage at pin 10, measured into a 50 Ω load with amplitude of approximately 100 µV.

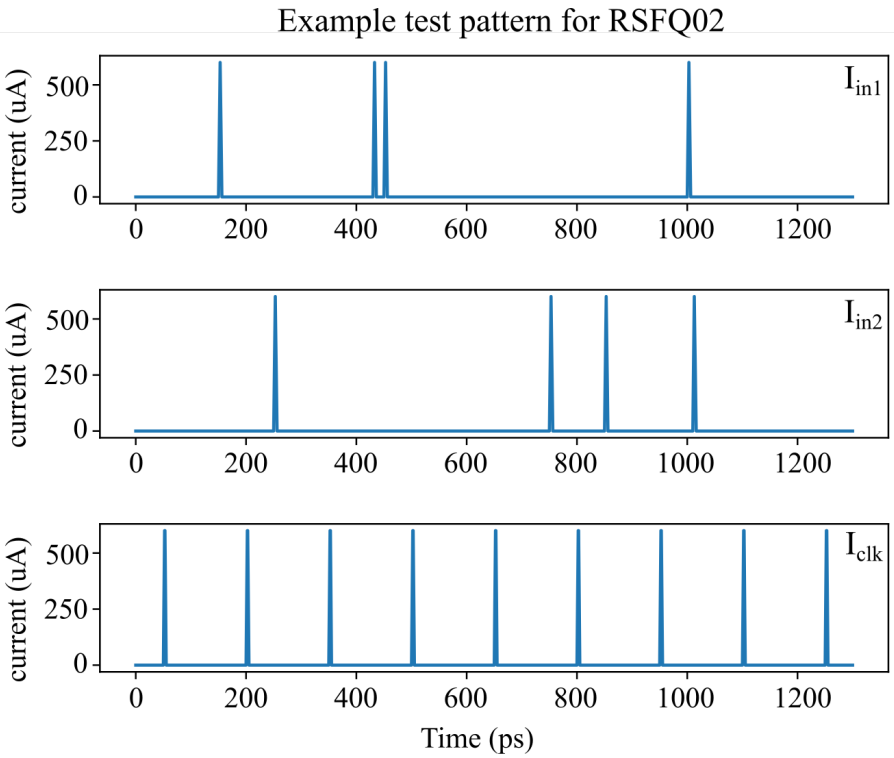

Figure 3.4: Example test pattern for RSFQ02.

Measurements required to adjust simulation tools, models and cell designs.

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 8 in zero magnetic field.
3. Maximum input signal frequency on pin 9 at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.3 RSFQ03: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.3.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuits tests the functionality of a DFF with integrated PTL drivers and receivers with PTL connections.

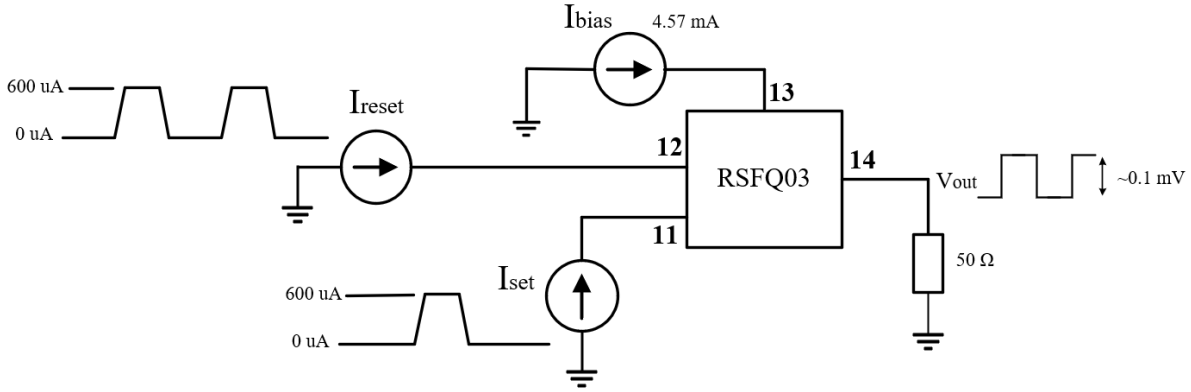

Figure 3.5: Test setup for RSFQ03 that shows required sources, pin numbers and signal shapes.

3.3.2 Pins

Table 3.3: Pin numbers for RSFQ03.

Pin	Description
11	Set signal input current:0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
12	Reset signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
13	Bias input current: 4.57 mA, with about ±20 % margin.
14	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

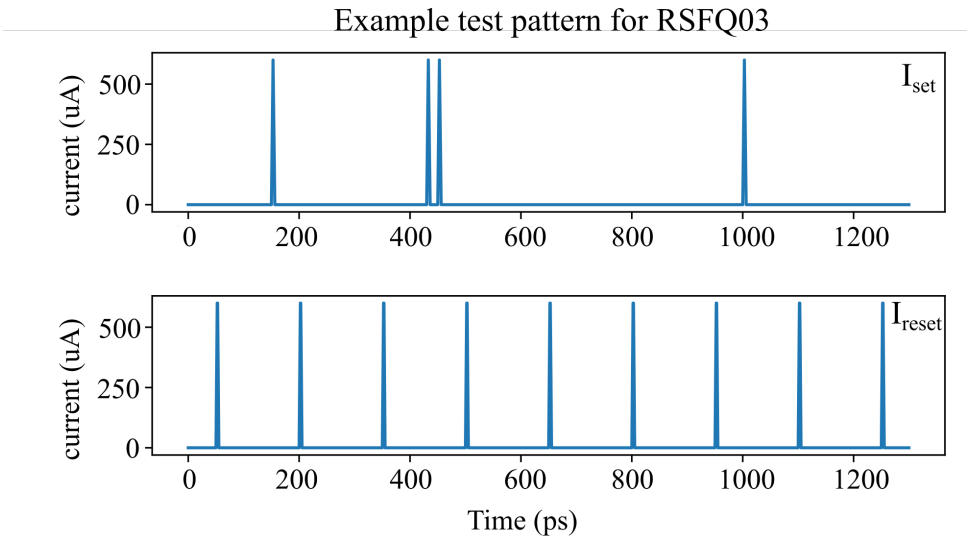

Figure 3.6: Example test pattern for RSFQ03.

3.3.3 Test sequence

Apply 4.57 mA of bias current to pin 13 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 12. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 11. The following test pattern (also illustrated in Fig. 3.6) is required to test all possible instances: no set signal before reset signal arrives, set signal before reset signal arrives, and two set signals before reset signal arrives. The output voltage at pin 14, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 13 in zero magnetic field.
3. Maximum input signal frequency on pin 12 at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.4 RSFQ04: Sky-plane-shielded RSFQ cells in magnetic field (low frequency test)

3.4.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuits tests the functionality of a DFF with integrated PTL drivers and receivers with PTL connections. The test is similar to RSFQ03, but includes PTLs with corners to investigate the effect on circuit functionality.

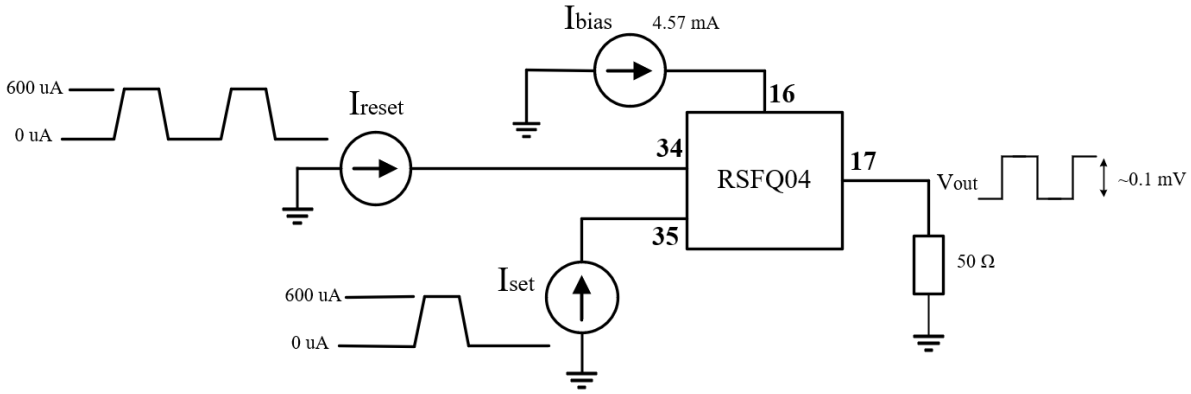

Figure 3.7: Test setup for RSFQ04 that shows required sources, pin numbers and signal shapes.

3.4.2 Pins

Table 3.4: Pin numbers for RSFQ04.

Pin	Description
35	Set signal input current:0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip.
34	Reset signal input current: 0 V for no input, pulsed to approximately 600 µA to create an SFQ pulse on-chip. Pulse train with frequency of around 1 kHz to 10 kHz is recommended.
16	Bias input current: 4.57 mA, with about ±20 % margin.
17	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.4.3 Test sequence

Apply 4.57 mA of bias current to pin 16 to bias the circuit. Apply an input pulse train as a current with 0 – 600 µA amplitude (±20 % range) to pin 34. Apply an input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 35. The following test pattern (also illustrated in Fig. 3.6) is required to test all possible instances: no set signal before reset signal arrives, set signal before reset signal arrives, and two set signals before reset signal arrives. The output voltage at pin 17, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude at zero magnetic field.
2. Bias margins on pin 16 in zero magnetic field.
3. Maximum input signal frequency on pin 34 at zero magnetic field and nominal bias current (even if limited by test equipment).

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

3.5 RES01: Resonance on PTL test

3.5.1 Aim

Test functionality of sky-plane-shielded RSFQ cells and obtain magnetic field operating limits. The circuit tests the functionality of the OR2 cell with integrated PTL drivers and receivers with PTL connections.

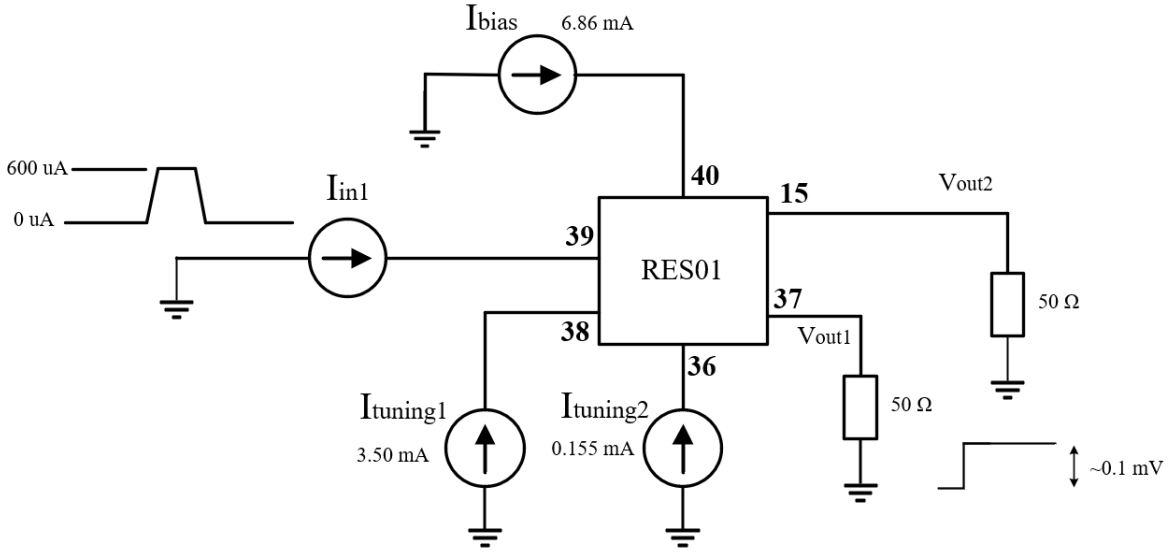

Figure 3.8: Test setup for RES01 that shows required sources, pin numbers and signal shapes.

3.5.2 Pins

Table 3.5: Pin numbers for RES01.

Pin	Description
39	Signal input current: 0 V for no input, pulsed to approximately 600 µA to create a single SFQ pulse on-chip.
40	Bias input current: 6.86 mA, with about ±20 % margin.
38	Tuning Bias input current: 3.50 mA
36	Tuning Bias input current: 0.155 mA
37	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.
15	Output voltage: Approximately 0 – 100 µV (averaged) into a 50 Ω load.

3.5.3 Test sequence

Apply 6.86 mA of bias current to pin 40 to bias the circuit. Apply 3.50 mA of tuning bias current to pin 38. Apply 0.155 mA of tuning bias current to pin 36.

Apply a single input pulse as a current with 0 – 600 µA amplitude (±20 % range) at pin 39. This input pulse feeds the ring oscillator. The output frequency of the ring oscillator is observed at pin 37, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

The circuit output voltage at pin 15, measured into a 50 Ω load. This voltage should vary between approximately 0 V and 100 µV.

Tune the bias current on pin 38 until the output on pin 37 reaches the specified resonant frequency. Confirm output voltage at pin 15. Tune the bias on pin 36 to determine the effect on output pin 15.

Measurements required to adjust simulation tools, models and cell designs

Operational verification:

1. Output voltage amplitude on pin 15 and 37 at zero magnetic field.
2. Bias margins on pin 40 and 36 in zero magnetic field.
3. Bias margins on pin 38 in zero magnetic field.

Magnetic rule checking investigations:

1. Bias margins vs applied magnetic flux density (after cool-down) in x, y and z directions. The flux density can be adjusted in 1 µT increments (positive and negative) until the circuit fails.

Appendix K

User Manual - ColdFlux Logic Cell Library for MIT-LL SFQ Process

- L. Schindler, C. J. Fourie, C. L. Ayala, O. Chen and N. Yoshikawa

The majority of work done on the development and documentation of the RSFQ logic cell library is my own. Part 1 of the documentation is excluded as the work done on the AQFP logic cell library was completed by a team at Yokohama National University and is not within the scope of this research.

IARPA SuperTools Deliverable

ColdFlux Logic Cell Library for MIT-LL SFQ Process

Submitted by

ColdFlux Team
Yokohama National University
Stellenbosch University

Version 2.0

Version History

- **Version 2.0:** This version updates the AQFP and RSFQ logic cell libraries for SuperTools phase 2, and combines both libraries in a single document.
- **Version 1.5:** Previous release of AQFP Logic cell library document.
- **Version 1.1:** Previous release of RSFQ Logic cell library document.

Acknowledgment

The research is based upon work supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via the U.S. Army Research Office grant W911NF-17-1-0120. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the ODNI, IARPA, or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation herein.

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Part II

RSFQ Logic

3. Introduction and Setup

3.1 Introduction

This RSFQ cell library is developed under the IARPA SuperTools/ColdFlux contract via the U.S. Army Research Office grant W911NF-17-1-0120. The aim is to create a generic and open-source cell library with RSFQ logic [9] as part of the IARPA SuperTools Program[10], [11]. The cell library is continually updated and the latest version of the library can always be found at: `https://github.com/sunmagnetics/RSFQlib`. The RSFQ cell library on GitHub does not include the layout files as these files include Government-furnished information (GFI).

The free and open-source tools *XIC* [12], *JoSIM* [13], [14], *JoSIM-tools* [15], *KLayout* and *TimEx* [16], [17] is used to develop and test the RSFQ cells. The circuit schematics are drawn using *XIC*. *JoSIM* is used as the SPICE engine for simulating the cells, while *JoSIM-tools* is used for operating margin analysis as well as cell parameter optimization. *KLayout* is used to construct the cell layouts. *TimEx* is used to extracted the characteristics of the cell to generate the Mealy Finite State Machine diagram and Verilog files. Additionally, *InductEx* [3], [18] is used for impedance extraction during cell layout design. A free version of InductEx is available, but has limited capacity.

The RSFQ cell library is currently designed to only be connected using Passive Transmission Lines (PTLs). The cells are designed with integrated PTL transmitters and receivers to minimize complexity and surface area required on a chip. Separate PTL transmitters and receivers are therefore no longer necessary when connecting the cells to PTLs. To indicate the integration of PTL transmitters and receivers within a cell, the letter 'T' is added at the end of a cell name, for example the DFF with integrated PTL transmitters and receivers will be referred to as DFFT.

The following core cells are included in the RSFQ cell library:

- Interconnects: JTLT, SPLITT, MERGET, PTLTX and PTLRX.
- Logic cells: AND2T, OR2T, XORT and NOTT.
- Buffers: DFFT, NDROT, BUFF and BUFFT.
- Interfacing cells: DCSFQ, DCSFQ-PTLTX, PTLRX-SFQDC and SFQDC.

More complex functions can be constructed through connecting several core cells. Versions of each cell without integrated PTL transmitters and receivers are also in

development. The cells are currently optimized to run at a maximum clock frequency of 50 GHz.

Each delivered cell is documented in 5 parts:

1. **Schematic:** The schematic of a cell is constructed using *Xic* and is delivered in the native *Xic* format.
2. **Layout:**
   (a) The physical layout of the cells can be constructed using *Xic* or *KLayout* and is delivered in standard GDSII format.
   (b) The *InductEx* extraction is also included.
3. **Analog model:**
   (a) **Netlist:** The netlist presents the device-level construction of a circuit. The netlist can be generated and adapted from the schematic file using *Xic* or can be constructed by hand.
   (b) **Pin list:** The pin labels and function of each pin is listed.
   (c) **Simulation results:** JoSIM is used for all circuit simulations.
4. **Digital model:**
   (a) **Verilog model:** The behavior-level model of a cell with timing specifications included within the model. All verilog models are extracted using *TimEx* and is delivered in standard HDL Verilog format.
   (b) **Simulation results:** The digital simulation testbench is generated through *TimEx* and is run using *Icarus Verilog* and wave viewer *GTKWave*. Each edge event indicated an SFQ pulse.
   (c) **Mealy finite state machine diagram:** The state machine diagram is extracted using *TimEx* and is delivered in standard PDF format.
5. **Power consumption:** The power consumption of each cell is calculated in terms of static and dynamic power consumption. Following [19], dynamic power consumption can be calculated as $P_d = f\Phi_0 I_c$ and static power consumption can be calculated as $P_s = I_b V_b$.

3.2 Setup

The latest version of the RSFQ cell library can be found at: `https://github.com/sunmagnetics/RSFQlib`. The RSFQ cell library is simulated and tested using several free and/or open-source tools:

- *Xic* is part of *XicTools* and can be found at `http://www.wrcad.com/xic.html`.
- *JoSIM* can be found at `https://github.com/JoeyDelp/JoSIM/`.
- *JoSIM-tools* can be found at `https://github.com/pleroux0/josim-tools`.
- *TimEx* can be found at `https://github.com/sunmagnetics/TimEx`.
- *KLayout* can be found at `https://www.klayout.de/`.
- *InductEx* can be found at `https://www.inductex.info`.
- *Icarus Verilog* can be found at `http://iverilog.icarus.com/`.
- *GTKWave* can be found at `http://gtkwave.sourceforge.net/`.

No additional setup is required to use the RSFQ cell library.

3.3 License

The generic RSFQ cell library, excluding the cell layouts, is free to distribute and/or modify under the terms of the MIT license.

4. RSFQ Cell Library

4.1 Interconnects

4.1.1 JTLT

The JTLT, Josephson transmission line, cell is commonly used to reestablish and propagate RSFQ pulses when long PTL connections are required. The cell has integrated PTL transmitters and receivers and is meant to connect directly to a PTL.

Schematic

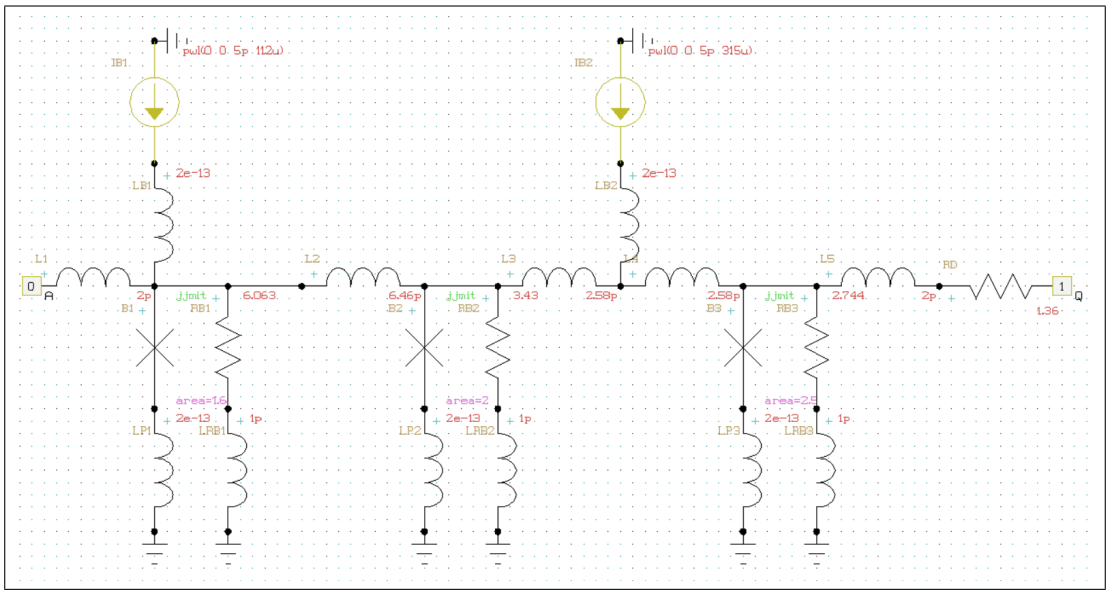

Figure 4.1: Schematic of RSFQ JTLT.

Layout

The physical layout for the RSFQ JTLT is shown in Fig. 4.2 and the resulting InductEx extraction is shown in Listing 4.1. The layout height is 70 μm and the width is 40 μm.

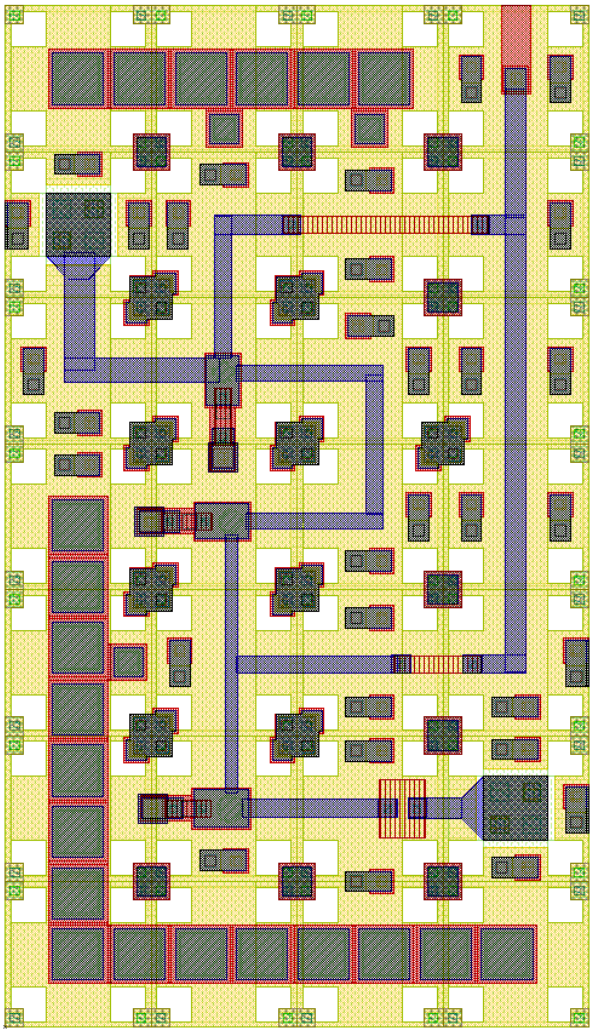

Figure 4.2: RSFQ JTLT Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_JTLT_v1p5.GDS -n LSmitll_JTLT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_JTLT_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
Total fundamental loops identified in netlist = 6
Using TetraHenry with analytical integration.
1188 structures read. Reduced 1188 objects to 1118 polygons and 4 terminals.
Top level structure is "LSMITLL_JTLT_V1P5".
GDS file LSmitll_JTLT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 7; Labels = 7; Extracted Ports = 7

Port                  Positive terminal    Negative terminal
P1                    M6,   line along x;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 5.061; unknowns = 20; rank = 20.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          2.89322E-12 --          --          +2.8932E-12 --%
L2        6.46E-12    6.4667E-12  --          --          +6.7015E-15 +0.10374%
L3        2.58E-12    2.57146E-12 --          --          -8.5375E-15 -0.33091%
L4        2.58E-12    2.56823E-12 --          --          -1.1774E-14 -0.45635%
L5        --          2.39515E-12 --          --          +2.3951E-12 --%
LB1       --          3.21204E-12 --          --          +3.212E-12  --%
LB2       --          2.8367E-12  --          --          +2.8367E-12 --%
LP1       --          5.39345E-13 --          --          +5.3934E-13 --%
LP2       --          5.44485E-13 --          --          +5.4448E-13 --%
LP3       --          5.08968E-13 --          --          +5.0897E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.00016     0.00017055
J2        0.0002      0.00020853
J3        0.00025     0.00025893

Error bound on extracted values: 0.792036%

Deallocating memory.
Cycles found in 0.027 seconds.
SVD solution in 0.014 seconds.
Job finished in 113.946 seconds.
```

Listing 4.1: RSFQ JTLT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                              a q
.subckt LSMITLL_JTLT a q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param Phi0=2.067833848E-15
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param LP=0.2p
.param ICreceive=1.6
.param ICtrans=2.5
.param Lptl=2p
.param LB=2p
.param BiasCoef=0.7
.param RD=1.36
.param B1=ICreceive
.param B2=ICtrans/1.25
.param B3=ICtrans
.param IB1=B1*Ic0*BiasCoef
.param IB2=(B2+B3)*Ic0*BiasCoef
.param L1=Lptl
.param L2=Phi0/(2*B1*Ic0)
.param L3=(Phi0/(2*B2*Ic0))/2
.param L4=L3
.param L5=Lptl
.param LP1=LP
.param LP2=LP
.param LP3=LP
.param LB1=LB
.param LB2=LB
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param LRB1=(RB1/Rsheet)*Lsheet+LP
.param LRB2=(RB2/Rsheet)*Lsheet+LP
.param LRB3=(RB3/Rsheet)*Lsheet+LP
B1          6           7           jjmit area=B1
B2          9           10          jjmit area=B2
B3          12          13          jjmit area=B3
IB1         0           18         pwl(0       0 5p IB1)
IB2         0           19         pwl(0       0 5p IB2)
L1          a           6           L1
L2          6           9           L2
L3          9           16          L3
L4          16          12          L4
L5          12          17          L5
LB1         6           18          LB1
LB2         16          19          LB2
LP1         0           7           LP1
LP2         0           10          LP2
LP3         0           13          LP3
LRB1        0           8           LRB1
LRB2        0           11          LRB2
LRB3        0           14          LRB3
RB1         8           6           RB1
RB2         11          9           RB2
RB3         14          12          RB3
RD          17          q           RD
.ends
```

Listing 4.2: RSFQ JTLT JoSIM netlist.

Table 4.1: RSFQ JTLT pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ JTLT using JoSIM is shown in Fig. 4.3. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected via a PTL to the JTLT.

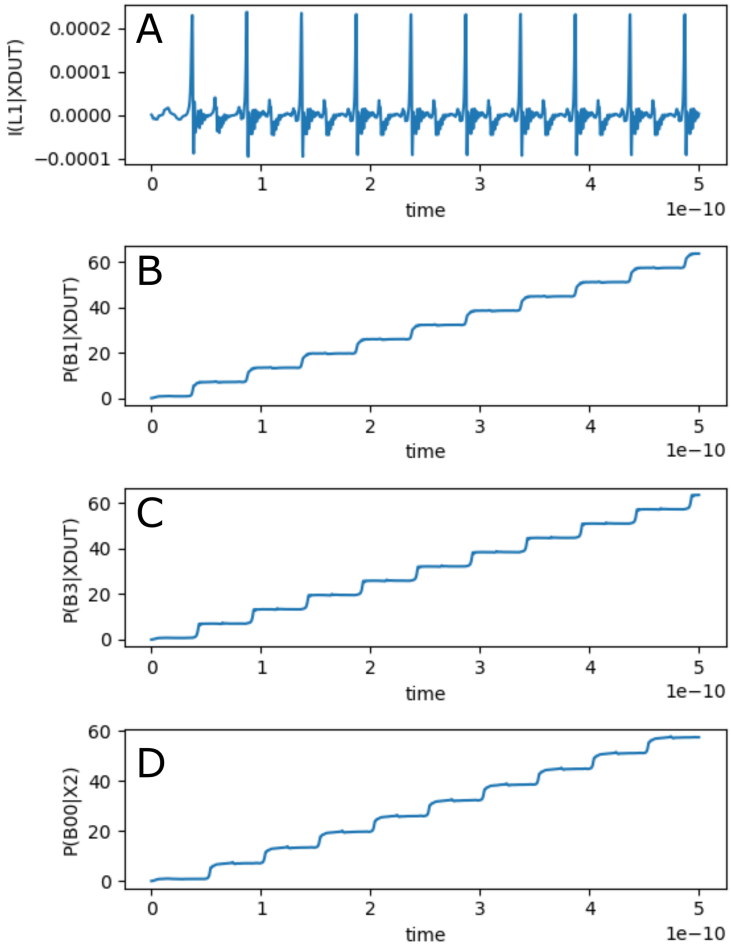

Figure 4.3: RSFQ JTLT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_JTLT_v1p5 (a, q);

input
  a;

output
  q;

reg
  q;

real
  delay_state0_a_q = 5.5,
  ct_state0_a_a = 6.6;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end

endmodule
```

Listing 4.3: RSFQ JTLT verilog model.

The digital simulation results for the RSFQ JTLT is shown in Fig. 4.4 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.5.

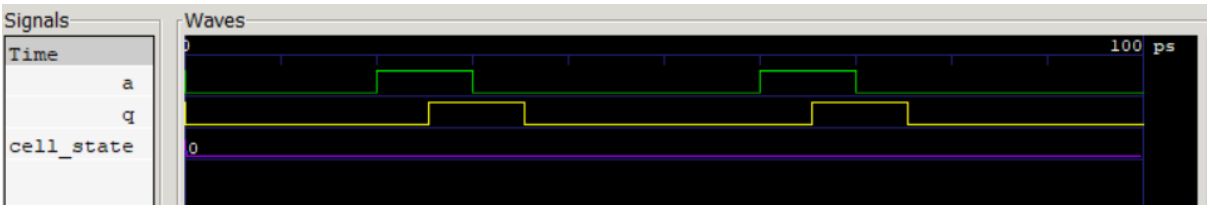

Figure 4.4: RSFQ JTLT digital simulation results.

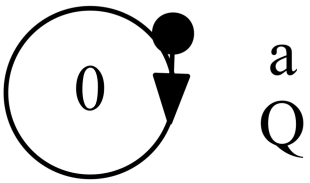

Figure 4.5: RSFQ JTLT Mealy finite state machine diagram.

Power Consumption

Table 4.2: RSFQ JTLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	111	1.26
2	111	2.52
5	111	6.31
10	111	12.6
20	111	25.2
50	111	63.1

4.1.2 SPLITT

The SPLITT cell is used to split a single pulse signal line into two duplicate output pulse signal lines. The cell has integrated PTL transmitters and receivers and is meant to connect directly to a PTL.

Schematic

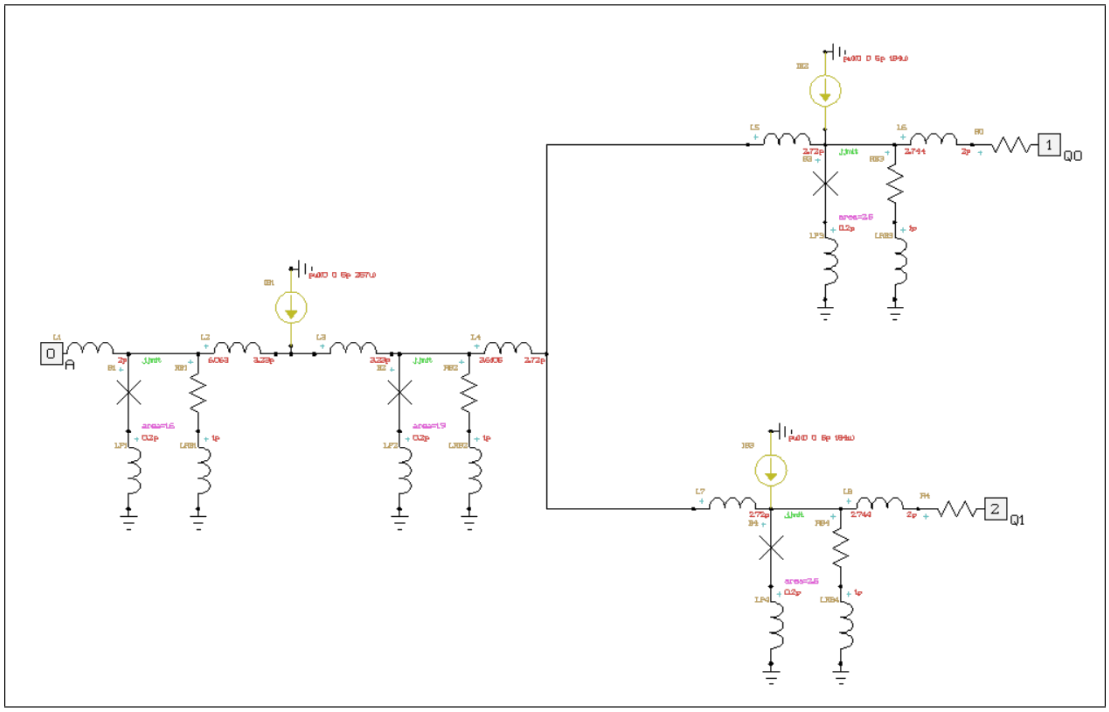

Figure 4.6: Schematic of RSFQ SPLITT.

Layout

The physical layout for the RSFQ SPLITT is shown in Fig. 4.7 and the resulting InductEx extraction is shown in Listing 4.4. The layout height is 70 μm and the width is 50 μm.

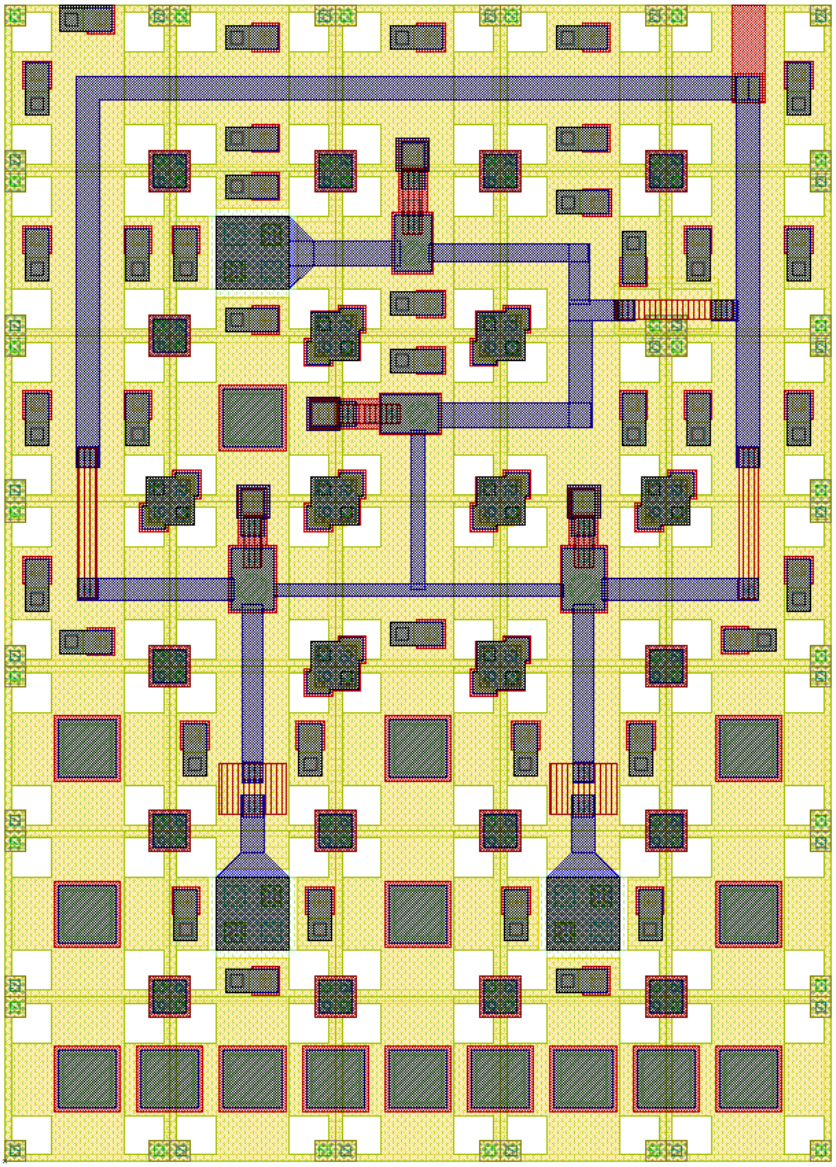

Figure 4.7: RSFQ SPLITT layout.

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_SPLITT_v1p5.gds -n LSmitll_SPLITT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_SPLITT_v1p5_idx.cir read. Totals: L = 15, k = 0, P = 10.
Total fundamental loops identified in netlist = 9
Using TetraHenry with analytical integration.
1379 structures read. Reduced 1379 objects to 1346 polygons and 6 terminals.
Top level structure is "LSMITLL_SPLITT_V1P5".
GDS file LSmitll_SPLITT_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Terminal blocks = 10; Labels = 10; Extracted Ports = 10

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along x;  M4,   same as "+" terminal.
P3                    M6,   line along x;  M4,   same as "+" terminal.
PB1                   M6,   line along y;  M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 8.562; unknowns = 30; rank = 30.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name       Design      Extracted   Design      Extracted   (L only)    (L only)
L1         --          1.50149E-12 --          --          +1.5015E-12 --%
L2         2.84E-12    2.82215E-12 --          --          -1.7855E-14 -0.62869%
L3         2.84E-12    2.83155E-12 --          --          -8.4487E-15 -0.29749%
L4         2.69E-12    2.68895E-12 --          --          -1.0457E-15 -0.038873%
L5         2.69E-12    2.69743E-12 --          --          +7.4322E-15 +0.27629%
L6         --          2.36538E-12 --          --          +2.3654E-12 --%
L7         2.69E-12    2.69634E-12 --          --          +6.3413E-15 +0.23573%
L8         --          2.36586E-12 --          --          +2.3659E-12 --%
LP1        --          4.58145E-13 --          --          +4.5814E-13 --%
LP2        --          5.30306E-13 --          --          +5.3031E-13 --%
LP3        --          4.94587E-13 --          --          +4.9459E-13 --%
LP4        --          4.93676E-13 --          --          +4.9368E-13 --%
LB1        --          6.25411E-13 --          --          +6.2541E-13 --%
LB2        --          2.15533E-12 --          --          +2.1553E-12 --%
LB3        --          2.12844E-12 --          --          +2.1284E-12 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         0.00016     0.00016855
J2         0.000167    0.00017455
J3         0.00025     0.00025893
J4         0.00025     0.00025893

Error bound on extracted values: 1.17944%

Deallocating memory.
Cycles found in 0.030 seconds.
SVD solution in 0.013 seconds.
Job finished in 150.310 seconds.
```

Listing 4.4: RSFQ SPLITT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                          a q0 q1
.subckt LSMITLL_SPLITT a q0 q1
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param Phi0=2.067833848E-15
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param LP=0.2p
.param IC=1.9
.param ICreceive=1.6
.param ICtrans=2.5
.param Lptl=2p
.param BiasCoef=0.735
.param RD=1.36
.param B1=ICreceive
.param B2=IC
.param B3=ICtrans
.param B4=ICtrans
.param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
.param IB2=BiasCoef*(B3*Ic0)
.param IB3=BiasCoef*(B4*Ic0)
.param L1=Lptl
.param L2=(Phi0/(2*B1*Ic0))/2
.param L3=(Phi0/(2*B1*Ic0))/2
.param L4=(Phi0/(2*B2*Ic0))/2
.param L5=(Phi0/(2*B2*Ic0))/2
.param L6=Lptl
.param L7=(Phi0/(2*B2*Ic0))/2
.param L8=Lptl
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param LRB1=(RB1/Rsheet)*Lsheet
.param LRB2=(RB2/Rsheet)*Lsheet
.param LRB3=(RB3/Rsheet)*Lsheet
.param LRB4=(RB4/Rsheet)*Lsheet
IB1 0 4 pwl(0 0 5p IB1)
IB2 0 8 pwl(0 0 5p IB2)
IB3 0 11 pwl(0 0 5p IB3)
B1 2 3 jjmit area=B1
B2 5 6 jjmit area=B2
B3 8 9 jjmit area=B3
B4 11 12 jjmit area=B4
L1 a 2 L1
L2 2 4 L2
L3 4 5 L3
L4 5 7 L4
L5 7 8 L5
L6 8 10 L6
L7 7 11 L7
L8 11 13 L8
LP1 3 0 0.2p
LP2 6 0 0.2p
LP3 9 0 0.2p
LP4 12 0 0.2p
RB1 2 102 RB1
LRB1 102 0 LRB1
RB2 5 105 RB2
```

```
68 LRB2 105 0 LRB2
69 RB3 8 108 RB3
70 LRB3 108 0 LRB3
71 RB4 11 111 RB4
72 LRB4 111 0 LRB4
73 RD1 13 q0 RD
74 RD2 10 q1 RD
75 .ends
```

Listing 4.5: RSFQ SPLITT JoSIM netlist.

Table 4.3: RSFQ SPLITT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ SPLITT are shown in Fig. 4.8. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q0**,

(d) the phase over the output JJ of pin **q1**,

(e) the phase over the input JJ of the load cell connected to pin q0 through a PTL, and

(f) the phase over the input JJ of the load cell connected to pin q1 through a PTL.

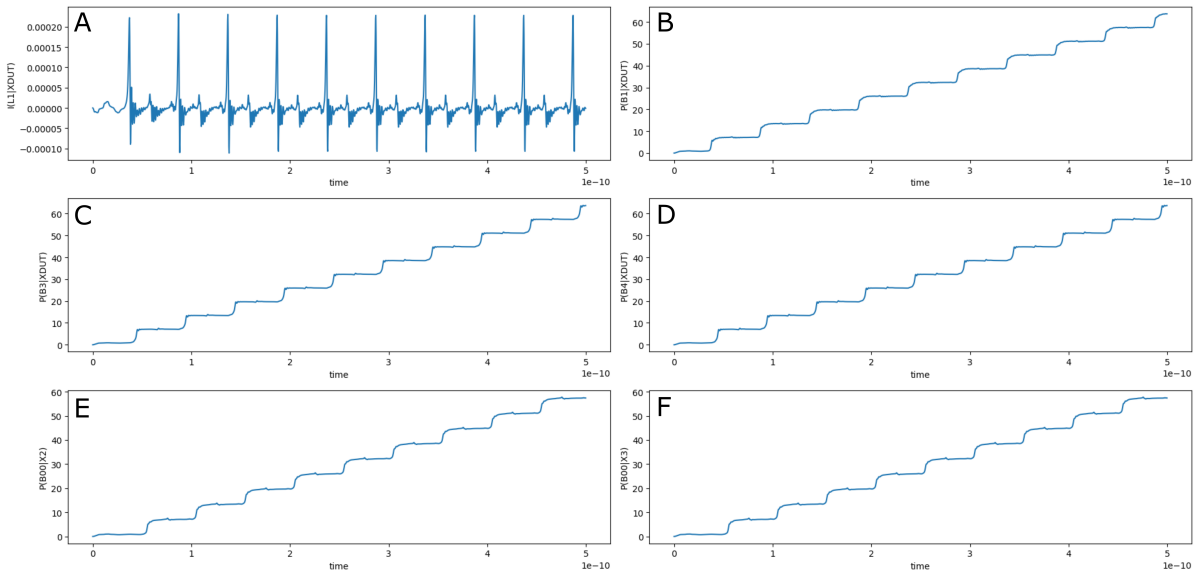

Figure 4.8: RSFQ SPLITT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_SPLITT_v1p5 (a, q0, q1);

input
  a;
output
  q0, q1;
reg
  q0, q1;
real
  delay_state0_a_q0 = 7.0,
  delay_state0_a_q1 = 7.0,
  ct_state0_a_a = 10.3;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q0 = 0; // All outputs start at 0
      q1 = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q0 <= 1'bX;  // Set all outputs to unknown
                  q1 <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q0 <= #(delay_state0_a_q0) !q0;
                           q1 <= #(delay_state0_a_q1) !q1;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end
endmodule
```

Listing 4.6: RSFQ SPLITT verilog model.

The digital simulation results for the RSFQ SPLITT is shown in Fig. 4.9 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.10.

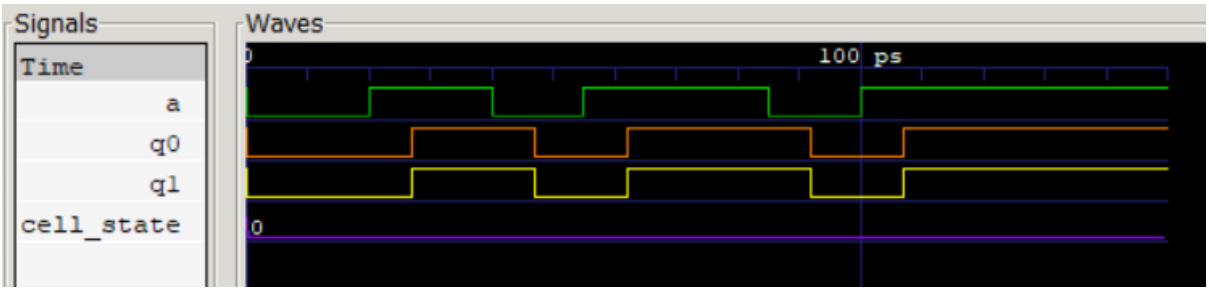

Figure 4.9: RSFQ SPLITT digital simulation results.

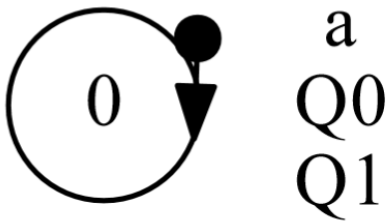

Figure 4.10: RSFQ SPLITT Mealy finite state diagram.

Power consumption

Table 4.4: RSFQ SPLITT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	162	1.76
2	162	3.52
5	162	8.79
10	162	17.6
20	162	35.2
50	162	87.9

4.1.3 CLKSPLT

The CLKSPLT cell is a splitter cell used for clock splitting. It is designed to have the same a-to-q delay as the CLKSPLTT, BUFF and BUFFT cell. The CLKSPLT does not have integrated PTL transmitters and receivers and connecting the cell directly to a PTL is not recommended.

Schematic

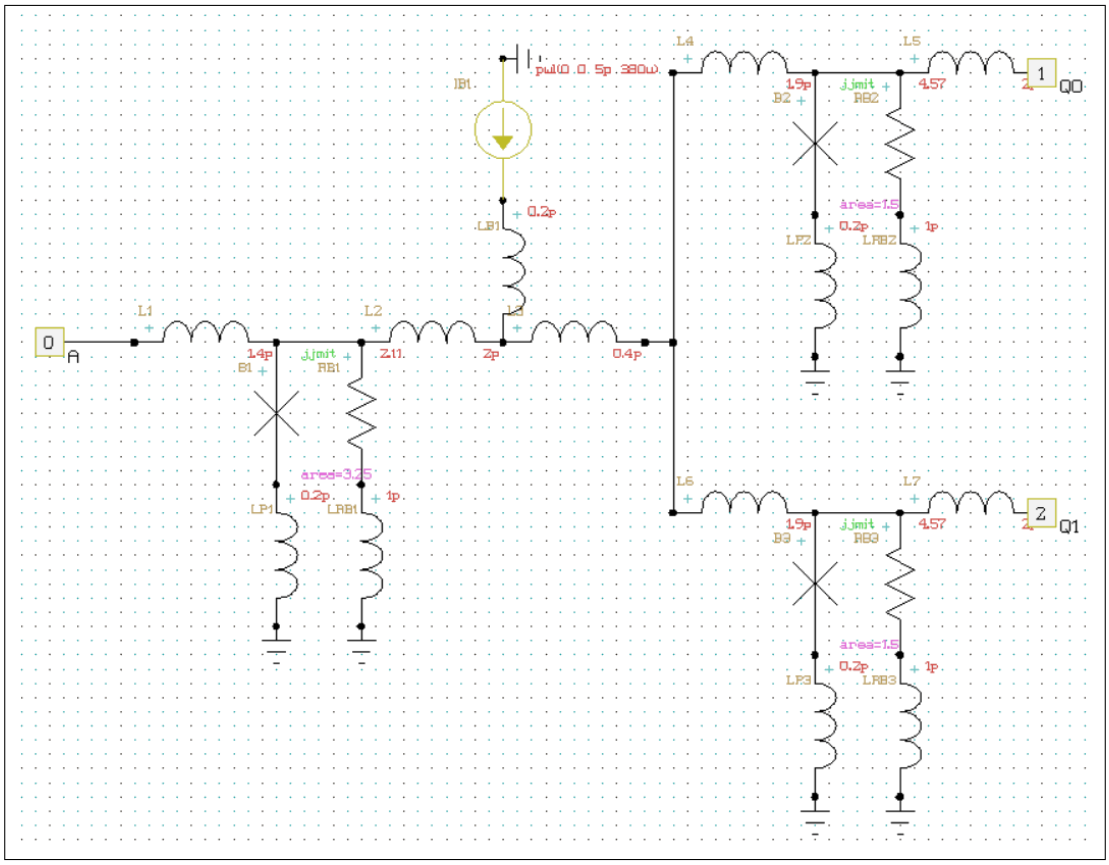

Figure 4.11: Schematic of RSFQ CLKSPLT.

Layout

The physical layout of the RSFQ CLKSPLT is shown in Fig. 4.12 and the resulting InductEx extraction is shown in Listing 4.7. The height of the layout is 70 μm and the width is 50 μm. If required, an additional and smaller layout can be made to minimize chip space for clock splitting.

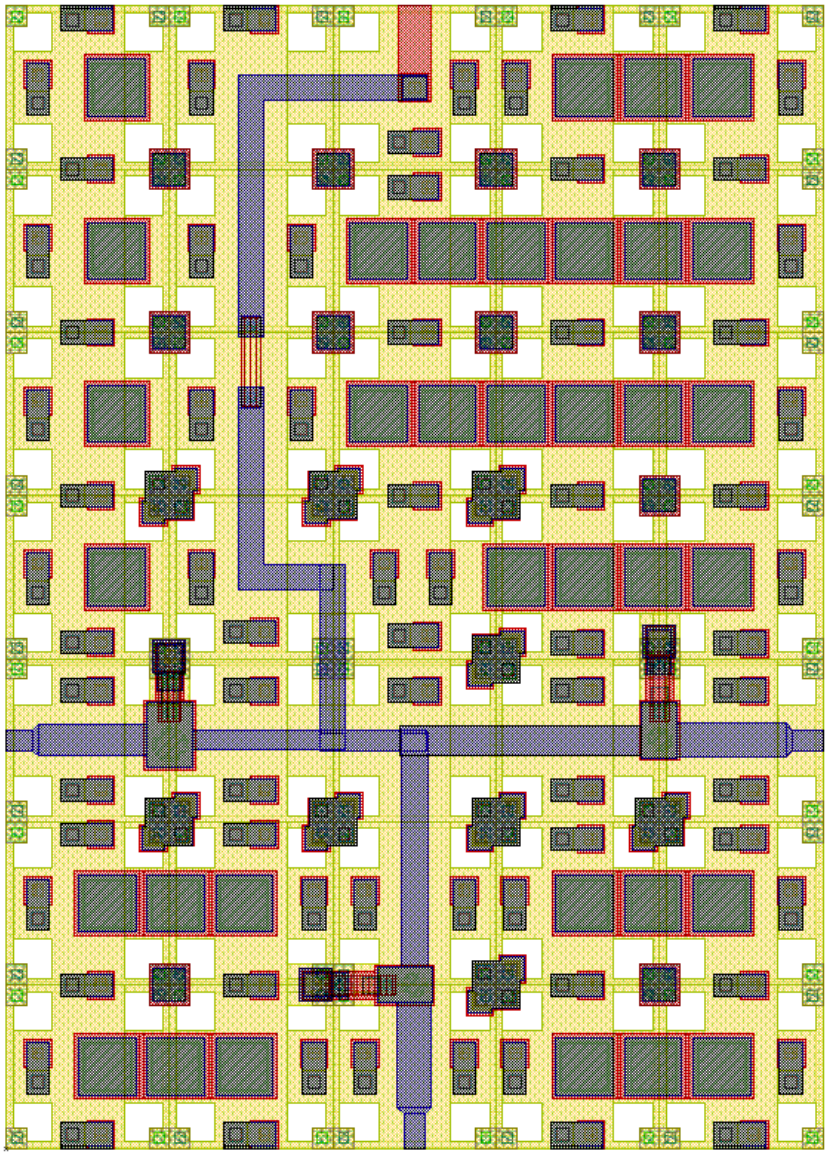

Figure 4.12: RSFQ CLKSPLT layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_CLKSPLT_v1p5p1.GDS -n LSmitll_CLKSPLT_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_CLKSPLT_idx.cir read. Totals: L = 11, k = 0, P = 7.
Total fundamental loops identified in netlist = 6
Using TetraHenry with analytical integration.
1653 structures read. Reduced 1653 objects to 1519 polygons and 4 terminals.
Top level structure is "LSMITLL_CLKSPLT_V1P5P1".
GDS file LSmitll_CLKSPLT_v1p5p1.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 7; Labels = 7; Extracted Ports = 7

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
P3                    M6,   line along x;  M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 7.934; unknowns = 22; rank = 22.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        2E-12       2.00245E-12 --          --          +2.4493E-15 +0.12246%
L2        2E-12       1.99792E-12 --          --          -2.0779E-15 -0.10389%
L3        1E-12       1.00373E-12 --          --          +3.7267E-15 +0.37267%
L4        2.3E-12     2.3219E-12  --          --          +2.1899E-14 +0.95214%
L5        2E-12       1.98942E-12 --          --          -1.0584E-14 -0.5292%
L6        2.3E-12     2.33197E-12 --          --          +3.1972E-14 +1.3901%
L7        2E-12       1.98418E-12 --          --          -1.5819E-14 -0.79093%
LP1       --          4.39941E-13 --          --          +4.3994E-13 --%
LP2       --          5.03617E-13 --          --          +5.0362E-13 --%
LP3       --          5.10561E-13 --          --          +5.1056E-13 --%
LB1       --          4.67421E-12 --          --          +4.6742E-12 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000325    0.00033376
J2        0.00015     0.00015829
J3        0.00015     0.00015829

Error bound on extracted values: 0.0925697%

Deallocating memory.
Cycles found in 0.027 seconds.
SVD solution in 0.015 seconds.
Job finished in 154.433 seconds.
```

Listing 4.7: RSFQ CLKSPLT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 24 June 2020
* Last modification by: L. Schindler

*$Ports                              a q0 q1
.subckt LSMITLL_CLKSPLT a q0 q1
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01rx1=1.01
.param B01tx1=1.70
.param B1=1.70
.param B2=1.21
.param IB01rx1=0.000135
.param IB01tx1=7.6e-05
.param IB1=0.000360
.param L01rx1=2.6757035519114777e-13
.param L02tx1=2.2253212527851025e-12
.param L1=1.5258529970572481e-12
.param L2=2.9153847294043574e-12
.param L3=4.813688043861165e-13
.param L4=1.2716425006912427e-12
.param L5=1.2572241510058017e-12
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB1=(RB1/Rsheet)*Lsheet
.param LRB2=(RB2/Rsheet)*Lsheet
.param RB01rx1=B0Rs/B01rx1
.param RB01tx1=B0Rs/B01tx1
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
B01rx1 6 20 jjmit area=B01rx1
B01tx1 5 16 jjmit area=B01tx1
B01tx2 9 28 jjmit area=B01tx1
B1 7 22  jjmit area=B1
B2 4 14  jjmit area=B2
B3 8 25  jjmit area=B2
IB01rx1 0 12 pwl(0 0 5p IB01rx1)
IB01tx1 0 10 pwl(0 0 5p IB01tx1)
IB01tx2 0 27 pwl(0 0 5p IB01tx1)
IB1 0 13 pwl(0 0 5p IB1)
L01rx1 a 6 L01rx1
L02tx1 5 q0 L02tx1
L02tx2 9 q1 L02tx1
L1 6 7 L1
L2 7 18 L2
L3 18 19 L3
L4 4 19 L4
L5 4 5 L5
L6 19 8 L4
L7 8 9 L5
LP01rx1 20 0 0.34p
LP01tx1 16 0 0.05p
LP01tx2 28 0 0.05p
LP1 22 0 0.2p
LP2 14 0 0.2p
LP3 25 0 0.2p
LPR01rx1 12 6 0.2p
LPR01tx1 10 5 0.2p
LPR01tx2 9 27 0.2p
LPRIB1 13 18 0.2p
LRB01rx1 21 0 LRB01rx1
```

```
68 LRB01tx1 17 0 LRB01tx1
69 LRB01tx2 29 0 LRB01tx1
70 LRB1 23 0 LRB1
71 LRB2 15 0 LRB2
72 LRB3 26 0 LRB2
73 RB01rx1 6 21 RB01rx1
74 RB01tx1 5 17 RB01tx1
75 RB01tx2 9 29 RB01tx1
76 RB1 7 23 RB1
77 RB2 4 15 RB2
78 RB3 8 26 RB2
79 .ends
```

Listing 4.8: RSFQ CLKSPLT JoSIM netlist.

Table 4.5: RSFQ CLKSPLT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ CLKSPLT are shown in Fig. 4.13. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q0**,

(d) the phase over the output JJ of pin **q1**,

(e) the phase over the input JJ of the load cell connected to pin q0, and

(f) the phase over the input JJ of the load cell connected to pin q1.

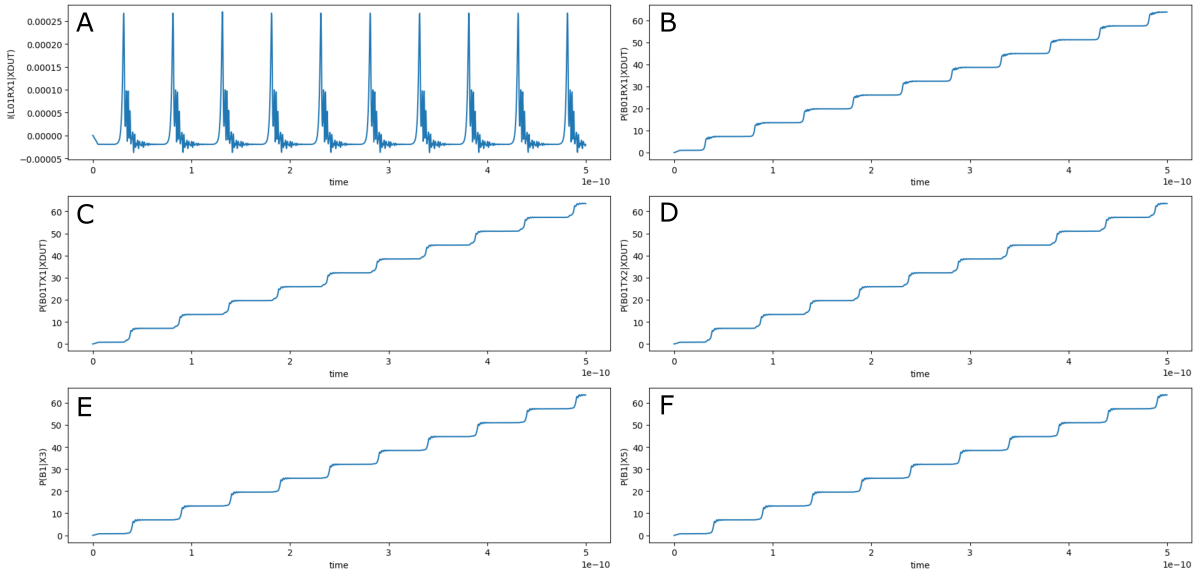

Figure 4.13: RSFQ CLKSPLT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_CLKSPLT_v1p5 (a, q0, q1);

input
  a;
output
  q0, q1;
reg
  q0, q1;

real
  delay_state0_a_q0 = 5.5,
  delay_state0_a_q1 = 5.5,
  ct_state0_a_a = 3.5;
reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q0 = 0; // All outputs start at 0
      q1 = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q0 <= 1'bX;  // Set all outputs to unknown
                  q1 <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q0 <= #(delay_state0_a_q0) !q0;
                           q1 <= #(delay_state0_a_q1) !q1;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end
endmodule
```

Listing 4.9: RSFQ CLKSPLT verilog model.

The digital simulation results for the RSFQ CLKSPLT is shown in Fig. 4.14 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.15.

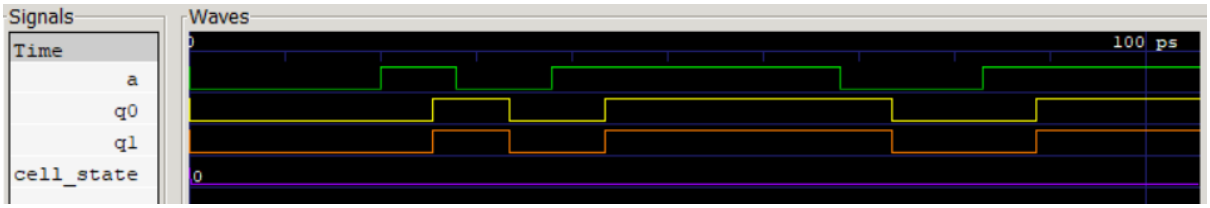

Figure 4.14: RSFQ CLKSPLT digital simulation results.

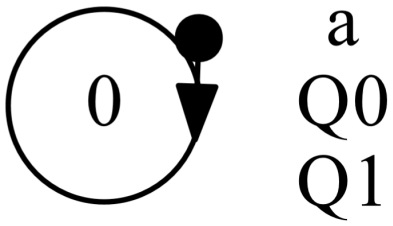

Figure 4.15: RSFQ CLKSPLT Mealy finite state diagram.

Power consumption

Table 4.6: RSFQ CLKSPLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	168	1.76
2	168	3.53
5	168	8.82
10	168	17.6
20	168	35.3
50	168	88.2

4.1.4 CLKSPLTT

The CLKSPLTT cell is a splitter cell used for clock splitting. It is designed to have the same a-to-q delay as the CLKSPLT, BUFF and BUFFT cell. The CLKSPLTT has integrated PTL transmitters and receivers is designed to be directly connected to a PTL.

Schematic

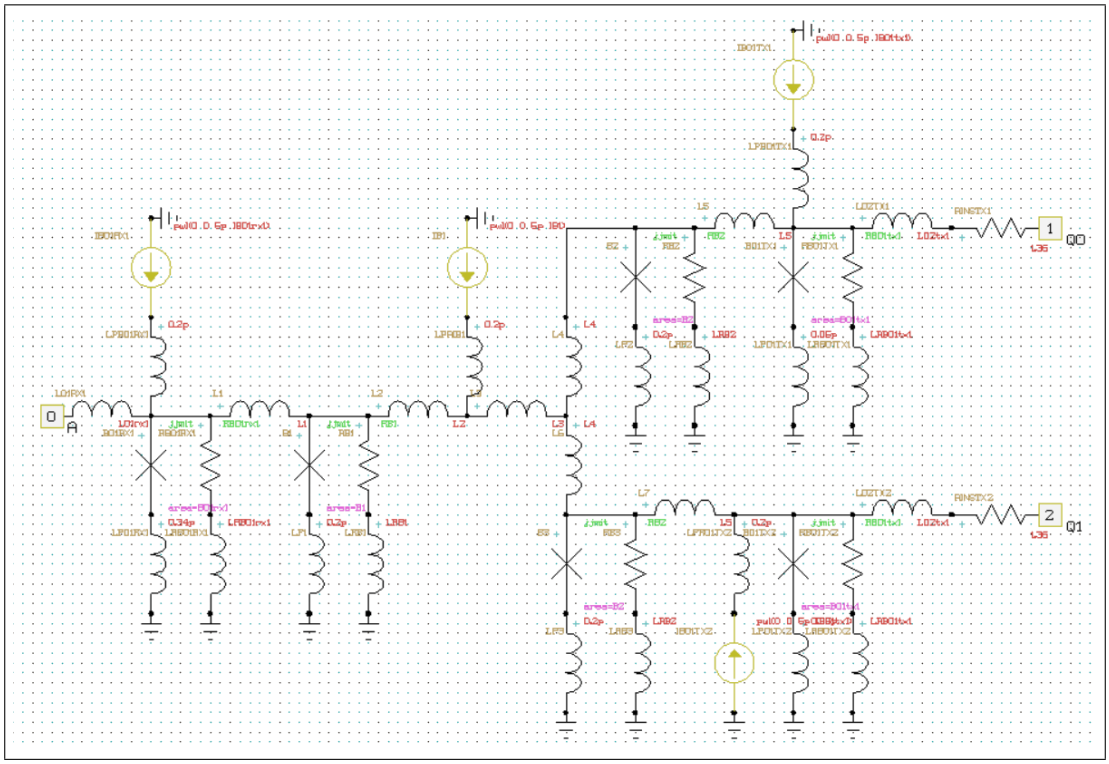

Figure 4.16: Schematic of RSFQ CLKSPLTT.

Layout

The physical layout of the RSFQ CLKSPLTT is shown in Fig. 4.17 and the resulting InductEx extraction is shown in Listing 4.10. The height of the layout is 70 μm and the width is 50 μm.

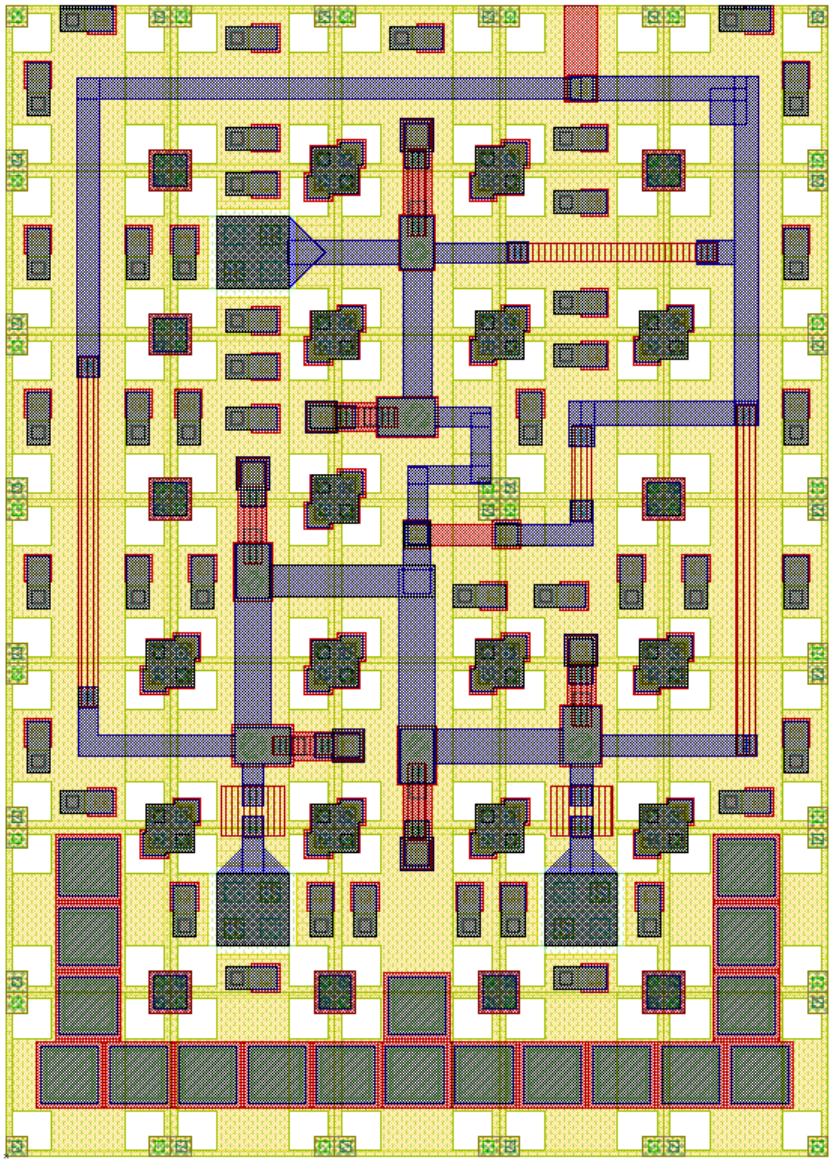

Figure 4.17: RSFQ CLKSPLTT layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_CLKSPLTT_v1p5p1.GDS -n LSmitll_CLKSPLTT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_CLKSPLTT_v1p5_idx.cir read. Totals: L = 20, k = 0, P = 13.
7  Total fundamental loops identified in netlist = 12
8  Using TetraHenry with analytical integration.
9  1628 structures read. Reduced 1628 objects to 1472 polygons and 7 terminals.
10 Top level structure is "LSMITLL_CLKSPLTT_V1P5P1".
11 GDS file LSmitll_CLKSPLTT_v1p5p1.GDS read: db units in 1E-9 m, 0.001 units per user unit.
```

```
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Object in layer I5 moved to TERM layer. (Pj5)
Object in layer I5 moved to TERM layer. (Pj6)
Terminal blocks = 13; Labels = 13; Extracted Ports = 13

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
P3                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 7.754; unknowns = 40; rank = 40.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.49169E-12 --          --          +1.4917E-12 --%
L2        1.526E-12   1.53461E-12 --          --          +8.6065E-15 +0.56399%
L3        2.915E-12   2.87691E-12 --          --          -3.809E-14  -1.3067%
L4        4.8E-13     4.79727E-13 --          --          -2.7336E-16 -0.056949%
L5        1.27E-12    1.29653E-12 --          --          +2.6531E-14 +2.0891%
L6        1.27E-12    1.28261E-12 --          --          +1.2609E-14 +0.99283%
L7        1.257E-12   1.29052E-12 --          --          +3.3524E-14 +2.667%
L8        1.257E-12   1.30541E-12 --          --          +4.8409E-14 +3.8512%
L9        --          6.86244E-13 --          --          +6.8624E-13 --%
L10       --          6.78006E-13 --          --          +6.7801E-13 --%
LB1       --          1.4803E-12  --          --          +1.4803E-12 --%
LB2       --          2.73025E-12 --          --          +2.7303E-12 --%
LB3       --          2.22471E-12 --          --          +2.2247E-12 --%
LB4       --          2.7607E-12  --          --          +2.7607E-12 --%
LP1       --          5.28207E-13 --          --          +5.2821E-13 --%
LP2       --          5.2066E-13  --          --          +5.2066E-13 --%
LP3       --          5.73088E-13 --          --          +5.7309E-13 --%
LP4       --          4.29024E-13 --          --          +4.2902E-13 --%
LP5       --          5.82022E-13 --          --          +5.8202E-13 --%
LP6       --          4.62166E-13 --          --          +4.6217E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000101    0.00010875
J2        0.00017     0.00017853
J3        0.000121    0.00012895
J4        0.00017     0.00017853
J5        0.000121    0.00012895
J6        0.00017     0.00017853

Error bound on extracted values: 5.45866%

Deallocating memory.
Cycles found in 0.030 seconds.
SVD solution in 0.014 seconds.
Job finished in 166.023 seconds.
```

Listing 4.10: RSFQ CLKSPLTT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports  a q0 q1
.subckt LSMITLL_CLKSPLTT a q0 q1
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param Phi0=2.067833848E-15
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param LP=0.2p
.param IC=1.9
.param ICreceive=1.6
.param ICtrans=2.5
.param Lptl=2p
.param LB=2p
.param BiasCoef=0.83
.param RD=1.36
.param B1=ICreceive
.param B2=IC
.param B3=ICtrans
.param B4=ICtrans
.param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
.param IB2=BiasCoef*(B3*Ic0)
.param IB3=BiasCoef*(B4*Ic0)
.param L1=Lptl
.param L2=(Phi0/(2*B1*Ic0))*(B2/(B1+B2))
.param L3=(Phi0/(2*B1*Ic0))*(B1/(B1+B2))
.param L4=(Phi0/(2*B2*Ic0))/2
.param L5=(Phi0/(2*B2*Ic0))/2
.param L6=Lptl
.param L7=(Phi0/(2*B2*Ic0))/2
.param L8=Lptl
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param LRB1=(RB1/Rsheet)*Lsheet
.param LRB2=(RB2/Rsheet)*Lsheet
.param LRB3=(RB3/Rsheet)*Lsheet
.param LRB4=(RB4/Rsheet)*Lsheet
IB1 0 4 pwl(0 0 5p IB1)
IB2 0 8 pwl(0 0 5p IB2)
IB3 0 11 pwl(0 0 5p IB3)
B1 2 3 jjmit area=B1
B2 5 6 jjmit area=B2
B3 8 9 jjmit area=B3
B4 11 12 jjmit area=B4
L1 a 2 L1
L2 2 4 L2
L3 4 5 L3
L4 5 7 L4
L5 7 8 L5
L6 8 10 L6
L7 7 11 L7
L8 11 13 L8
LP1 3 0 0.2p
LP2 6 0 0.2p
LP3 9 0 0.2p
LP4 12 0 0.2p
RB1 2 102 RB1
LRB1 102 0 LRB1
```

```
RB2 5 105 RB2
LRB2 105 0 LRB2
RB3 8 108 RB3
LRB3 108 0 LRB3
RB4 11 111 RB4
LRB4 111 0 LRB4
RD1 13 q0 RD
RD2 10 q1 RD
.ends
```

Listing 4.11: RSFQ CLKSPLTT JoSIM netlist.

Table 4.7: RSFQ CLKSPLTT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ CLKSPLTT are shown in Fig. 4.18. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q0**,

(d) the phase over the output JJ of pin **q1**,

(e) the phase over the input JJ of the load cell connected to pin q0, and

(f) the phase over the input JJ of the load cell connected to pin q1.

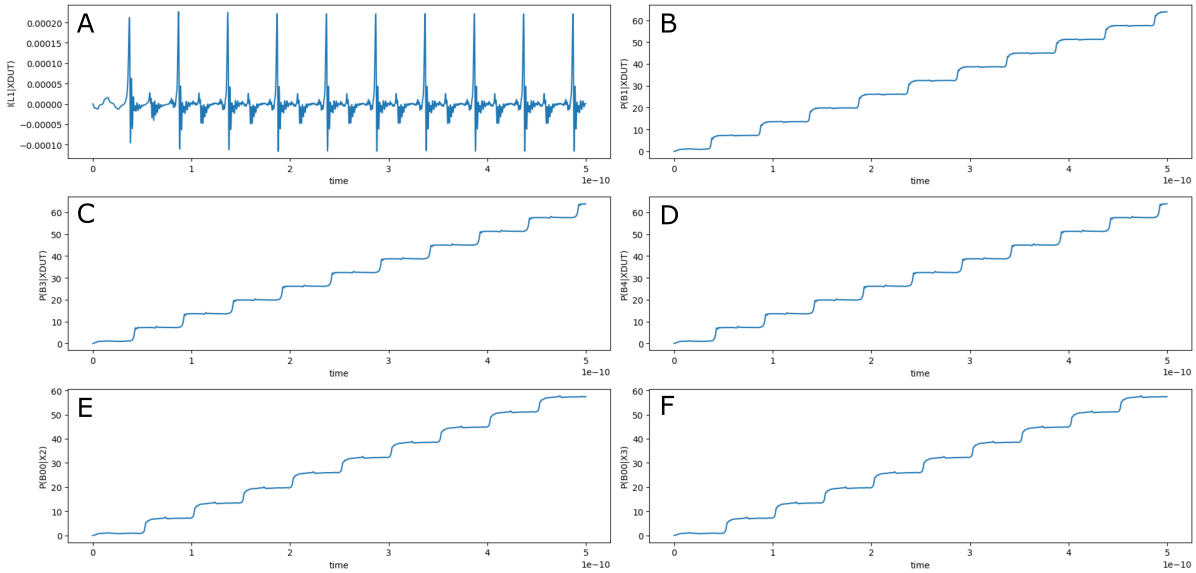

Figure 4.18: RSFQ CLKSPLTT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_CLKSPLTT_v1p5 (a, q0, q1);

input
  a;
output
  q0, q1;
reg
  q0, q1;

real
  delay_state0_a_q0 = 5.5,
  delay_state0_a_q1 = 5.5,
  ct_state0_a_a = 7.0;
reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q0 = 0; // All outputs start at 0
      q1 = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q0 <= 1'bX;  // Set all outputs to unknown
                  q1 <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q0 <= #(delay_state0_a_q0) !q0;
                           q1 <= #(delay_state0_a_q1) !q1;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end
endmodule
```

Listing 4.12: RSFQ CLKSPLTT verilog model.

The digital simulation results for the RSFQ CLKSPLTT is shown in Fig. 4.19 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.20.

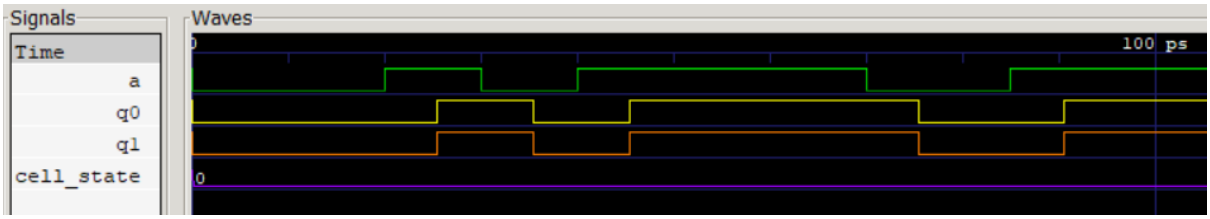

Figure 4.19: RSFQ CLKSPLTT digital simulation results.

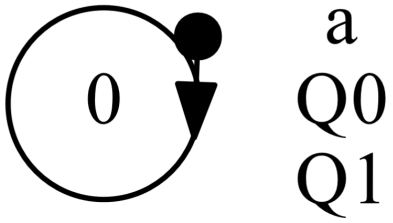

Figure 4.20: RSFQ CLKSPLTT Mealy finite state diagram.

Power consumption

Table 4.8: RSFQ CLKSPLTT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	186	1.76
2	186	3.52
5	186	8.79
10	186	17.6
20	186	35.2
50	186	87.9

4.1.5 MERGET

The MERGET joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the MERGET will generate a pulse on the output signal line. The MERGET has integrated PTL transmitters and receivers is designed to be directly connected to a PTL.

Schematic

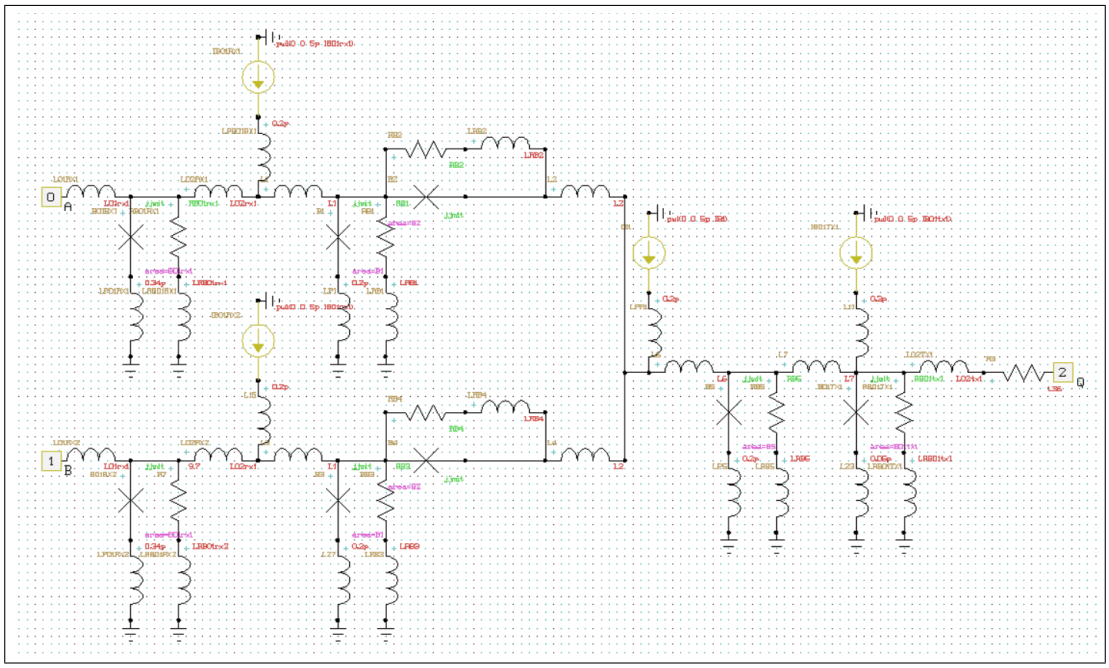

Figure 4.21: Schematic of RSFQ MERGET.

Layout

The physical layout of the RSFQ MERGET is shown in Fig. 4.22 and the resulting InductEx extraction is shown in Listing 4.13. The height of the layout is 70 μm and the width is 70 μm.

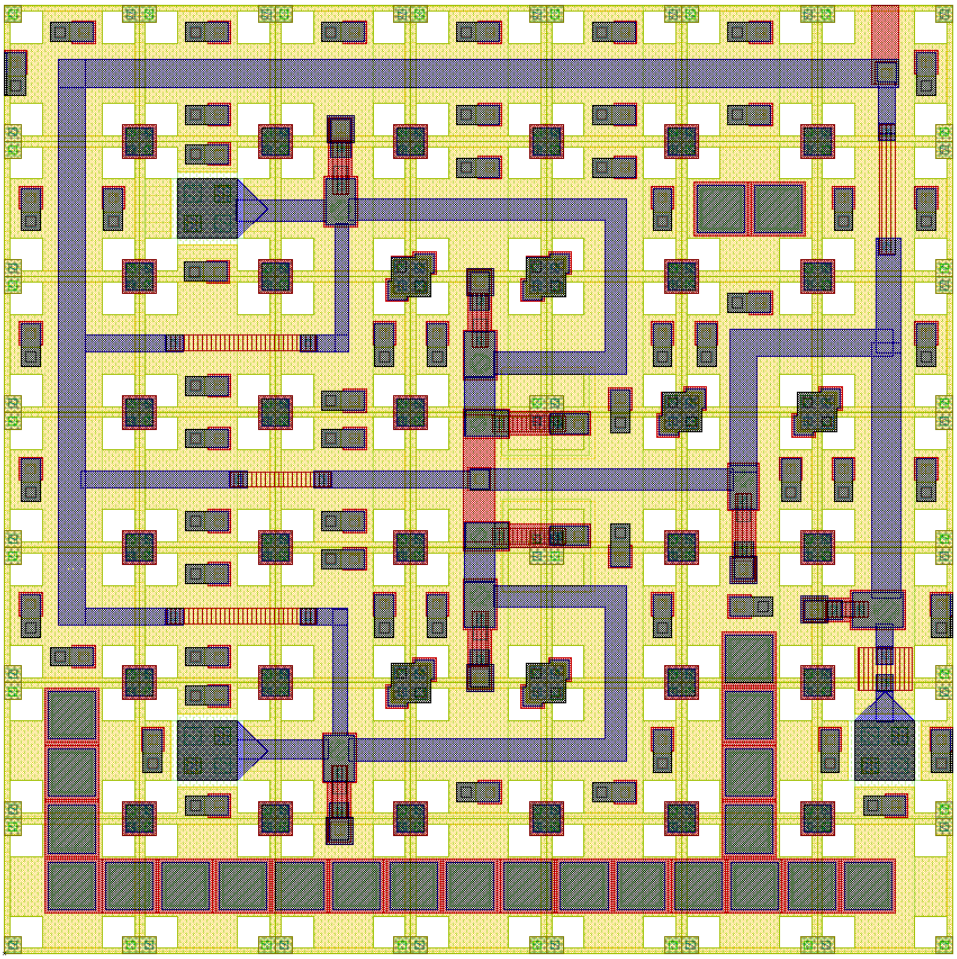

Figure 4.22: RSFQ MERGET layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_MERGET_v1p5.GDS -n LSmitll_MERGET_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_MERGET_v1p5_idx.cir read. Totals: L = 20, k = 0, P = 15.
7  Total fundamental loops identified in netlist = 12
8  Using TetraHenry with analytical integration.
9  3031 structures read. Reduced 3031 objects to 1868 polygons and 7 terminals.
10 Top level structure is "LSMITLL_MERGET_V1P5".
11 GDS file LSmitll_MERGET_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 Object in layer I5 moved to TERM layer. (Pj1)
13 Object in layer I5 moved to TERM layer. (Pj2)
14 Object in layer I5 moved to TERM layer. (Pj3)
15 Object in layer I5 moved to TERM layer. (Pj4)
16 Object in layer I5 moved to TERM layer. (Pj5)
17 Object in layer I5 moved to TERM layer. (Pj6)
18 Object in layer I5 moved to TERM layer. (Pj7)
19 Object in layer I5 moved to TERM layer. (Pj8)
20 Terminal blocks = 15; Labels = 15; Extracted Ports = 15
```

```
21
22 Port                  Positive terminal    Negative terminal
23 P1                    M6,   line along y;  M4,   same as "+" terminal.
24 P2                    M6,   line along y;  M4,   same as "+" terminal.
25 P3                    M6,   line along x;  M4,   same as "+" terminal.
26 PB1                   M6,   line along y;  M4,   same as "+" terminal.
27 PB2                   M6,   line along y;  M4,   same as "+" terminal.
28 PB3                   M6,   line along y;  M4,   same as "+" terminal.
29 PB4                   M6,   line along x;  M4,   same as "+" terminal.
30 J1                    M6,   polygon;       M5,   same as "+" terminal.
31 J2                    M6,   polygon;       M5,   same as "+" terminal.
32 J3                    M6,   polygon;       M5,   same as "+" terminal.
33 J4                    M6,   polygon;       M5,   same as "+" terminal.
34 J5                    M6,   polygon;       M5,   same as "+" terminal.
35 J6                    M6,   polygon;       M5,   same as "+" terminal.
36 J7                    M6,   polygon;       M5,   same as "+" terminal.
37 J8                    M6,   polygon;       M5,   same as "+" terminal.
38
39 SVD info: Condition nr. = 22.23; unknowns = 40; rank = 40.
40
41 Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
42 Name       Design      Extracted   Design      Extracted   (L only)    (L only)
43 L1         --          1.43596E-12 --          --          +1.436E-12  --%
44 L2         7E-12       6.9603E-12  --          --          -3.9696E-14 -0.56709%
45 L3         1.1516E-12  1.1585E-12  --          --          +6.8974E-15 +0.59894%
46 L4         --          1.46901E-12 --          --          +1.469E-12  --%
47 L5         7E-12       6.98178E-12 --          --          -1.8223E-14 -0.26033%
48 L6         1.1516E-12  1.16474E-12 --          --          +1.3135E-14 +1.1406%
49 L7         3.432E-12   3.42648E-12 --          --          -5.5184E-15 -0.16079%
50 L8         2.706E-12   2.72351E-12 --          --          +1.7511E-14 +0.6471%
51 L9         2.706E-12   2.72509E-12 --          --          +1.9087E-14 +0.70534%
52 L10        --          4.94845E-13 --          --          +4.9484E-13 --%
53 LB1        --          2.78262E-12 --          --          +2.7826E-12 --%
54 LB2        --          2.76369E-12 --          --          +2.7637E-12 --%
55 LB3        --          2.49926E-12 --          --          +2.4993E-12 --%
56 LB4        --          1.32299E-12 --          --          +1.323E-12  --%
57 LP1        --          4.81069E-13 --          --          +4.8107E-13 --%
58 LP2        --          5.38402E-13 --          --          +5.384E-13  --%
59 LP4        --          4.79009E-13 --          --          +4.7901E-13 --%
60 LP5        --          5.35867E-13 --          --          +5.3587E-13 --%
61 LP7        --          5.92031E-13 --          --          +5.9203E-13 --%
62 LP8        --          3.667E-13   --          --          +3.667E-13  --%
63
64 Ports      Design    Extracted AbsDiff   PercDiff
65 J1         --          0.00016855
66 J2         --          0.00016197
67 J3         --          0.00010274
68 J4         --          0.00016855
69 J5         --          0.00016197
70 J6         --          0.00010274
71 J7         --          0.00012397
72 J8         --          0.00025893
73
74 Error bound on extracted values: 2.75924%
75
76 Deallocating memory.
77 Cycles found in 0.028 seconds.
78 SVD solution in 0.015 seconds.
79 Job finished in 259.423 seconds.
```

Listing 4.13: RSFQ MERGET InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                          a b q
.subckt LSmitll_MERGET a b q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01rx1=0.88429
.param B01tx1=0.842106
.param B1=1.45438
.param B2=0.960422
.param B5=0.805138
.param IB01rx1=0.000106334
.param IB01tx1=5.04979e-5
.param IB1=0.000186124
.param L01rx1=2e-012
.param L02rx1=1.27924e-012
.param L02tx1=4.81637e-012
.param L1=1.75737e-012
.param L2=2e-012
.param L6=2.22418e-012
.param L7=8.49377e-012
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB1=(RB1/Rsheet)*Lsheet
.param LRB2=(RB2/Rsheet)*Lsheet
.param LRB3=(RB3/Rsheet)*Lsheet
.param LRB4=(RB4/Rsheet)*Lsheet
.param LRB5=(RB5/Rsheet)*Lsheet
.param RB01rx1=B0Rs/B01rx1
.param RB01rx2=B0Rs/B01rx1
.param RB01tx1=B0Rs/B01tx1
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B1
.param RB4=B0Rs/B2
.param RB5=B0Rs/B5
B01rx1 6 18  jjmit area=B01rx1
B01rx2 13 32  jjmit area=B01rx1
B01tx1 10 28  jjmit area=B01tx1
B1 7 20  jjmit area=B1
B2 4 5  jjmit area=B2
B3 14 34  jjmit area=B1
B4 11 12  jjmit area=B2
B5 9 26  jjmit area=B5
IB01rx1 0 15 pwl(0 0 5p IB01rx1)
IB01rx2 0 24 pwl(0 0 5p IB01rx1)
IB01tx1 0 23 pwl(0 0 5p IB01tx1)
IB1 0 22 pwl(0 0 5p IB1)
L01rx1 a 6 L01rx1
L01rx2 b 13 L01rx1
L02rx1 6 16 L02rx1
L02rx2 13 30 L02rx1
L02tx1 10 25 L02tx1
L1 16 7 L1
L2 5 8 L2
L3 30 14 L1
L12 23 10 0.2p
L16 24 30 0.2p
```

```
L1b 7 4 1p
L25 28 0 0.05p
L29 34 0 0.2p
L3b 14 11 1p
L4 12 8 L2
L6 8 9 L6
L7 9 10 L7
LP01rx1 18 0 0.34p
LP01rx2 32 0 0.34p
LP1 20 0 0.2p
LP5 26 0 0.2p
LPR01rx1 15 16 0.2p
LPR1 22 8 0.2p
LRB01rx1 19 0 LRB01rx1
LRB01rx2 33 0 LRB01rx2
LRB01tx1 29 0 LRB01tx1
LRB1 21 0 LRB1
LRB2 17 5 LRB2
LRB3 35 0 LRB3
LRB4 31 12 LRB4
LRB5 27 0 LRB5
R3 25 q 1.36
RB01rx2 13 33 RB01rx2
RB01rx1 6 19 RB01rx1
RB01tx1 10 29 RB01tx1
RB1 7 21 RB1
RB2 4 17 RB2
RB3 14 35 RB3
RB4 11 31 RB4
RB5 9 27 RB5
.ends
```

Listing 4.14: RSFQ MERGET JoSIM netlist.

Table 4.9: RSFQ MERGET pin list.

Pin	Description
a	Data input
b	Data input
q	Data output

The JoSIM simulation results for the RSFQ MERGET are shown in Fig. 4.23. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **b**,

(d) the phase over the input JJ of pin **b**,

(e) the phase over the output JJ of pin **q**,

(f) the phase over the input JJ of the load cell connected to pin q via a PTL.

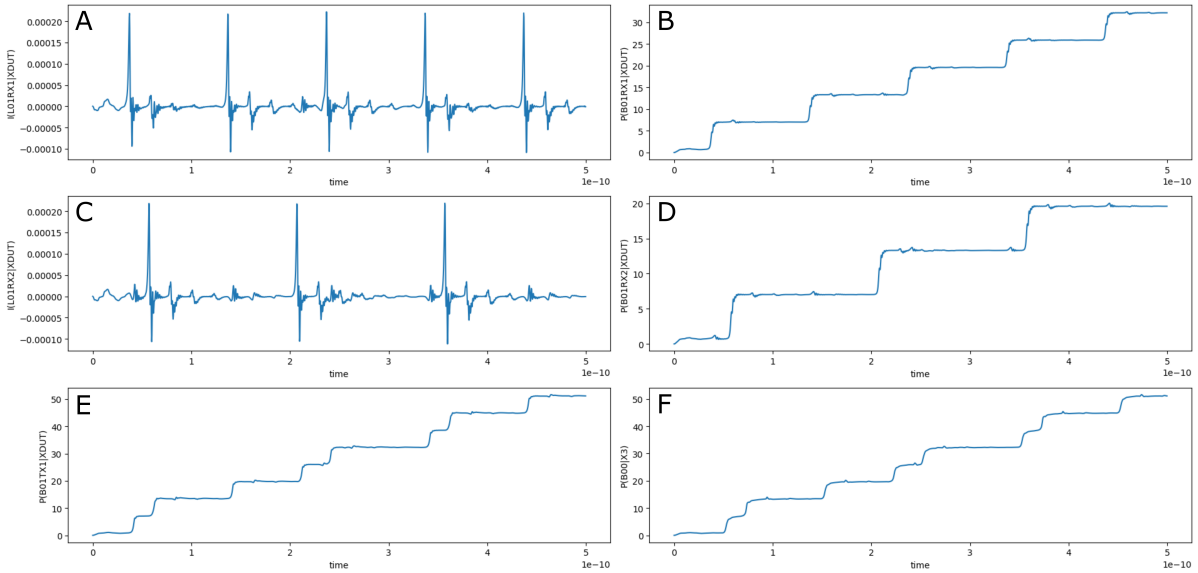

Figure 4.23: RSFQ MERGET analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_MERGET_v1p5 (a, b, q);

input
  a, b;

output
  q;

reg
  q;

real
  delay_state0_a_q = 5.3,
  delay_state0_b_q = 5.3,
  ct_state0_a_a = 4.8,
  ct_state0_a_b = 1.6,
  ct_state0_b_a = 1.6,
  ct_state0_b_b = 4.8;

reg
   errorsignal_a,
   errorsignal_b;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                           errorsignal_b = 1;  // Critical timing on this input; assign
                               ↪ immediately
```

```
64                              errorsignal_b <= #(ct_state0_a_b) 0;  // Clear error signal
                                    ↪ after critical timing expires
65                          end
66                      endcase
67                  end
68          end
69      end
70
71  always @(posedge b or negedge b) // execute at positive and negative edges of input
72      begin
73         if ($time>4) // arbitrary steady-state time)
74            begin
75               if (errorsignal_b == 1'b1)  // A critical timing is active for this input
76                  begin
77                     outfile = $fopen("errors.txt", "a");
78                     $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                           ↪ ", $stime);
79                     $fclose(outfile);
80                     q <= 1'bX;  // Set all outputs to unknown
81                  end
82               if (errorsignal_b == 0)
83                  begin
84                     case (cell_state)
85                        0: begin
86                              q <= #(delay_state0_b_q) !q;
87                              errorsignal_a = 1;  // Critical timing on this input; assign
                                    ↪ immediately
88                              errorsignal_a <= #(ct_state0_b_a) 0;  // Clear error signal
                                    ↪ after critical timing expires
89                              errorsignal_b = 1;  // Critical timing on this input; assign
                                    ↪ immediately
90                              errorsignal_b <= #(ct_state0_b_b) 0;  // Clear error signal
                                    ↪ after critical timing expires
91                           end
92                     endcase
93                  end
94          end
95      end
96
97  endmodule
```

Listing 4.15: RSFQ MERGET verilog model.

The digital simulation results for the RSFQ MERGET is shown in Fig. 4.24 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.25.

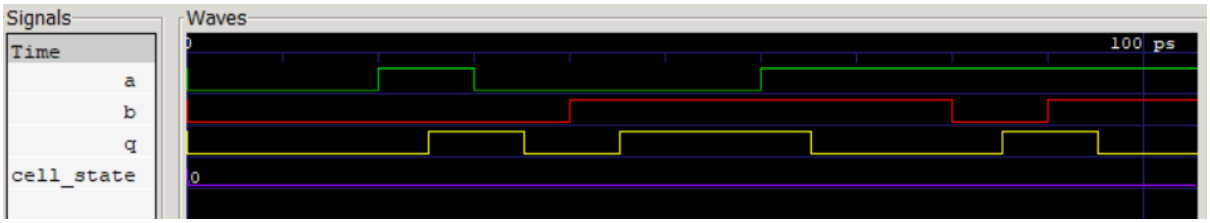

Figure 4.24: RSFQ MERGET digital simulation results.

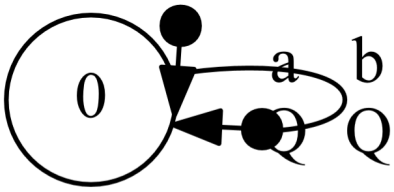

Figure 4.25: RSFQ MERGET Mealy finite state diagram.

Power consumption

Table 4.10: RSFQ MERGET power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	117	1.71
2	117	3.41
5	117	8.53
10	117	17.1
20	117	34.1
50	117	85.3

4.1.6 PTLTX

The RSFQ PTLTX is a cell which transmits a pulse signal over a PTL. It is connected to cells that are not designed to connect to PTLs when a PTL connection is required.

Schematic

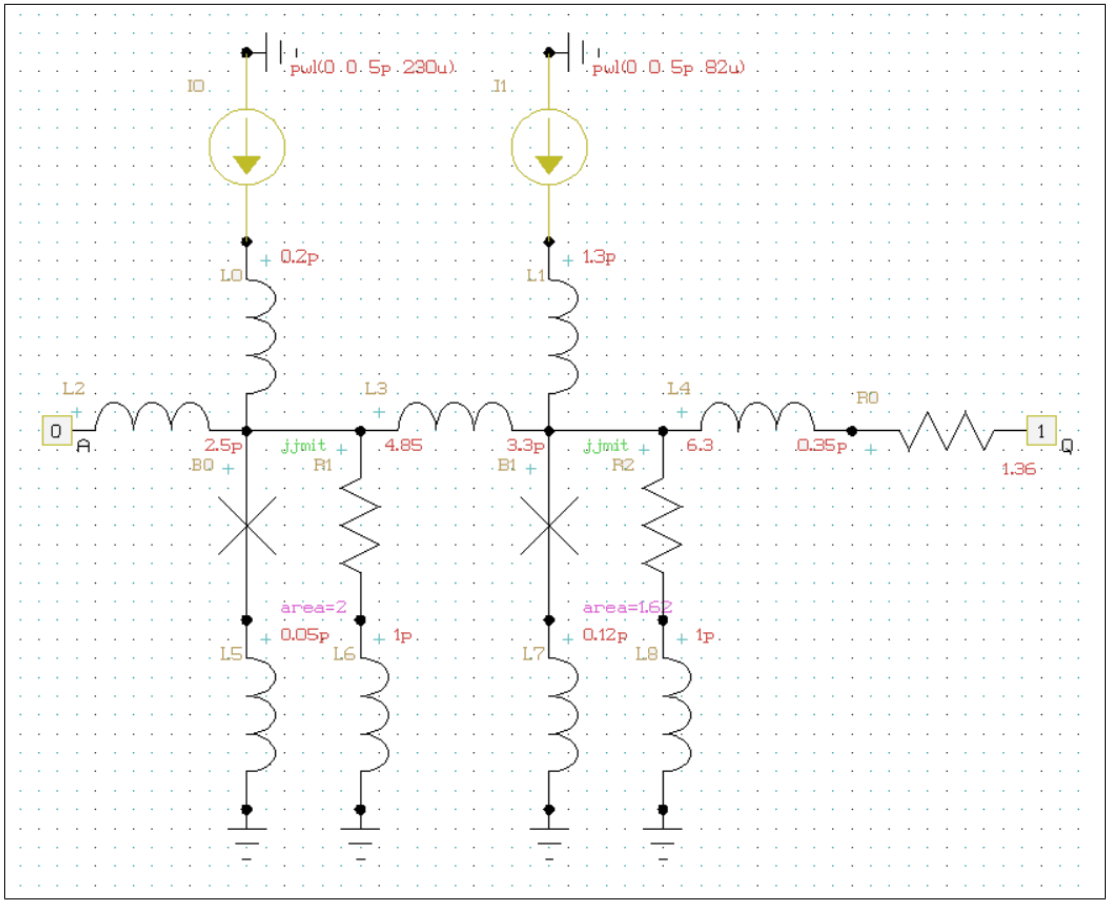

Figure 4.26: Schematic of RSFQ PTLTX.

Layout

The physical layout for the RSFQ PTLTX is shown in Fig. 4.27 and the resulting InductEx extraction is shown in Listing 4.16. The layout height is 70 μm and the width is 30 μm.

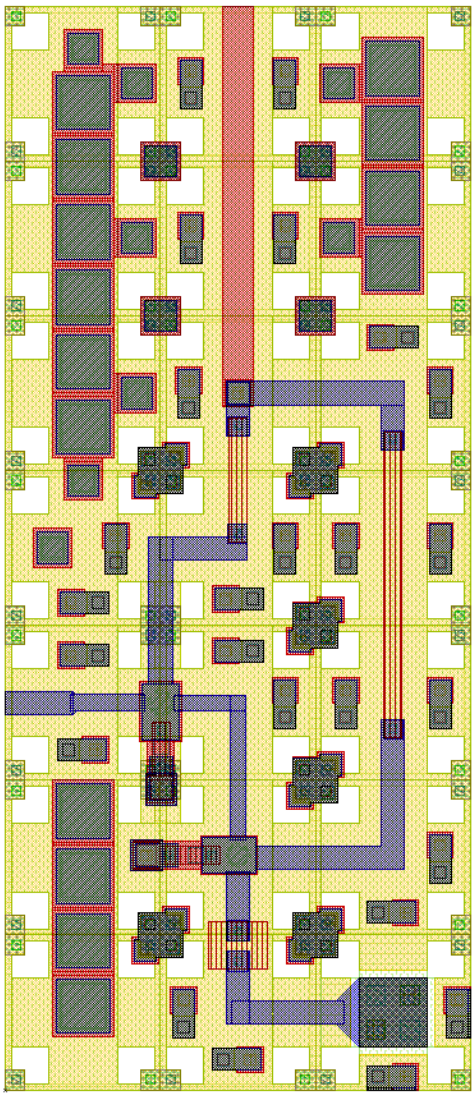

Figure 4.27: RSFQ PTLTX Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_PTLTX_v1p5.GDS -n LSmitll_ptltx_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_ptltx_v1p5_idx.cir read. Totals: L = 7, k = 0, P = 6.
Total fundamental loops identified in netlist = 5
Using TetraHenry with analytical integration.
898 structures read. Reduced 898 objects to 842 polygons and 4 terminals.
Top level structure is "LSMITLL_PTLTX_V1P5".
GDS file LSmitll_PTLTX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Terminal blocks = 6; Labels = 6; Extracted Ports = 6

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
P3                    M6,   polygon;       M4,   same as "+" terminal.
P4                    M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 3.491; unknowns = 14; rank = 14.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        2.5E-12     2.49244E-12 --          --          -7.5618E-15 -0.30247%
L2        3.3E-12     3.30827E-12 --          --          +8.2664E-15 +0.2505%
L3        --          1.00626E-12 --          --          +1.0063E-12 --%
LP1       --          5.06259E-13 --          --          +5.0626E-13 --%
LP2       --          4.76485E-13 --          --          +4.7648E-13 --%
LB1       --          2.87048E-12 --          --          +2.8705E-12 --%
LB2       --          3.42025E-12 --          --          +3.4203E-12 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.0002      0.00020853
J2        0.000162    0.00017055

Error bound on extracted values: 2.97934%

Deallocating memory.
Cycles found in 0.028 seconds.
SVD solution in 0.017 seconds.
Job finished in 78.918 seconds.
```

Listing 4.16: RSFQ PTLTX InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

* Ports                          a q
.subckt LSmitll_PTLTX a q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
B0 3 8 12 jjmit area=2
B1 4 10 13 jjmit area=1.62
I0 0 5 pwl(0 0 5p 230u)
I1 0 6 pwl(0 0 5p 82u)
L0 5 3 0.2p
L1 6 4 1.3p
L2 a 3 2.5p
L3 3 4 3.3p
L4 4 7 0.35p
L5 8 0 0.05p
L6 9 0 1p
L7 10 0 0.12p
L8 11 0 1p
R0 7 q 1.36
R1 3 9 4.85
R2 4 11 6.3
.ends
```

Listing 4.17: RSFQ PTLTX JoSIM netlist.

Table 4.11: RSFQ PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLTX using JoSIM is shown in Fig. 4.28. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected via a PTL to the PTLTX.

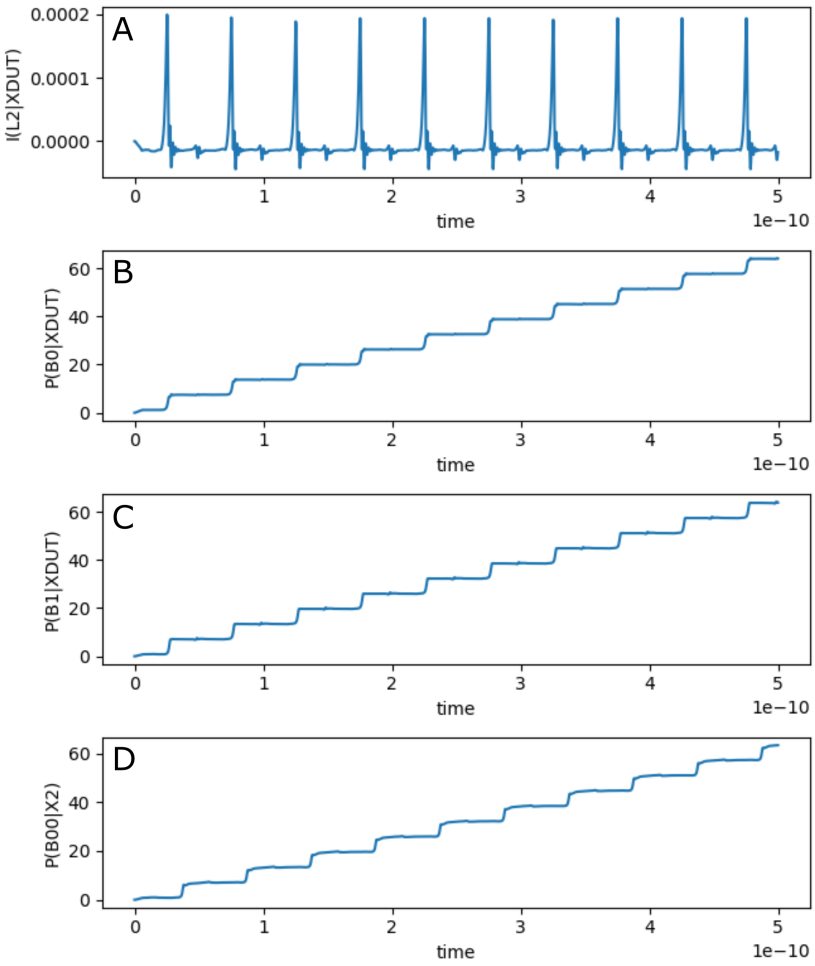

Figure 4.28: RSFQ PTLTX analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_ptltx_v1p5 (a, q);

input
  a;

output
  q;

reg
  q;

real
  delay_state0_a_q = 2.2,
  ct_state0_a_a = 3.5;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end

endmodule
```

Listing 4.18: RSFQ PTLTX verilog model.

The digital simulation results for the RSFQ PTLTX is shown in Fig. 4.29 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.30.

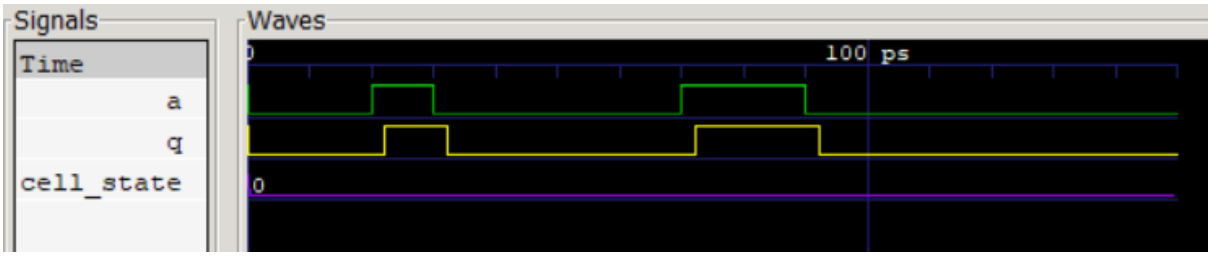

Figure 4.29: RSFQ PTLTX digital simulation results.

Figure 4.30: RSFQ PTLTX Mealy finite state machine diagram.

Power Consumption

Table 4.12: RSFQ PTLTX power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	81	0.75
2	81	1.50
5	81	3.74
10	81	7.49
20	81	15.0
50	81	37.4

4.1.7 PTLRX

The PTLRX is a receiver cell which receives a pulse signal from a PTL. It is connected to cells that are not designed to connect to PTLs when a PTL connection is required.

Schematic

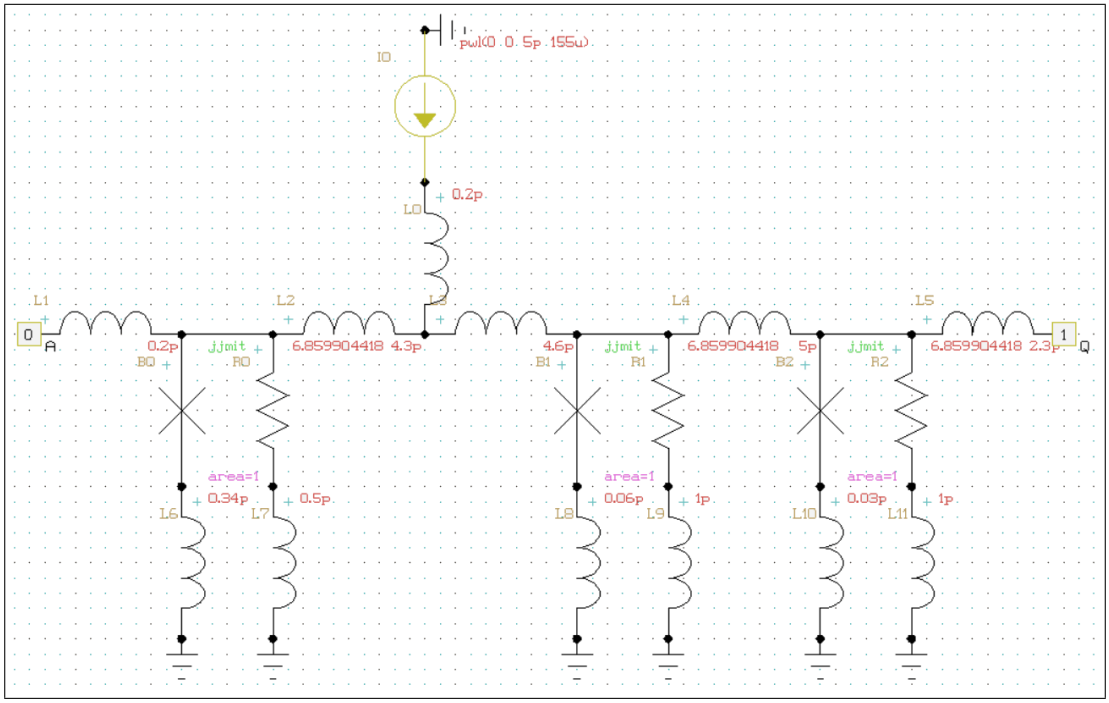

Figure 4.31: Schematic of RSFQ PTLRX.

Layout

The physical layout for the RSFQ PTLRX is shown in Fig. 4.32 and the resulting InductEx extraction is shown in Listing 4.19. The layout height is 70 μm and the width is 30 μm.

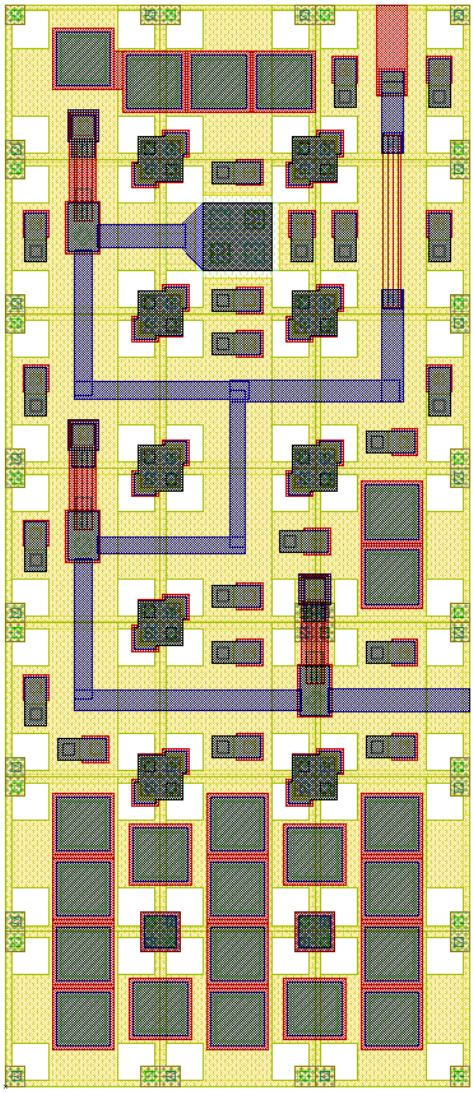

Figure 4.32: RSFQ PTLRX Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_PTLRX_v1p5.GDS -n LSmitll_ptlrx_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_ptlrx_v1p5_idx.cir read. Totals: L = 9, k = 0, P = 6.
Total fundamental loops identified in netlist = 5
Using TetraHenry with analytical integration.
881 structures read. Reduced 881 objects to 845 polygons and 3 terminals.
Top level structure is "LSMITLL_PTLRX_V1P5".
GDS file LSmitll_PTLRX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 6; Labels = 6; Extracted Ports = 6

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
P3                    M6,   line along y;  M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 10.05; unknowns = 18; rank = 18.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.46476E-12 --          --          +1.4648E-12 --%
L2        4.3E-12     4.28216E-12 --          --          -1.7838E-14 -0.41483%
L3        4.6E-12     4.63061E-12 --          --          +3.0611E-14 +0.66546%
L4        5E-12       4.98366E-12 --          --          -1.6344E-14 -0.32687%
L5        2.3E-12     2.28808E-12 --          --          -1.192E-14  -0.51826%
LB1       --          3.25119E-12 --          --          +3.2512E-12 --%
LP1       --          5.57791E-13 --          --          +5.5779E-13 --%
LP2       --          6.14427E-13 --          --          +6.1443E-13 --%
LP3       --          5.44764E-13 --          --          +5.4476E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.0001      0.00010794
J2        0.0001      0.00010794
J3        0.0001      0.00010794

Error bound on extracted values: 0.119751%

Deallocating memory.
Cycles found in 0.028 seconds.
SVD solution in 0.015 seconds.
Job finished in 77.204 seconds.
```

Listing 4.19: RSFQ PTLRX InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

* Ports                          a q
.subckt LSmitll_PTLRX a q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
B0 3 8 14 jjmit area=1
B1 4 10 15 jjmit area=1
B2 5 12 16 jjmit area=1
I0 0 6 pwl(0 0 5p 155u)
L0 6 7 0.2p
L1 a 3 0.2p
L2 3 7 4.3p
L3 7 4 4.6p
L4 4 5 5p
L5 5 q 2.3p
L6 8 0 0.34p
L7 9 0 0.5p
L8 10 0 0.06p
L9 11 0 1p
L10 12 0 0.03p
L11 13 0 1p
R0 3 9 6.859904418
R1 4 11 6.859904418
R2 5 13 6.859904418
.ends
```

Listing 4.20: RSFQ PTLRX JoSIM netlist.

Table 4.13: RSFQ PTLRX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX using JoSIM is shown in Fig. 4.33. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected to pin **q**.

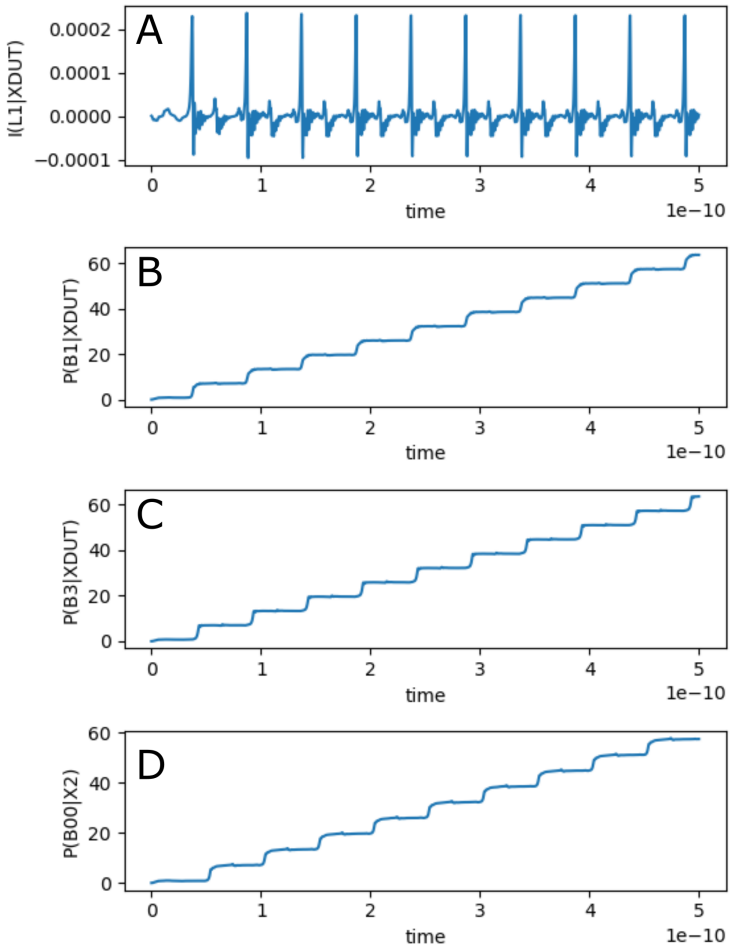

Figure 4.33: RSFQ PTLRX analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_ptlrx_v1p5 (a, q);

input
  a;

output
  q;

reg
  q;

real
  delay_state0_a_q = 5.3,
  ct_state0_a_a = 11.3;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end

endmodule
```

Listing 4.21: RSFQ PTLRX verilog model.

The digital simulation results for the RSFQ PTLRX is shown in Fig. 4.34 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.35.

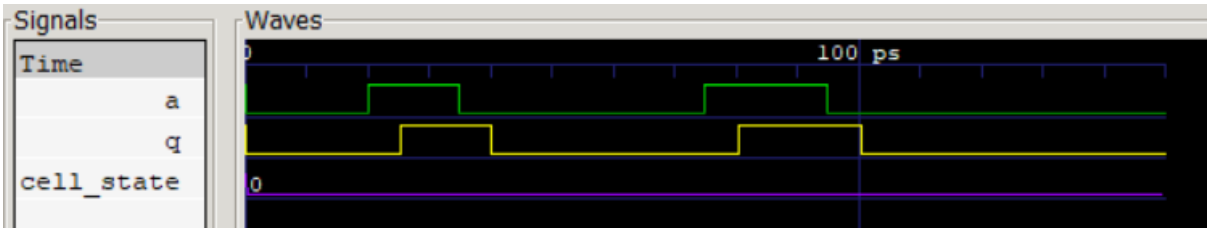

Figure 4.34: RSFQ PTLRX digital simulation results.

Figure 4.35: RSFQ PTLRX Mealy finite state machine diagram.

Power Consumption

Table 4.14: RSFQ PTLRX power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	40.3	0.62
2	40.3	1.24
5	40.3	3.10
10	40.3	6.20
20	40.3	12.4
50	40.3	31.0

4.2 Logic Cells

4.2.1 AND2T

The RSFQ AND2T cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The AND2T is designed with integrated PTL transmitters and receivers and is meant to be connected directly to a PTL.

Schematic

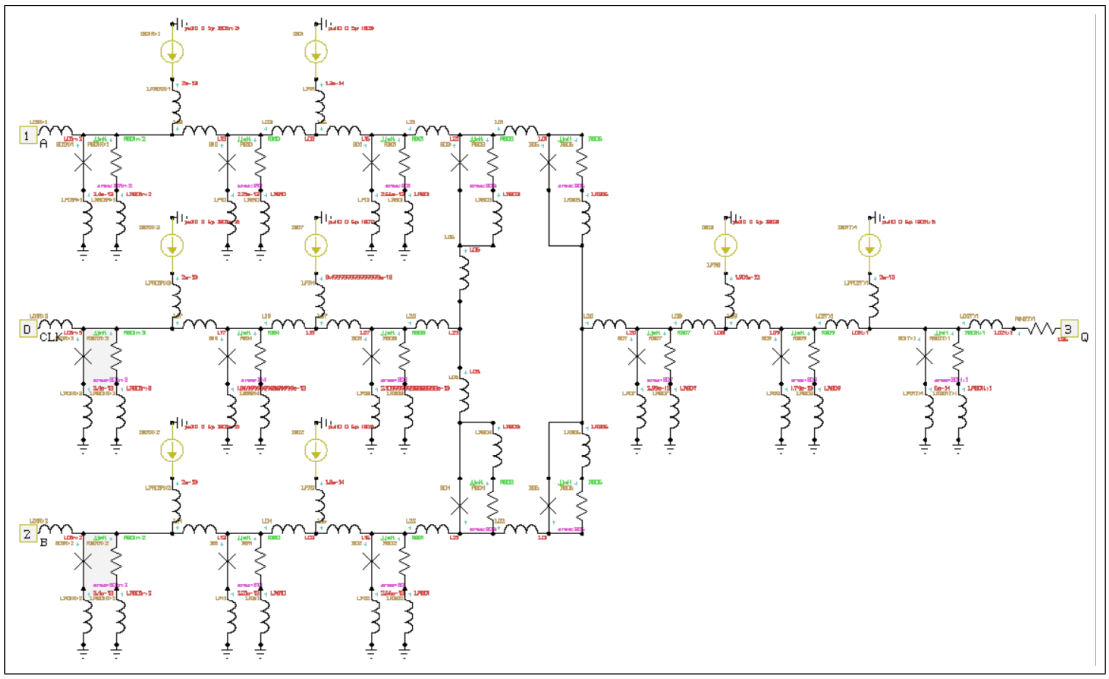

Figure 4.36: Schematic of RSFQ AND2T.

Layout

The physical layout for the RSFQ AND2T is shown in Fig. 4.37 and the resulting InductEx extraction is shown in Listing 4.22. The layout height is 70 μm and the width is 100 μm.

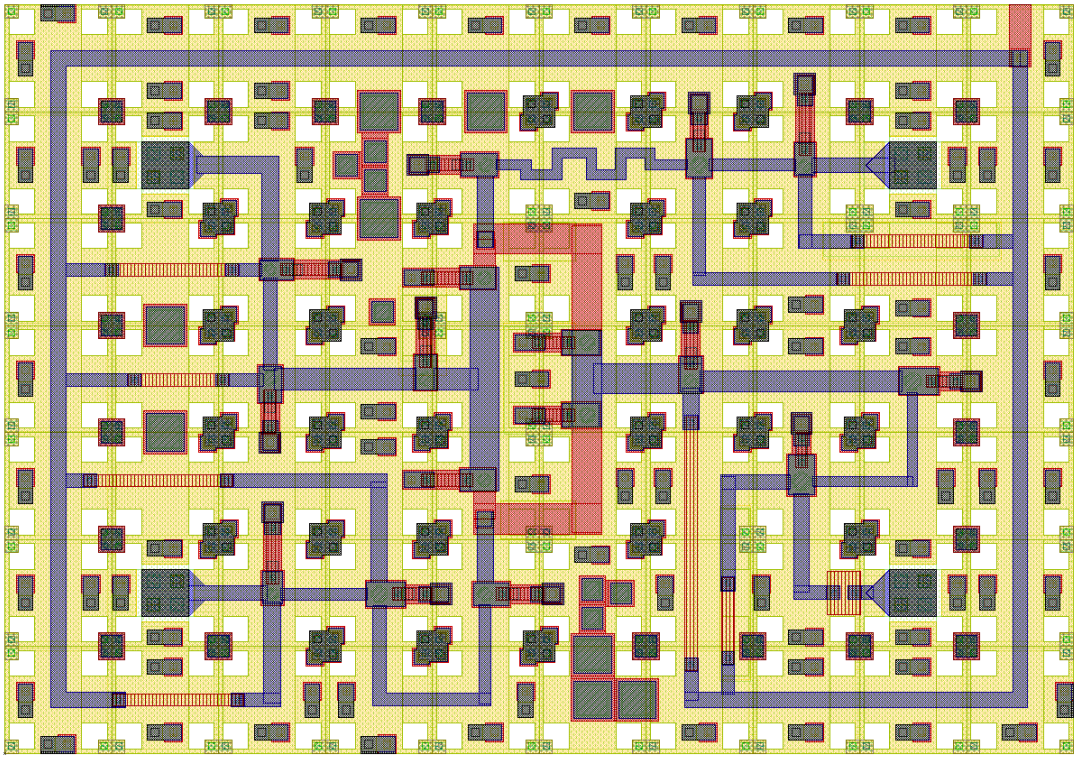

Figure 4.37: RSFQ AND2T Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_AND2T_v1p5.GDS -n LSmitll_AND2T_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_AND2T_v1p5_idx.cir read. Totals: L = 40, k = 0, P = 28.
Total fundamental loops identified in netlist = 24
Using TetraHenry with analytical integration.
2849 structures read. Reduced 2849 objects to 2647 polygons and 12 terminals.
Top level structure is "LSMITLL_AND2T_V1P5".
GDS file LSmitll_AND2T_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Port clk not in netlist. Ignored.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Object in layer I5 moved to TERM layer. (Pj5)
Object in layer I5 moved to TERM layer. (Pj6)
Object in layer I5 moved to TERM layer. (Pj7)
Object in layer I5 moved to TERM layer. (Pj8)
Object in layer I5 moved to TERM layer. (Pj9)
Object in layer I5 moved to TERM layer. (Pj10)
Object in layer I5 moved to TERM layer. (Pj11)
Object in layer I5 moved to TERM layer. (Pj12)
Object in layer I5 moved to TERM layer. (Pj13)
Object in layer I5 moved to TERM layer. (Pj14)
Object in layer I5 moved to TERM layer. (Pj15)
Object in layer I5 moved to TERM layer. (Pj16)
Terminal blocks = 28; Labels = 29; Extracted Ports = 28

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
P3                    M6,   line along y;  M4,   same as "+" terminal.
P4                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
PB5                   M6,   polygon;       M4,   same as "+" terminal.
PB6                   M6,   polygon;       M4,   same as "+" terminal.
PB7                   M6,   polygon;       M4,   same as "+" terminal.
PB8                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M5,   polygon;       M6,   same as "+" terminal.
J5                    M5,   polygon;       M6,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M6,   polygon;       M5,   same as "+" terminal.
J8                    M6,   polygon;       M5,   same as "+" terminal.
J9                    M6,   polygon;       M5,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.
J11                   M6,   polygon;       M5,   same as "+" terminal.
J12                   M6,   polygon;       M5,   same as "+" terminal.
J13                   M6,   polygon;       M5,   same as "+" terminal.
J14                   M6,   polygon;       M5,   same as "+" terminal.
J15                   M6,   polygon;       M5,   same as "+" terminal.
J16                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 8.412; unknowns = 80; rank = 80.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.60073E-12 --          --          +1.6007E-12 --%
L2        2.23E-12    2.25151E-12 --          --          +2.1505E-14 +0.96436%
L4        6.105E-12   6.11619E-12 --          --          +1.1188E-14 +0.18326%
L5        1.2909E-12  1.29165E-12 --          --          +7.4642E-16 +0.057821%
L6        2.58E-12    2.59574E-12 --          --          +1.574E-14  +0.61009%
L7        1.1464E-12  1.59839E-12 --          --          +4.5199E-13 +39.427%
```

```
L8        --          3.11847E-12 --          --          +3.1185E-12 --%
L9        1.9428E-12  1.94567E-12 --          --          +2.8651E-15 +0.14747%
L11       1.9932E-12  1.98734E-12 --          --          -5.8588E-15 -0.29394%
L12       --          6.07532E-13 --          --          +6.0753E-13 --%
L13       --          1.64628E-12 --          --          +1.6463E-12 --%
L14       2.23E-12    2.22004E-12 --          --          -9.9623E-15 -0.44674%
L16       6.105E-12   6.02447E-12 --          --          -8.0528E-14 -1.3191%
L17       1.2909E-12  1.23479E-12 --          --          -5.6106E-14 -4.3463%
L18       2.58E-12    2.59837E-12 --          --          +1.8368E-14 +0.71195%
L19       1.1464E-12  1.59255E-12 --          --          +4.4615E-13 +38.918%
L20       4E-13       8.96801E-13 --          --          +4.968E-13  +124.2%
L22       2.925E-12   2.96832E-12 --          --          +4.3321E-14 +1.481%
L23       4.644E-12   4.70343E-12 --          --          +5.943E-14  +1.2797%
L24       --          2.59567E-12 --          --          +2.5957E-12 --%
LB1       --          2.57564E-12 --          --          +2.5756E-12 --%
LB2       --          4.95898E-12 --          --          +4.959E-12  --%
LB3       --          8.25429E-13 --          --          +8.2543E-13 --%
LB4       --          9.86159E-13 --          --          +9.8616E-13 --%
LB5       --          2.61941E-12 --          --          +2.6194E-12 --%
LB6       --          5.13694E-12 --          --          +5.1369E-12 --%
LB7       --          8.14214E-13 --          --          +8.1421E-13 --%
LB8       --          3.19526E-12 --          --          +3.1953E-12 --%
LP1       --          5.35804E-13 --          --          +5.358E-13  --%
LP2       --          5.41416E-13 --          --          +5.4142E-13 --%
LP3       --          5.31678E-13 --          --          +5.3168E-13 --%
LP6       --          5.4205E-13  --          --          +5.4205E-13 --%
LP7       --          5.01792E-13 --          --          +5.0179E-13 --%
LP8       --          5.52821E-13 --          --          +5.5282E-13 --%
LP9       --          5.37028E-13 --          --          +5.3703E-13 --%
LP10      --          5.37254E-13 --          --          +5.3725E-13 --%
LP11      --          5.86571E-13 --          --          +5.8657E-13 --%
LP14      --          5.36996E-13 --          --          +5.37E-13   --%
LP15      --          5.39743E-13 --          --          +5.3974E-13 --%
LP16      --          5.29126E-13 --          --          +5.2913E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000088    0.000095735
J2        0.000176    0.00018464
J3        0.000132    0.00013971
J4        0.000113    0.00012116
J5        0.000153    0.00016161
J6        0.00009     0.00009764
J7        0.00015     0.00015829
J8        0.000117    0.0001249
J9        0.000088    0.000095735
J10       0.000176    0.00018464
J11       0.000132    0.00013971
J12       0.000113    0.00012116
J13       0.000153    0.00016161
J14       0.000126    0.00013429
J15       0.000204    0.00021285
J16       0.000227    0.00023609

Error bound on extracted values: 4.50093%

Deallocating memory.
Cycles found in 0.033 seconds.
SVD solution in 0.050 seconds.
Job finished in 410.701 seconds.
```

Listing 4.22: RSFQ AND2T InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                              a b clk q
.subckt LSmitll_AND2T a b clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1.0
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01=1.31899
.param B01rx2=0.88063
.param B01rx3=0.90139
.param B01tx1=2.26625
.param B03=1.13403
.param B05=1.52701
.param B07=1.25725
.param B08=1.56701
.param B09=2.03545
.param B10=1.75934
.param B14=1.50181
.param IB01=0.000113269
.param IB01rx2=0.000131447
.param IB01rx3=0.000127540
.param IB01tx1=0.000213665
.param IB03=0.000062676
.param IB07=0.000179300
.param L01=2.57966e-12
.param L01rx2=1.53695e-12
.param L01rx3=1.77460e-12
.param L01tx1=1.53695e-12
.param L02tx1=2.74282e-12
.param L03=1.93254e-12
.param L05=1.14641e-12
.param L07=1.99319e-12
.param L08=3.9e-14
.param L09=2.92475e-12
.param L13=2.23040e-12
.param L15=6.10490e-12
.param L17=1.94280e-12
.param L19=2.03734e-13
.param L20=3.99011e-13
.param L21=1.29090e-13
.param L23=1e-14
.param LRB01=(RB01/Rsheet)*Lsheet
.param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
.param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB03=(RB03/Rsheet)*Lsheet
.param LRB05=(RB05/Rsheet)*Lsheet
.param LRB07=(RB07/Rsheet)*Lsheet
.param LRB08=(RB08/Rsheet)*Lsheet
.param LRB09=(RB09/Rsheet)*Lsheet
.param LRB10=(RB10/Rsheet)*Lsheet
.param LRB14=(RB14/Rsheet)*Lsheet
.param RB01=B0Rs/B01
.param RB01rx2=B0Rs/B01rx2
.param RB01rx3=B0Rs/B01rx3
.param RB01tx1=B0Rs/B01tx1
.param RB03=B0Rs/B03
.param RB05=B0Rs/B05
.param RB07=B0Rs/B07
.param RB08=B0Rs/B08
.param RB09=B0Rs/B09
.param RB10=B0Rs/B10
.param RB14=B0Rs/B14
B01 7 32 jjmit area=B01
B01RX1 5 28 jjmit area=B01rx2
B01RX2 20 60 jjmit area=B01rx2
B01RX3 13 43 jjmit area=B01rx3
B01TX1 18 53 jjmit area=B01tx1
B02 22 64 jjmit area=B01
B03 8 10 jjmit area=B03
B04 23 19 jjmit area=B03
B05 9 11 jjmit area=B05
B06 24 11 jjmit area=B05
B07 16 49 jjmit area=B07
B08 15 47 jjmit area=B08
B09 17 51 jjmit area=B09
B10 6 30 jjmit area=B10
B11 21 62 jjmit area=B10
B14 14 45 jjmit area=B14
IB01 0 26 pwl(0 0 5p IB01)
IB01RX1 0 25 pwl(0 0 5p IB01rx2)
IB01RX2 0 55 pwl(0 0 5p IB01rx2)
IB01RX3 0 36 pwl(0 0 5p IB01rx3)
IB01TX1 0 39 pwl(0 0 5p IB01tx1)
IB02 0 56 pwl(0 0 5p IB01)
IB03 0 38 pwl(0 0 5p IB03)
IB07 0 37 pwl(0 0 5p IB07)
L01 8 9 L01
L01RX1 a 5 L01rx2
L01RX2 b 20 L01rx2
L01RX3 clk 13 L01rx3
L01TX1 17 18 L01tx1
L02 23 24 L01
L02TX1 18 42 L02tx1
L03 6 27 L03
L04 21 59 L03
L05 10 12 L05
L06 12 19 L05
L07 40 15 L07
L08 16 41 L08
L09 41 17 L09
L13 5 6 L13
L14 20 21 L13
L15 27 7 L15
L16 59 22 L15
L17 13 14 L17
L19 14 40 L19
L20 11 16 L20
L21 7 8 L21
L22 22 23 L21
L23 15 12 L23
LP01 32 0 2.55e-13
LP01RX1 28 0 3.4e-13
LP01RX2 60 0 3.4e-13
LP01RX3 43 0 3.4e-13
LP01TX1 53 0 5e-14
LP02 64 0 2.55e-13
LP07 49 0 2.99e-13
LP08 47 0 2.11e-13
LP09 51 0 1.74e-13
LP10 30 0 2.21e-13
LP11 62 0 2.21e-13
```

```
LP14 45 0 1.87e-13
LPR01RX1 25 5 2e-13
LPR01RX2 55 20 2e-13
LPR01RX3 36 13 2e-13
LPR01TX1 39 18 2e-13
LPR1 26 27 1.3e-14
LPR2 56 59 1.3e-14
LPR3 38 41 1.901e-12
LPR4 37 40 8.5e-13
LRB01 33 0 LRB01
LRB01RX1 29 0 LRB01rx2
LRB01RX2 61 0 LRB01rx2
LRB01RX3 44 0 LRB01rx3
LRB01TX1 54 0 LRB01tx1
LRB02 65 0 LRB01
LRB03 34 10 LRB03
LRB04 19 57 LRB03
LRB05 35 11 LRB05
LRB06 11 58 LRB05
LRB07 50 0 LRB07
LRB08 48 0 LRB08
LRB09 52 0 LRB09
LRB10 31 0 LRB10
LRB11 63 0 LRB10
LRB14 46 0 LRB14
RB01 7 33 RB01
RB01RX1 5 29 RB01rx2
RB01RX2 20 61 RB01rx2
RB01RX3 13 44 RB01rx3
RB01TX1 18 54 RB01tx1
RB02 22 65 RB01
RB03 8 34 RB03
RB04 57 23 RB03
RB05 9 35 RB05
RB06 58 24 RB05
RB07 16 50 RB07
RB08 15 48 RB08
RB09 17 52 RB09
RB10 6 31 RB10
RB11 21 63 RB10
RB14 14 46 RB14
RINSTX1 42 q 1.36
.ends
```

Listing 4.23: RSFQ AND2T JoSIM netlist.

Table 4.15: RSFQ AND2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ AND2T using JoSIM is shown in Fig. 4.38. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **b**,

(d) the phase over the input JJ of pin **b**,

(e) the current through the input inductor connected to pin **clk**,

(f) the phase over the input JJ of pin **clk**,

(g) the phase over the output JJ of pin **q**, and

(h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

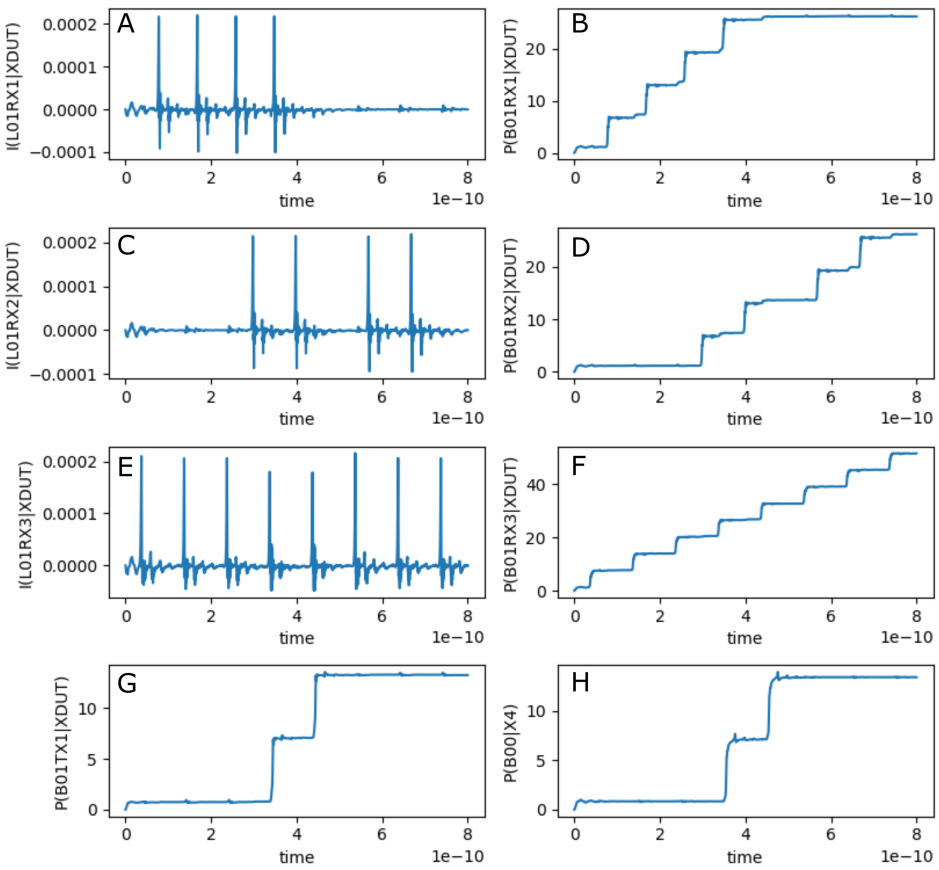

Figure 4.38: RSFQ AND2T analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_AND2T_v1p5 (a, b, clk, q);

input
  a, b, clk;

output
  q;

reg
  q;

real
  delay_state3_clk_q = 7.0,
  ct_state0_clk_a = 3.3,
  ct_state0_clk_b = 3.3,
  ct_state1_clk_a = 2.5,
  ct_state1_clk_b = 2.8,
  ct_state2_clk_a = 2.8,
  ct_state2_clk_b = 2.5,
  ct_state3_clk_a = 1.8,
  ct_state3_clk_b = 1.5;

reg
   errorsignal_a,
   errorsignal_b,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                        end
```

```
67                      1: begin
68                         end
69                      2: begin
70                            cell_state = 3;  // Blocking statement -- immediately
71                         end
72                      3: begin
73                         end
74                   endcase
75                end
76          end
77    end
78
79 always @(posedge b or negedge b) // execute at positive and negative edges of input
80    begin
81       if ($time>4) // arbitrary steady-state time)
82          begin
83             if (errorsignal_b == 1'b1)  // A critical timing is active for this input
84                begin
85                   outfile = $fopen("errors.txt", "a");
86                   $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                        ↪ ", $stime);
87                   $fclose(outfile);
88                   q <= 1'bX;  // Set all outputs to unknown
89                end
90             if (errorsignal_b == 0)
91                begin
92                   case (cell_state)
93                      0: begin
94                            cell_state = 2;  // Blocking statement -- immediately
95                         end
96                      1: begin
97                            cell_state = 3;  // Blocking statement -- immediately
98                         end
99                      2: begin
100                        end
101                     3: begin
102                        end
103                  endcase
104               end
105         end
106   end
107
108 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
109   begin
110      if ($time>4) // arbitrary steady-state time)
111         begin
112            if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
113               begin
114                  outfile = $fopen("errors.txt", "a");
115                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                        ↪ ", $stime);
116                  $fclose(outfile);
117                  q <= 1'bX;  // Set all outputs to unknown
118               end
119            if (errorsignal_clk == 0)
120               begin
121                  case (cell_state)
122                     0: begin
123                           errorsignal_a = 1;  // Critical timing on this input; assign
                              ↪ immediately
124                           errorsignal_a <= #(ct_state0_clk_a) 0;  // Clear error signal
                              ↪ after critical timing expires
125                           errorsignal_b = 1;  // Critical timing on this input; assign
                              ↪ immediately
126                           errorsignal_b <= #(ct_state0_clk_b) 0;  // Clear error signal
                              ↪ after critical timing expires
127                        end
128                     1: begin
129                           cell_state = 0;  // Blocking statement -- immediately
130                           errorsignal_a = 1;  // Critical timing on this input; assign
```

```
                                ↪ immediately
131                             errorsignal_a <= #(ct_state1_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
132                             errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
133                             errorsignal_b <= #(ct_state1_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
134                          end
135                       2: begin
136                             cell_state = 0;  // Blocking statement -- immediately
137                             errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
138                             errorsignal_a <= #(ct_state2_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
139                             errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
140                             errorsignal_b <= #(ct_state2_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
141                          end
142                       3: begin
143                             q <= #(delay_state3_clk_q) !q;
144                             cell_state = 0;  // Blocking statement -- immediately
145                             errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
146                             errorsignal_a <= #(ct_state3_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
147                             errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
148                             errorsignal_b <= #(ct_state3_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
149                          end
150                    endcase
151                 end
152           end
153     end
154
155 endmodule
```

Listing 4.24: RSFQ AND2T verilog model.

The digital simulation results for the RSFQ AND2T is shown in Fig. 4.39 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.40.

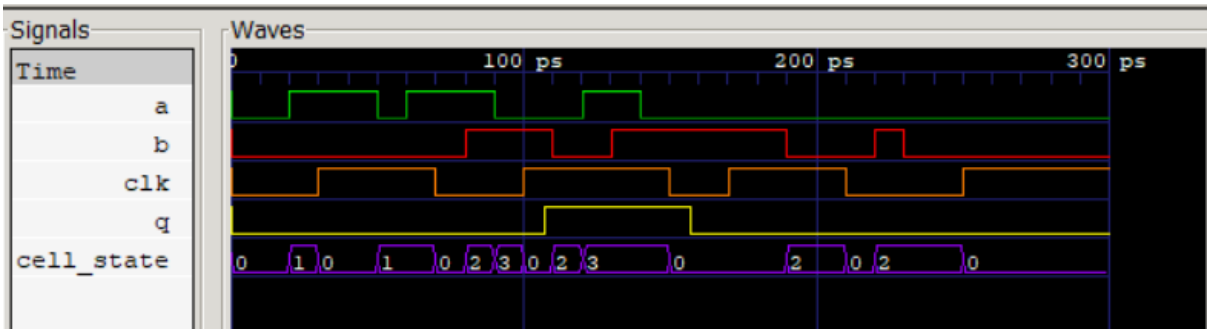

Figure 4.39: RSFQ AND2T digital simulation results.

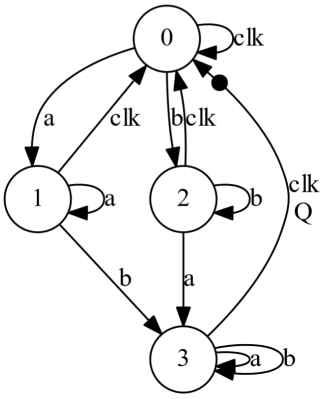

Figure 4.40: RSFQ AND2T Mealy finite state machine diagram.

Power Consumption

Table 4.16: RSFQ AND2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	279	4.71
2	279	9.42
5	279	23.5
10	279	47.1
20	279	94.2
50	279	235

4.2.2 OR2T

The RSFQ OR2T cell generates an output pulse if an input pulse from either input lines was received before the clock signal. The OR2T cell is designed with integrated PTL transmitters and receivers and is intended to be connected directly to a PTL.

Schematic

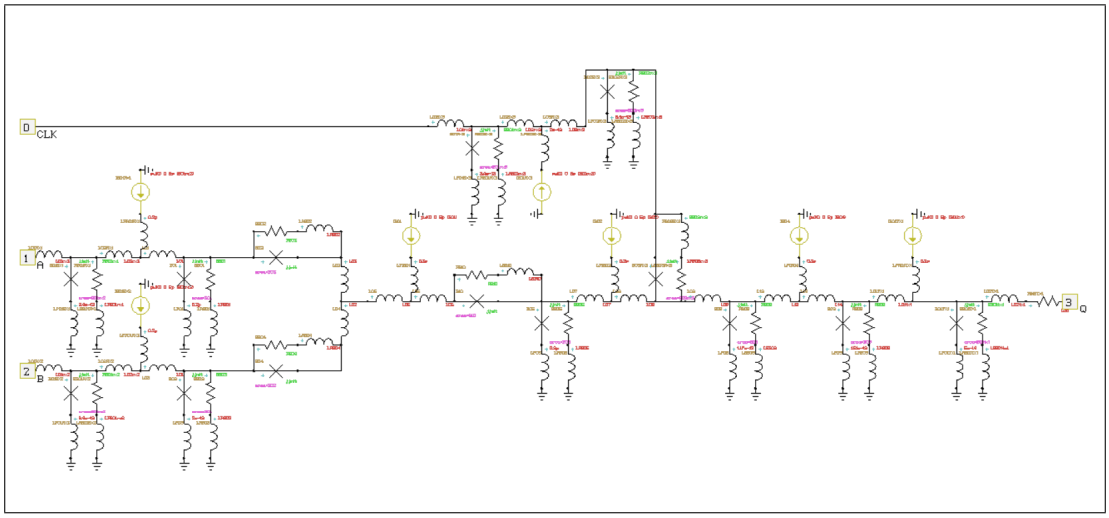

Figure 4.41: Schematic of RSFQ OR2T.

Layout

The physical layout for the RSFQ OR2T is shown in Fig. 4.42 and the resulting InductEx extraction is shown in Listing 4.25. The layout height is 70 μm and the width is 100 μm.

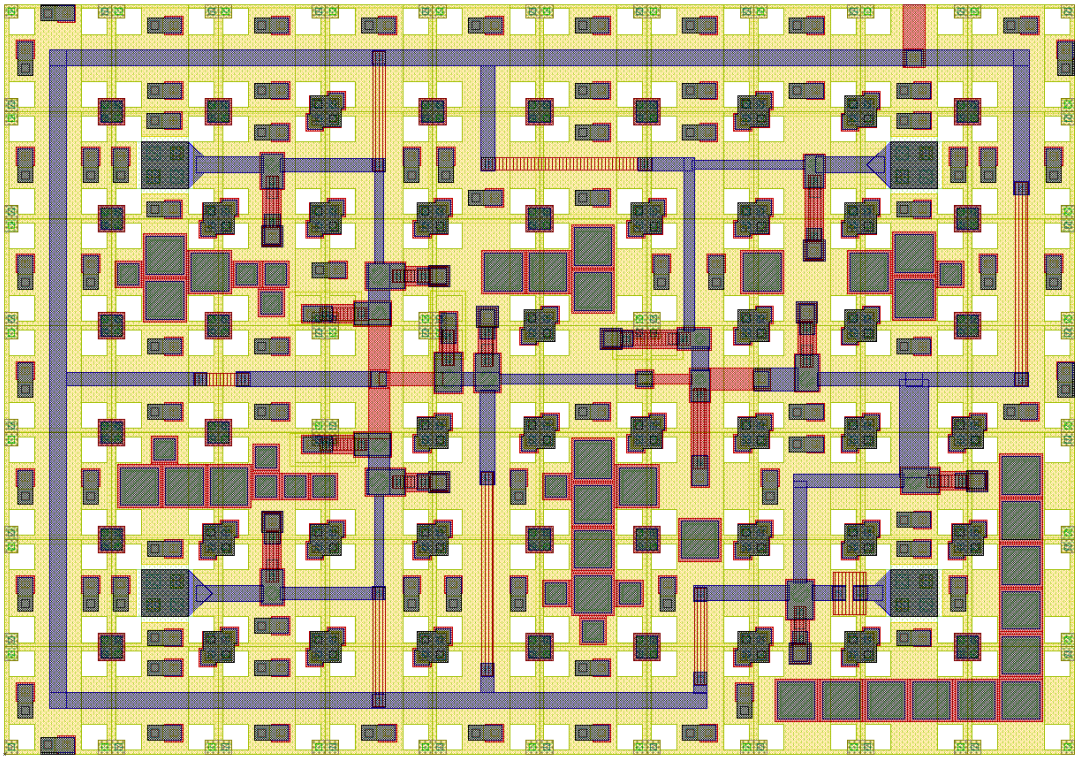

Figure 4.42: RSFQ OR2T Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_OR2T_v1p5.GDS -n LSmitll_OR2T_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_OR2T_v1p5_idx.cir read. Totals: L = 36, k = 0, P = 25.
Total fundamental loops identified in netlist = 20
Using TetraHenry with analytical integration.
3019 structures read. Reduced 3019 objects to 2798 polygons and 11 terminals.
Top level structure is "LSMITLL_OR2T_V1P5".
GDS file LSmitll_OR2T_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Port clk not in netlist. Ignored.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Object in layer I5 moved to TERM layer. (Pj5)
Object in layer I5 moved to TERM layer. (Pj6)
Object in layer I5 moved to TERM layer. (Pj7)
Object in layer I5 moved to TERM layer. (Pj8)
Object in layer I5 moved to TERM layer. (Pj9)
Object in layer I5 moved to TERM layer. (Pj10)
Object in layer I5 moved to TERM layer. (Pj11)
Object in layer I5 moved to TERM layer. (Pj12)
Object in layer I5 moved to TERM layer. (Pj13)
Object in layer I5 moved to TERM layer. (Pj14)
Terminal blocks = 25; Labels = 26; Extracted Ports = 25

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
P3                    M6,   line along y;  M4,   same as "+" terminal.
P4                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
PB5                   M6,   polygon;       M4,   same as "+" terminal.
PB6                   M6,   polygon;       M4,   same as "+" terminal.
PB7                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M5,   polygon;       M6,   same as "+" terminal.
J8                    M6,   polygon;       M5,   same as "+" terminal.
J9                    M6,   polygon;       M5,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.
J11                   M6,   polygon;       M5,   same as "+" terminal.
J12                   M6,   polygon;       M5,   same as "+" terminal.
J13                   M6,   polygon;       M5,   same as "+" terminal.
J14                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 15.36; unknowns = 72; rank = 72.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.56576E-12 --          --          +1.5658E-12 --%
L2        2.0822E-12  2.07611E-12 --          --          -6.0936E-15 -0.29265%
L3        2.6809E-12  2.67435E-12 --          --          -6.5483E-15 -0.24426%
L4        1.3486E-12  1.34248E-12 --          --          -6.1193E-15 -0.45375%
L5        --          1.5833E-12  --          --          +1.5833E-12 --%
L6        2.0822E-12  2.08865E-12 --          --          +6.4494E-15 +0.30974%
L7        2.6809E-12  2.67708E-12 --          --          -3.8191E-15 -0.14246%
L8        1.3486E-12  1.34422E-12 --          --          -4.3756E-15 -0.32445%
L10       1.889E-12   1.87128E-12 --          --          -1.772E-14  -0.93806%
L12       5.4916E-12  5.43634E-12 --          --          -5.5265E-14 -1.0063%
L13       --          1.4674E-12  --          --          +1.4674E-12 --%
```

```
L14       3.3652E-12  3.35955E-12 --          --          -5.65E-15   -0.1679%
L15       4.0267E-12  3.98704E-12 --          --          -3.9664E-14 -0.98503%
L16       --          5.9501E-13  --          --          +5.9501E-13 --%
L17       1.5727E-12  1.5753E-12  --          --          +2.5958E-15 +0.16505%
L18       2.0776E-12  2.05735E-12 --          --          -2.0246E-14 -0.97449%
L19       8.85E-13    9.05707E-13 --          --          +2.0707E-14 +2.3397%
L20       4.2904E-12  4.29095E-12 --          --          +5.5498E-16 +0.012935%
L21       --          7.63945E-13 --          --          +7.6394E-13 --%
LB1       --          2.75189E-13 --          --          +2.7519E-13 --%
LB2       --          2.78685E-13 --          --          +2.7868E-13 --%
LB3       --          2.83116E-12 --          --          +2.8312E-12 --%
LB4       --          1.91903E-12 --          --          +1.919E-12  --%
LB5       --          1.13608E-12 --          --          +1.1361E-12 --%
LB6       --          2.21616E-12 --          --          +2.2162E-12 --%
LB7       --          2.02089E-12 --          --          +2.0209E-12 --%
LP1       --          4.89448E-13 --          --          +4.8945E-13 --%
LP2       --          4.67731E-13 --          --          +4.6773E-13 --%
LP4       --          4.85068E-13 --          --          +4.8507E-13 --%
LP5       --          4.66522E-13 --          --          +4.6652E-13 --%
LP8       --          5.07324E-13 --          --          +5.0732E-13 --%
LP9       --          5.24369E-13 --          --          +5.2437E-13 --%
LP10      --          5.47545E-13 --          --          +5.4754E-13 --%
LP12      --          4.82536E-13 --          --          +4.8254E-13 --%
LP13      --          5.2846E-13  --          --          +5.2846E-13 --%
LP14      --          4.44578E-13 --          --          +4.4458E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000117    0.0001249
J2        0.000195    0.00020358
J3        0.000131    0.00013903
J4        0.000117    0.0001249
J5        0.000195    0.00020358
J6        0.000131    0.00013903
J7        0.00022     0.00022853
J8        0.000172    0.00018001
J9        0.000081    0.000088493
J10       0.000075    0.000082555
J11       0.000063    0.000070413
J12       0.00014     0.00014826
J13       0.000162    0.00017055
J14       0.00019     0.0001986

Error bound on extracted values: 5.59447%

Deallocating memory.
Cycles found in 0.033 seconds.
SVD solution in 0.039 seconds.
Job finished in 440.152 seconds.
```

Listing 4.25: RSFQ OR2T InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                          a b clk q
.subckt LSmitll_OR2T a b clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap
    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
    ↪ )
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01=1.9518
.param B01rx2=1.1720
.param B01rx3=0.8056
.param B01tx1=1.9004
.param B02=1.3074
.param B02rx3=0.7521
.param B03rx3=0.6339
.param B05=1.7221
.param B08=1.3953
.param B09=1.6170
.param B10=2.2048
.param IB01=0.0003277005
.param IB01rx2=0.0001412752
.param IB01rx3=9.8325e-05
.param IB01tx1=0.0001765029
.param IB02=8.1358e-05
.param IB04=8.0964e-05
.param L01=2.6809e-12
.param L01rx2=2.0307e-12
.param L01rx3=1.4136e-12
.param L01tx1=4.2904e-12
.param L02=1.3486e-12
.param L02rx2=2.0822e-12
.param L02rx3=3.3652e-12
.param L02tx1=2.7779e-12
.param L03rx3=4.0267e-12
.param L05=3.7250e-13
.param L06=1.8890e-12
.param L07=2.1922e-13
.param L08=5.4916e-12
.param L09=1.5727e-12
.param L13=2.0776e-12
.param L14=8.8496e-13
.param LRB01=(RB01/Rsheet)*Lsheet
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
.param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB02=(RB02/Rsheet)*Lsheet
.param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
.param LRB03=(RB03/Rsheet)*Lsheet
.param LRB03rx3=(RB03rx3/Rsheet)*Lsheet
.param LRB04=(RB04/Rsheet)*Lsheet
.param LRB05=(RB05/Rsheet)*Lsheet
.param LRB08=(RB08/Rsheet)*Lsheet
.param LRB09=(RB09/Rsheet)*Lsheet
.param LRB10=(RB10/Rsheet)*Lsheet
.param RB01=B0Rs/B01
.param RB01rx1=B0Rs/B01rx2
.param RB01rx2=B0Rs/B01rx2
.param RB01rx3=B0Rs/B01rx3
.param RB01tx1=B0Rs/B01tx1
.param RB02=B0Rs/B02
.param RB02rx3=B0Rs/B02rx3
.param RB03=B0Rs/B01
.param RB03rx3=B0Rs/B03rx3
.param RB04=B0Rs/B02
.param RB05=B0Rs/B05
.param RB08=B0Rs/B08
.param RB09=B0Rs/B09
.param RB10=B0Rs/B10
B01 7 36 jjmit area=B01
B01rx1 9 34 jjmit area=B01rx2
B01rx2 19 54 jjmit area=B01rx2
B01rx3 6 23 jjmit area=B01rx3
B01tx1 16 50 jjmit area=B01tx1
B02 7 8 jjmit area=B02
B02rx3 5 20 jjmit area=B02rx3
B03 17 56 jjmit area=B01
B03rx3 5 13 jjmit area=B03rx3
B04 17 18 jjmit area=B02
B05 11 44 jjmit area=B05
B08 14 46 jjmit area=B08
B09 15 48 jjmit area=B09
B10 10 11 jjmit area=B10
IB01 0 28 pwl(0 0 5p IB01)
IB01rx1 0 26 pwl(0 0 5p IB01rx2)
IB01rx2 0 42 pwl(0 0 5p IB01rx2)
IB01rx3 0 25 pwl(0 0 5p IB01rx3)
IB01tx1 0 32 pwl(0 0 5p IB01tx1)
IB02 0 29 pwl(0 0 5p IB02)
IB04 0 31 pwl(0 0 5p IB04)
L01 27 7 L01
L01rx1 a 9 L01rx2
L01rx2 b 19 L01rx2
L01rx3 clk 6 L01rx3
L01tx1 15 16 L01tx1
L02 8 12 L02
L02rx1 9 27 L02rx2
L02rx2 19 52 L02rx2
L02rx3 6 22 L02rx3
L02tx1 16 43 L02tx1
L03 52 17 L01
L03rx3 22 5 L03rx3
L04 12 18 L02
L05 12 38 L05
L06 38 10 L06
L07 11 39 L07
L08 39 13 L08
L09 13 14 L09
L13 14 40 L13
L14 40 15 L14
LP01 36 0 0.2p
LP01rx1 34 0 3.4e-13
LP01rx2 54 0 3.4e-13
LP01rx3 23 0 3.4e-13
LP01tx1 50 0 5e-14
LP02rx3 20 0 3.4e-13
LP03 56 0 2e-13
LP05 44 0 0.2p
LP08 46 0 1.17e-13
LP09 48 0 1.51e-13
LPIB01 28 38 0.2p
LPIB02 29 39 0.2p
LPIB04 31 40 0.2p
LPR01rx1 26 27 0.2p
```

```
LPR01rx2 42 52 0.2p
LPR01rx3 22 25 2e-13
LPR01tx1 32 16 0.2p
LRB01 37 0 LRB01
LRB01rx1 35 0 LRB01rx1
LRB01rx2 55 0 LRB01rx2
LRB01rx3 24 0 LRB01rx3
LRB01tx1 51 0 LRB01tx1
LRB02 33 8 LRB02
LRB02rx3 21 0 LRB02rx3
LRB03 57 0 LRB03
LRB03rx3 30 13 LRB03rx3
LRB04 53 18 LRB04
LRB05 45 0 LRB05
LRB08 47 0 LRB08
LRB09 49 0 LRB09
LRB10 41 11 LRB10
RB01 7 37 RB01
RB01rx1 9 35 RB01rx1
RB01rx2 19 55 RB01rx2
RB01rx3 6 24 RB01rx3
RB01tx1 16 51 RB01tx1
RB02 7 33 RB02
RB02rx3 5 21 RB02rx3
RB03 17 57 RB03
RB03rx3 5 30 RB03rx3
RB04 17 53 RB04
RB05 11 45 RB05
RB08 14 47 RB08
RB09 15 49 RB09
RB10 10 41 RB10
RINStx1 43 q 1.36
.ends
```

Listing 4.26: RSFQ OR2T JoSIM netlist.

Table 4.17: RSFQ OR2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ OR2T using JoSIM is shown in Fig. 4.43. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **b**,

(d) the phase over the input JJ of pin **b**,

(e) the current through the input inductor connected to pin **clk**,

(f) the phase over the input JJ of pin **clk**,

(g) the phase over the output JJ of pin **q**, and

(h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

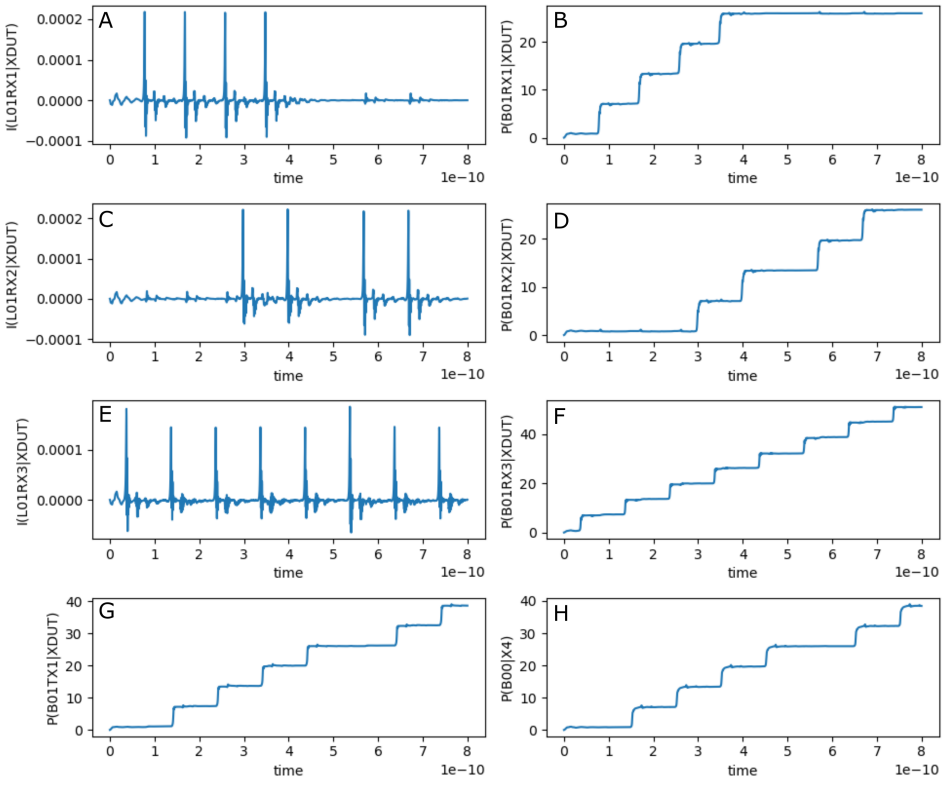

Figure 4.43: RSFQ OR2T analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_OR2T_v1p5 (a, b, clk, q);

input
  a, b, clk;
output
  q;
reg
  q;

real
  delay_state1_clk_q = 5.5,
  ct_state0_a_clk = 2.3,
  ct_state0_b_clk = 2.3,
  ct_state1_a_clk = 1.6,
  ct_state1_b_clk = 1.6;

reg
   errorsignal_a,
   errorsignal_b,
   errorsignal_clk;
integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                           errorsignal_clk = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_clk <= #(ct_state0_a_clk) 0;  // Clear error signal
                               ↪  after critical timing expires
                        end
                     1: begin
                           errorsignal_clk = 1;  // Critical timing on this input; assign
                               ↪ immediately
```

```
64                          errorsignal_clk <= #(ct_state1_a_clk) 0;  // Clear error signal
                                ↪  after critical timing expires
65                      end
66                  endcase
67              end
68          end
69      end
70
71  always @(posedge b or negedge b) // execute at positive and negative edges of input
72      begin
73          if ($time>4) // arbitrary steady-state time)
74              begin
75                  if (errorsignal_b == 1'b1)  // A critical timing is active for this input
76                      begin
77                          outfile = $fopen("errors.txt", "a");
78                          $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                                ↪ ", $stime);
79                          $fclose(outfile);
80                          q <= 1'bX;  // Set all outputs to unknown
81                      end
82                  if (errorsignal_b == 0)
83                      begin
84                          case (cell_state)
85                              0: begin
86                                     cell_state = 1;  // Blocking statement -- immediately
87                                     errorsignal_clk = 1;  // Critical timing on this input; assign
                                           ↪ immediately
88                                     errorsignal_clk <= #(ct_state0_b_clk) 0;  // Clear error signal
                                           ↪  after critical timing expires
89                                 end
90                              1: begin
91                                     errorsignal_clk = 1;  // Critical timing on this input; assign
                                           ↪ immediately
92                                     errorsignal_clk <= #(ct_state1_b_clk) 0;  // Clear error signal
                                           ↪  after critical timing expires
93                                 end
94                          endcase
95                      end
96              end
97      end
98
99  always @(posedge clk or negedge clk) // execute at positive and negative edges of input
100     begin
101         if ($time>4) // arbitrary steady-state time)
102             begin
103                 if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
104                     begin
105                         outfile = $fopen("errors.txt", "a");
106                         $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                                ↪ ", $stime);
107                         $fclose(outfile);
108                         q <= 1'bX;  // Set all outputs to unknown
109                     end
110                 if (errorsignal_clk == 0)
111                     begin
112                         case (cell_state)
113                             0: begin
114                                end
115                             1: begin
116                                    q <= #(delay_state1_clk_q) !q;
117                                    cell_state = 0;  // Blocking statement -- immediately
118                                end
119                         endcase
120                     end
121             end
122     end
123 endmodule
```

Listing 4.27: RSFQ OR2T verilog model.

The digital simulation results for the RSFQ OR2T is shown in Fig. 4.44 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.45.

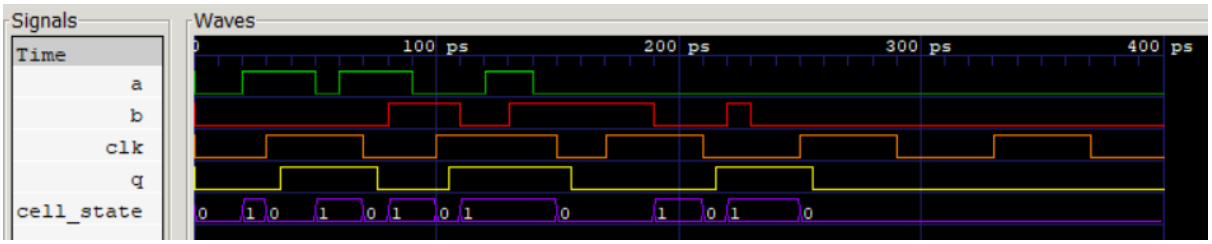

Figure 4.44: RSFQ OR2T digital simulation results.

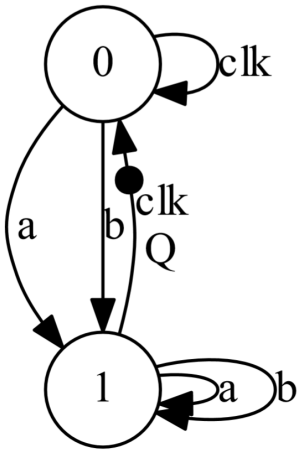

Figure 4.45: RSFQ OR2T Mealy finite state machine diagram.

Power Consumption

Table 4.18: RSFQ OR2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	272	4.11
2	272	8.23
5	272	20.6
10	272	41.1
20	272	82.3
50	272	206

4.2.3 XORT

The RSFQ XORT cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. The XORT cell is designed with integrated PTL transmitters and receivers and is intended to be connected directly to a PTL.

Schematic

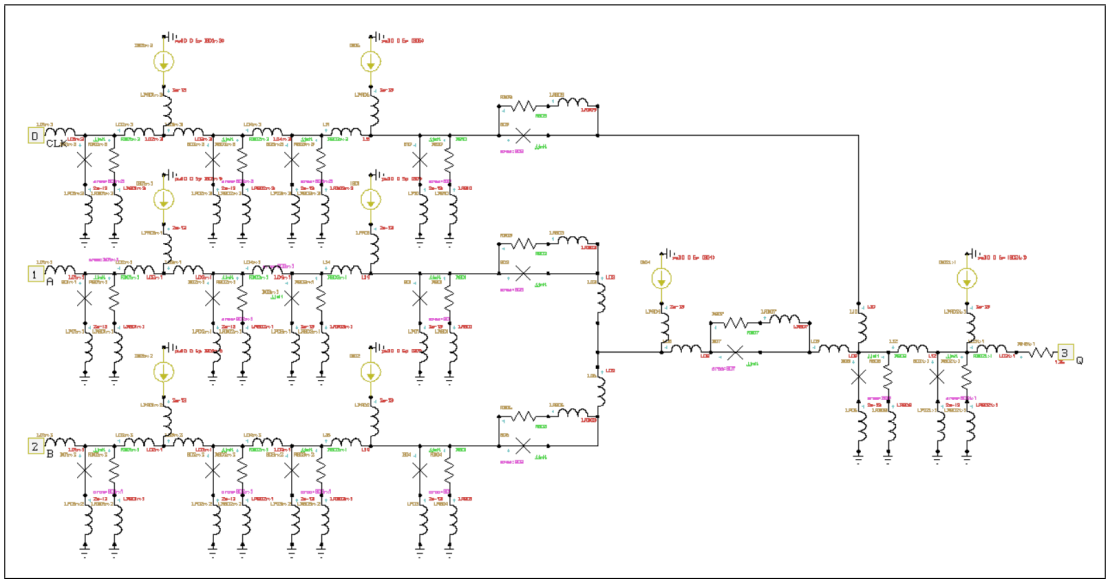

Figure 4.46: Schematic of RSFQ XORT.

Layout

The physical layout for the RSFQ XORT is shown in Fig. 4.47 and the resulting InductEx extraction is shown in Listing 4.28. The layout height is 70 μm and the width is 100 μm.

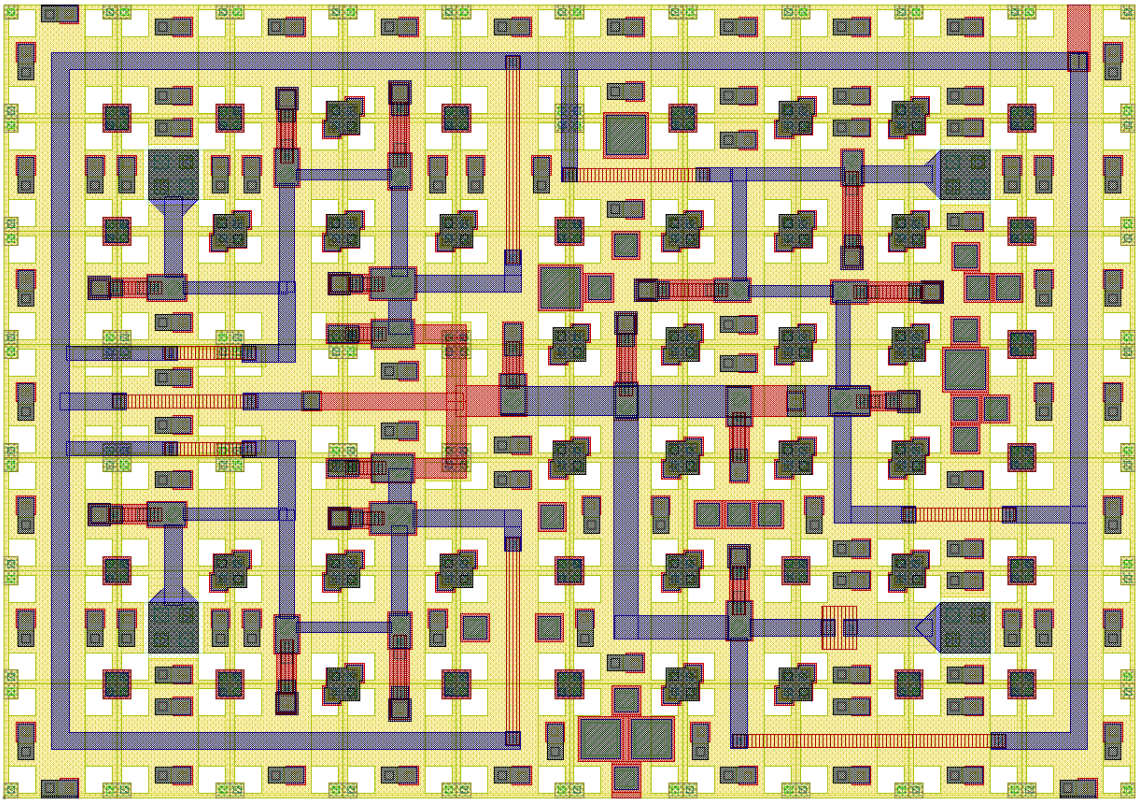

Figure 4.47: RSFQ XORT Layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_XORT_v1p5.GDS -n LSmitll_XORT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_XORT_v1p5_idx.cir read. Totals: L = 43, k = 0, P = 30.
7  Total fundamental loops identified in netlist = 25
8  Using TetraHenry with analytical integration.
9  2972 structures read. Reduced 2972 objects to 2763 polygons and 12 terminals.
10 Top level structure is "LSMITLL_XORT_V1P5".
11 GDS file LSmitll_XORT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 Port clk not in netlist. Ignored.
13 Object in layer I5 moved to TERM layer. (Pj1)
14 Object in layer I5 moved to TERM layer. (Pj2)
15 Object in layer I5 moved to TERM layer. (Pj3)
16 Object in layer I5 moved to TERM layer. (Pj4)
17 Object in layer I5 moved to TERM layer. (Pj5)
18 Object in layer I5 moved to TERM layer. (Pj6)
19 Object in layer I5 moved to TERM layer. (Pj7)
20 Object in layer I5 moved to TERM layer. (Pj8)
21 Object in layer I5 moved to TERM layer. (Pj9)
22 Object in layer I5 moved to TERM layer. (Pj10)
23 Object in layer I5 moved to TERM layer. (Pj11)
24 Object in layer I5 moved to TERM layer. (Pj12)
25 Object in layer I5 moved to TERM layer. (Pj13)
26 Object in layer I5 moved to TERM layer. (Pj14)
27 Object in layer I5 moved to TERM layer. (Pj15)
28 Object in layer I5 moved to TERM layer. (Pj16)
```

```
Object in layer I5 moved to TERM layer. (Pj17)
Object in layer I5 moved to TERM layer. (Pj18)
Terminal blocks = 30; Labels = 31; Extracted Ports = 30

Port                  Positive terminal    Negative terminal
P1                    M6,   line along x;  M4,   same as "+" terminal.
P2                    M6,   line along x;  M4,   same as "+" terminal.
P3                    M6,   line along y;  M4,   same as "+" terminal.
P4                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
PB5                   M6,   polygon;       M4,   same as "+" terminal.
PB6                   M6,   polygon;       M4,   same as "+" terminal.
PB7                   M6,   polygon;       M4,   same as "+" terminal.
PB8                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M6,   polygon;       M5,   same as "+" terminal.
J8                    M6,   polygon;       M5,   same as "+" terminal.
J9                    M6,   polygon;       M5,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.
J11                   M6,   polygon;       M5,   same as "+" terminal.
J12                   M6,   polygon;       M5,   same as "+" terminal.
J13                   M6,   polygon;       M5,   same as "+" terminal.
J14                   M6,   polygon;       M5,   same as "+" terminal.
J15                   M5,   polygon;       M6,   same as "+" terminal.
J16                   M5,   polygon;       M6,   same as "+" terminal.
J17                   M6,   polygon;       M5,   same as "+" terminal.
J18                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 5.664; unknowns = 86; rank = 86.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.43366E-12 --          --          +1.4337E-12 --%
L2        2.1529E-12  2.15066E-12 --          --          -2.2382E-15 -0.10396%
L3        1.9729E-12  1.95185E-12 --          --          -2.1048E-14 -1.0669%
L4        2.3966E-12  2.38059E-12 --          --          -1.6015E-14 -0.66823%
L5        1.6354E-12  1.63433E-12 --          --          -1.0673E-15 -0.065261%
L6        2.2793E-12  2.27355E-12 --          --          -5.75E-15   -0.25227%
L7        --          1.4265E-12  --          --          +1.4265E-12 --%
L8        2.1529E-12  2.15169E-12 --          --          -1.2074E-15 -0.056081%
L9        1.9729E-12  1.9544E-12  --          --          -1.8502E-14 -0.93781%
L10       2.3966E-12  2.3794E-12  --          --          -1.7199E-14 -0.71765%
L11       1.6354E-12  1.63063E-12 --          --          -4.7737E-15 -0.2919%
L12       2.2793E-12  2.27042E-12 --          --          -8.8785E-15 -0.38953%
L13       --          1.57592E-12 --          --          +1.5759E-12 --%
L14       2.2381E-12  2.25047E-12 --          --          +1.2371E-14 +0.55277%
L15       2.0205E-12  2.00348E-12 --          --          -1.7017E-14 -0.84223%
L16       2.0178E-12  2.02314E-12 --          --          +5.3403E-15 +0.26466%
L17       1.8033E-12  1.78416E-12 --          --          -1.9137E-14 -1.0612%
L18       2.2246E-12  2.18833E-12 --          --          -3.6268E-14 -1.6303%
L19       1.7515E-12  1.75481E-12 --          --          +3.3059E-15 +0.18874%
L20       3.8658E-12  3.88399E-12 --          --          +1.8187E-14 +0.47045%
L21       --          1.59174E-12 --          --          +1.5917E-12 --%
LP1       --          5.19299E-13 --          --          +5.193E-13  --%
LP2       --          5.79257E-13 --          --          +5.7926E-13 --%
LP3       --          5.76642E-13 --          --          +5.7664E-13 --%
LP4       --          4.79876E-13 --          --          +4.7988E-13 --%
LP6       --          5.2107E-13  --          --          +5.2107E-13 --%
LP7       --          5.75992E-13 --          --          +5.7599E-13 --%
LP8       --          5.77165E-13 --          --          +5.7716E-13 --%
LP9       --          4.781E-13   --          --          +4.781E-13  --%
LP11      --          5.184E-13   --          --          +5.184E-13  --%
```

```
LP12       --          6.01266E-13 --          --          +6.0127E-13 --%
LP13       --          5.96996E-13 --          --          +5.97E-13   --%
LP14       --          5.27298E-13 --          --          +5.273E-13  --%
LP17       --          5.93281E-13 --          --          +5.9328E-13 --%
LP18       --          5.33178E-13 --          --          +5.3318E-13 --%
LB1        --          1.86465E-12 --          --          +1.8647E-12 --%
LB2        --          2.30401E-12 --          --          +2.304E-12  --%
LB3        --          1.86071E-12 --          --          +1.8607E-12 --%
LB4        --          2.29666E-12 --          --          +2.2967E-12 --%
LB5        --          9.22503E-13 --          --          +9.225E-13  --%
LB6        --          2.91768E-12 --          --          +2.9177E-12 --%
LB7        --          4.09282E-12 --          --          +4.0928E-12 --%
LB8        --          2.01676E-12 --          --          +2.0168E-12 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         0.000121    0.00012895
J2         0.000116    0.00012397
J3         0.00009     0.00009764
J4         0.00028     0.00028898
J5         0.000192    0.00020036
J6         0.000121    0.00012895
J7         0.000116    0.00012397
J8         0.00009     0.00009764
J9         0.00028     0.00028898
J10        0.000192    0.00020036
J11        0.000072    0.00007941
J12        0.000077    0.000084655
J13        0.000083    0.0000907
J14        0.000169    0.00017758
J15        0.000129    0.00013711
J16        0.000149    0.00015691
J17        0.000093    0.00010059
J18        0.000137    0.00014499

Error bound on extracted values: 2.47313%

Deallocating memory.
Cycles found in 0.031 seconds.
SVD solution in 0.048 seconds.
Job finished in 558.757 seconds.
```

Listing 4.28: RSFQ XORT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                          a b clk q
.subckt LSmitll_XORT a b clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap
    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
    ↪ )
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01=2.7984
.param B01rx1=1.2124
.param B01rx3=0.7236
.param B02rx1=1.1586
.param B02rx3=0.7720
.param B02tx1=1.3695
.param B03=1.9159
.param B03rx1=0.8978
.param B03rx3=0.8280
.param B07=1.4857
.param B08=0.9336
.param B09=1.2859
.param B10=1.6863
.param IB01=8.9218e-05
.param IB01rx1=0.000229789
.param IB01rx3=0.000131858
.param IB02tx1=6.64568e-05
.param IB04=0.000134046
.param IB05=0.000177629
.param L01rx1=1.8604e-12
.param L01rx3=1.8928e-12
.param L02rx1=2.1529e-12
.param L02rx3=2.2381e-12
.param L03=2.2793e-12
.param L03rx1=1.9729e-12
.param L03rx3=2.0205e-12
.param L03tx1=2.2261e-12
.param L04rx1=2.3966e-12
.param L04rx3=2.0178e-12
.param L08=1.7515e-12
.param L09=1.2620e-12
.param L10=2.2246e-12
.param L11=1.8033e-12
.param L12=3.8658e-12
.param L14=1.6354e-12
.param LRB01=(RB01/Rsheet)*Lsheet
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
.param LRB02rx1=(RB02rx1/Rsheet)*Lsheet
.param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
.param LRB02tx1=(RB02tx1/Rsheet)*Lsheet
.param LRB03=(RB03/Rsheet)*Lsheet
.param LRB03rx1=(RB03rx1/Rsheet)*Lsheet
.param LRB03rx3=(RB03rx3/Rsheet)*Lsheet
.param LRB07=(RB07/Rsheet)*Lsheet
.param LRB08=(RB08/Rsheet)*Lsheet
.param LRB09=(RB09/Rsheet)*Lsheet
.param LRB10=(RB10/Rsheet)*Lsheet
.param RB01=B0Rs/B01
.param RB01rx1=B0Rs/B01rx1
.param RB01rx3=B0Rs/B01rx3
.param RB02rx1=B0Rs/B02rx1
.param RB02rx3=B0Rs/B02rx3
.param RB02tx1=B0Rs/B02tx1
.param RB03=B0Rs/B03
.param RB03rx1=B0Rs/B03rx1
.param RB03rx3=B0Rs/B03rx3
.param RB07=B0Rs/B07
.param RB08=B0Rs/B08
.param RB09=B0Rs/B09
.param RB10=B0Rs/B10
B01 10 49 jjmit area=B01
B01rx1 12 43 jjmit area=B01rx1
B01rx2 22 61 jjmit area=B01rx1
B01rx3 7 29 jjmit area=B01rx3
B02rx1 13 45 jjmit area=B02rx1
B02rx2 23 63 jjmit area=B02rx1
B02rx3 8 31 jjmit area=B02rx3
B02tx1 19 57 jjmit area=B02tx1
B03 10 11 jjmit area=B03
B03rx1 14 47 jjmit area=B03rx1
B03rx2 24 65 jjmit area=B03rx1
B03rx3 9 33 jjmit area=B03rx3
B04 20 67 jjmit area=B01
B06 20 21 jjmit area=B03
B07 16 17 jjmit area=B07
B08 18 55 jjmit area=B08
B09 5 6 jjmit area=B09
B10 5 35 jjmit area=B10
IB01 0 38 pwl(0 0 5p IB01)
IB01rx1 0 37 pwl(0 0 5p IB01rx1)
IB01rx2 0 53 pwl(0 0 5p IB01rx1)
IB01rx3 0 25 pwl(0 0 5p IB01rx3)
IB02 0 54 pwl(0 0 5p IB01)
IB02tx1 0 42 pwl(0 0 5p IB02tx1)
IB04 0 41 pwl(0 0 5p IB04)
IB05 0 26 pwl(0 0 5p IB05)
L01rx1 a 12 L01rx1
L01rx2 b 22 L01rx1
L01rx3 clk 7 L01rx3
L02rx1 12 39 L02rx1
L02rx2 22 59 L02rx1
L02rx3 7 27 L02rx3
L03 11 15 L03
L03rx1 39 13 L03rx1
L03rx2 59 23 L03rx1
L03rx3 27 8 L03rx3
L03tx1 19 52 L03tx1
L04rx1 13 14 L04rx1
L04rx2 23 24 L04rx1
L04rx3 8 9 L04rx3
L06 15 21 L03
L08 15 16 L08
L09 17 18 L09
L10 6 18 L10
L11 9 5 L11
L12 18 19 L12
L14 14 10 L14
L15 24 20 L14
LP01 49 0 2e-13
LP01rx1 43 0 2e-13
LP01rx2 61 0 2e-13
LP01rx3 29 0 2e-13
LP02rx1 45 0 2e-13
LP02rx2 63 0 2e-13
LP02rx3 31 0 2e-13
```

```
LP02tx1 57 0 2e-13
LP03 67 0 2e-13
LP03rx1 47 0 2e-13
LP03rx2 65 0 2e-13
LP03rx3 33 0 2e-13
LP05 55 0 2e-13
LP10 35 0 2e-13
LPR01 38 10 2e-13
LPR01rx1 37 39 2e-13
LPR01rx2 53 59 2e-13
LPR01rx3 25 27 2e-13
LPR02 54 20 2e-13
LPR02tx1 42 19 2e-13
LPR04 41 15 2e-13
LPR05 26 5 2e-13
LRB01 50 0 LRB01
LRB01rx1 44 0 LRB01rx1
LRB01rx2 62 0 LRB01rx1
LRB01rx3 30 0 LRB01rx3
LRB02rx1 46 0 LRB02rx1
LRB02rx2 64 0 LRB02rx1
LRB02rx3 32 0 LRB02rx3
LRB02tx1 58 0 LRB02tx1
LRB03 40 11 LRB03
LRB03rx1 48 0 LRB03rx1
LRB03rx2 66 0 LRB03rx1
LRB03rx3 34 0 LRB03rx3
LRB04 68 0 LRB01
LRB06 60 21 LRB03
LRB07 51 17 LRB07
LRB08 56 0 LRB08
LRB09 28 6 LRB09
LRB10 36 0 LRB10
RB01 10 50 RB01
RB01rx1 12 44 RB01rx1
RB01rx2 22 62 RB01rx1
RB01rx3 7 30 RB01rx3
RB02rx1 13 46 RB02rx1
RB02rx2 23 64 RB02rx1
RB02rx3 8 32 RB02rx3
RB02tx1 19 58 RB02tx1
RB03 10 40 RB03
RB03rx1 14 48 RB03rx1
RB03rx2 24 66 RB03rx1
RB03rx3 9 34 RB03rx3
RB04 20 68 RB01
RB06 20 60 RB03
RB07 16 51 RB07
RB08 18 56 RB08
RB09 5 28 RB09
RB10 5 36 RB10
RINStx1 52 q 1.36
.ends
```

Listing 4.29: RSFQ XORT JoSIM netlist.

Table 4.19: RSFQ XORT pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ XORT using JoSIM is shown in Fig. 4.48. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **b**,

(d) the phase over the input JJ of pin **b**,

(e) the current through the input inductor connected to pin **clk**,

(f) the phase over the input JJ of pin **clk**,

(g) the phase over the output JJ of pin **q**, and

(h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

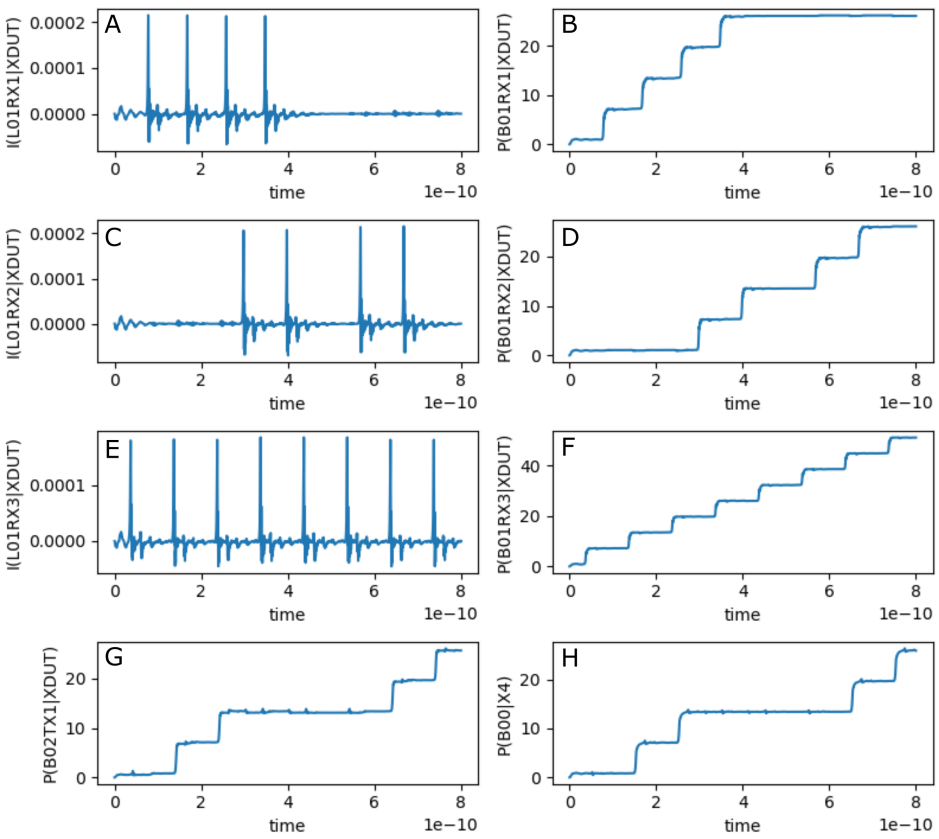

Figure 4.48: RSFQ XORT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_XORT_v1p5 (a, b, clk, q);

input
  a, b, clk;

output
  q;

reg
  q;

real
  delay_state1_clk_q = 5.2,
  delay_state2_clk_q = 5.2,
  ct_state0_a_clk = 2.5,
  ct_state0_b_clk = 2.5,
  ct_state1_a_b = 12.5,
  ct_state1_a_clk = 15.0,
  ct_state1_b_b = 3.3,
  ct_state1_clk_b = 3.8,
  ct_state2_a_a = 3.3,
  ct_state2_b_a = 12.5,
  ct_state2_b_clk = 15.0,
  ct_state2_clk_a = 3.8;

reg
   errorsignal_a,
   errorsignal_b,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
```

```
                    0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                           errorsignal_clk = 1;  // Critical timing on this input; assign immediately
                           errorsignal_clk <= #(ct_state0_a_clk) 0;  // Clear error signal after critical timing expires
                       end
                    1: begin
                           errorsignal_b = 1;  // Critical timing on this input; assign immediately
                           errorsignal_b <= #(ct_state1_a_b) 0;  // Clear error signal after critical timing expires
                           errorsignal_clk = 1;  // Critical timing on this input; assign immediately
                           errorsignal_clk <= #(ct_state1_a_clk) 0;  // Clear error signal after critical timing expires
                       end
                    2: begin
                           cell_state = 0;  // Blocking statement -- immediately
                           errorsignal_a = 1;  // Critical timing on this input; assign immediately
                           errorsignal_a <= #(ct_state2_a_a) 0;  // Clear error signal after critical timing expires
                       end
                endcase
            end
        end
    end

always @(posedge b or negedge b) // execute at positive and negative edges of input
    begin
        if ($time>4) // arbitrary steady-state time)
            begin
                if (errorsignal_b == 1'b1)  // A critical timing is active for this input
                begin
                    outfile = $fopen("errors.txt", "a");
                    $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n", $stime);
                    $fclose(outfile);
                    q <= 1'bX;  // Set all outputs to unknown
                end
                if (errorsignal_b == 0)
                begin
                    case (cell_state)
                        0: begin
                               cell_state = 2;  // Blocking statement -- immediately
                               errorsignal_clk = 1;  // Critical timing on this input; assign immediately
                               errorsignal_clk <= #(ct_state0_b_clk) 0;  // Clear error signal after critical timing expires
                           end
                        1: begin
                               cell_state = 0;  // Blocking statement -- immediately
                               errorsignal_b = 1;  // Critical timing on this input; assign immediately
                               errorsignal_b <= #(ct_state1_b_b) 0;  // Clear error signal after critical timing expires
                           end
                        2: begin
                               errorsignal_a = 1;  // Critical timing on this input; assign immediately
                               errorsignal_a <= #(ct_state2_b_a) 0;  // Clear error signal after critical timing expires
                               errorsignal_clk = 1;  // Critical timing on this input; assign immediately
                               errorsignal_clk <= #(ct_state2_b_clk) 0;  // Clear error signal after critical timing expires
                           end
                    endcase
                end
```

```
120         end
121    end
122
123 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
124    begin
125       if ($time>4) // arbitrary steady-state time)
126          begin
127             if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
128                begin
129                   outfile = $fopen("errors.txt", "a");
130                   $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                          ↪ ", $stime);
131                   $fclose(outfile);
132                   q <= 1'bX;  // Set all outputs to unknown
133                end
134             if (errorsignal_clk == 0)
135                begin
136                   case (cell_state)
137                      0: begin
138                         end
139                      1: begin
140                            q <= #(delay_state1_clk_q) !q;
141                            cell_state = 0;  // Blocking statement -- immediately
142                            errorsignal_b = 1;  // Critical timing on this input; assign
                                ↪ immediately
143                            errorsignal_b <= #(ct_state1_clk_b) 0;  // Clear error signal
                                ↪ after critical timing expires
144                         end
145                      2: begin
146                            q <= #(delay_state2_clk_q) !q;
147                            cell_state = 0;  // Blocking statement -- immediately
148                            errorsignal_a = 1;  // Critical timing on this input; assign
                                ↪ immediately
149                            errorsignal_a <= #(ct_state2_clk_a) 0;  // Clear error signal
                                ↪ after critical timing expires
150                         end
151                   endcase
152                end
153          end
154    end
155
156 endmodule
```

Listing 4.30: RSFQ XORT verilog model.

The digital simulation results for the RSFQ XORT is shown in Fig. 4.49 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.50.

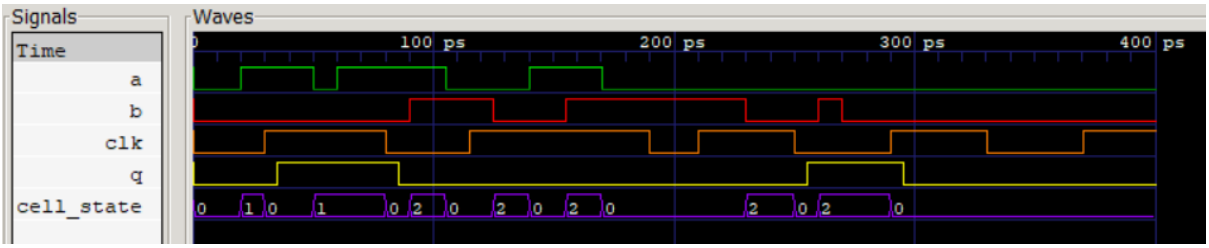

Figure 4.49: RSFQ XORT digital simulation results.

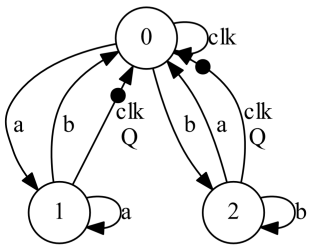

Figure 4.50: RSFQ XORT Mealy finite state machine diagram.

Power Consumption

Table 4.20: RSFQ XORT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	298	5.18
2	298	10.4
5	298	25.9
10	298	51.8
20	298	104
50	298	259

4.2.4 NOTT

The RSFQ NOTT cell is a signal inverting cell driven by a clock pulse signal line. The NOTT cell is designed with integrated PTL transmitters and receivers and is intended for direct connections with PTLs.

Schematic

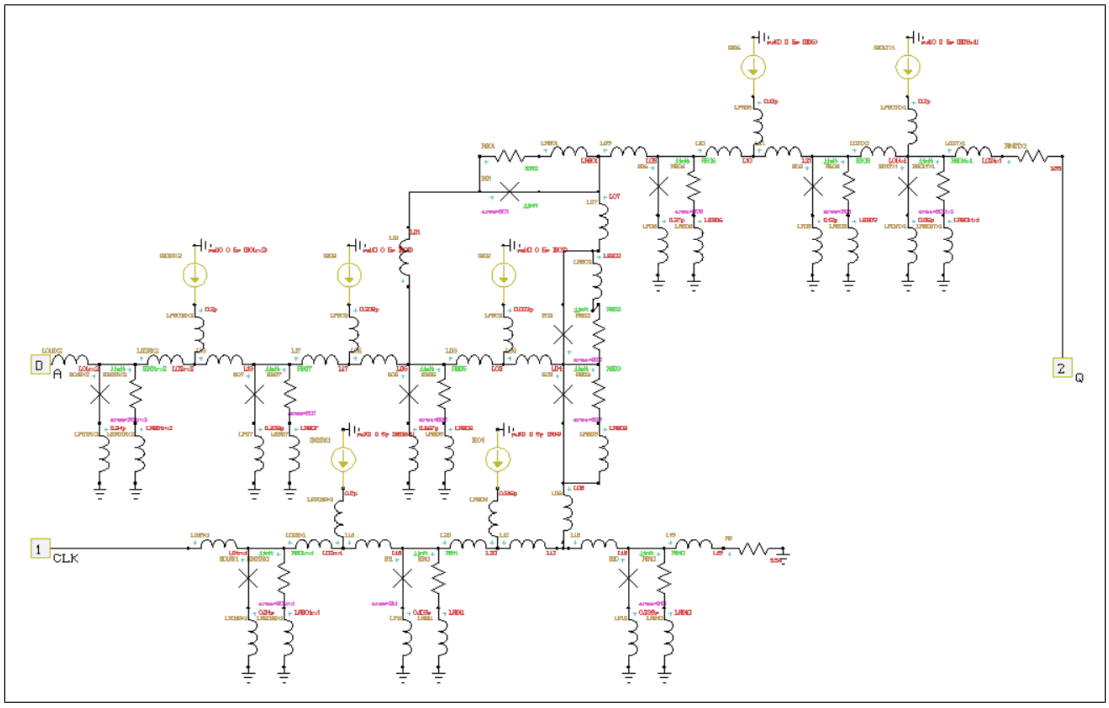

Figure 4.51: Schematic of RSFQ NOTT.

Layout

The physical layout for the RSFQ NOTT is shown in Fig. 4.52 and the resulting InductEx extraction is shown in Listing 4.31. The layout height is 70 μm and the width is 100 μm.

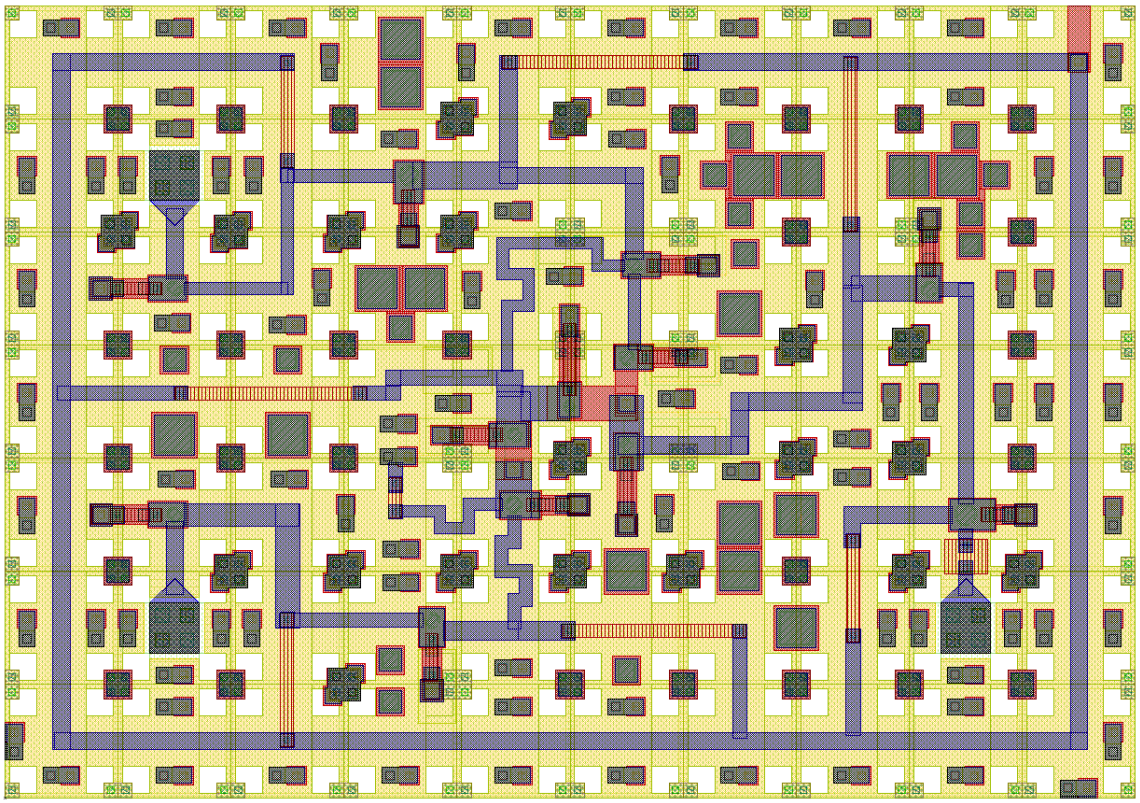

Figure 4.52: RSFQ NOTT Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_NOTT_v1p5.GDS -n LSmitll_NOTT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_NOTT_v1p5_idx.cir read. Totals: L = 37, k = 0, P = 23.
Total fundamental loops identified in netlist = 20
Using TetraHenry with analytical integration.
2868 structures read. Reduced 2868 objects to 2679 polygons and 11 terminals.
Top level structure is "LSMITLL_NOTT_V1P5".
GDS file LSmitll_NOTT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Port clk not in netlist. Ignored.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Object in layer I5 moved to TERM layer. (Pj5)
Object in layer I5 moved to TERM layer. (Pj6)
Object in layer I5 moved to TERM layer. (Pj7)
Object in layer I5 moved to TERM layer. (Pj8)
Object in layer I5 moved to TERM layer. (Pj9)
Object in layer I5 moved to TERM layer. (Pj10)
Object in layer I5 moved to TERM layer. (Pj11)
Object in layer I5 moved to TERM layer. (Pj12)
Terminal blocks = 23; Labels = 24; Extracted Ports = 23

Port                  Positive terminal    Negative terminal
P1                    M6,   line along x;  M4,   same as "+" terminal.
P2                    M6,   line along x;  M4,   same as "+" terminal.
P3                    M6,   polygon;       M4,   same as "+" terminal.
PR1                   M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
PB5                   M6,   polygon;       M4,   same as "+" terminal.
PB6                   M6,   polygon;       M4,   same as "+" terminal.
PB7                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M6,   polygon;       M5,   same as "+" terminal.
J8                    M6,   polygon;       M5,   same as "+" terminal.
J9                    M6,   polygon;       M5,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.
J11                   M6,   polygon;       M5,   same as "+" terminal.
J12                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 22.3; unknowns = 74; rank = 74.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.48938E-12 --          --          +1.4894E-12 --%
L2        2.5468E-12  2.56089E-12 --          --          +1.4091E-14 +0.55328%
L3        2.6117E-12  2.61229E-12 --          --          +5.8684E-16 +0.02247%
L4        1.1676E-12  1.17091E-12 --          --          +3.3091E-15 +0.28341%
L5        2.6532E-12  2.63295E-12 --          --          -2.0252E-14 -0.76332%
L7        3.1681E-12  3.08826E-12 --          --          -7.9836E-14 -2.52%
L8        8.6946E-13  9.61256E-13 --          --          +9.1796E-14 +10.558%
L9        --          1.46645E-12 --          --          +1.4664E-12 --%
L10       4.4718E-12  4.48451E-12 --          --          +1.2713E-14 +0.28429%
L11       2.1566E-12  2.17245E-12 --          --          +1.5845E-14 +0.73474%
L12       9.918E-13   1.00918E-12 --          --          +1.7376E-14 +1.752%
L13       3.286E-12   3.27206E-12 --          --          -1.3944E-14 -0.42436%
L14       6.5962E-12  6.56753E-12 --          --          -2.8666E-14 -0.43458%
L15       4.2413E-13  3.03051E-13 --          --          -1.2108E-13 -28.548%
L16       2.2847E-12  2.29566E-12 --          --          +1.096E-14  +0.47972%
```

```
L17        4.9986E-13  9.72893E-13 --          --          +4.7303E-13 +94.633%
L18        2.8417E-13  4.94044E-13 --          --          +2.0987E-13 +73.855%
L19        5.3651E-12  5.3561E-12  --          --          -8.9958E-15 -0.16767%
L20        7.4611E-13  7.4752E-13  --          --          +1.4102E-15 +0.18901%
L21        4.5195E-12  4.60071E-12 --          --          +8.1211E-14 +1.7969%
L22        --          5.80064E-13 --          --          +5.8006E-13 --%
LB1        --          3.14179E-13 --          --          +3.1418E-13 --%
LB2        --          1.10014E-12 --          --          +1.1001E-12 --%
LB3        --          5.15959E-13 --          --          +5.1596E-13 --%
LB4        --          1.95831E-12 --          --          +1.9583E-12 --%
LB5        --          2.94385E-12 --          --          +2.9438E-12 --%
LB6        --          1.30273E-12 --          --          +1.3027E-12 --%
LB7        --          2.38089E-12 --          --          +2.3809E-12 --%
LP1        --          5.25578E-13 --          --          +5.2558E-13 --%
LP2        --          4.98227E-13 --          --          +4.9823E-13 --%
LP3        --          5.10771E-13 --          --          +5.1077E-13 --%
LP6        --          5.23879E-13 --          --          +5.2388E-13 --%
LP7        --          4.79962E-13 --          --          +4.7996E-13 --%
LP8        --          5.71586E-13 --          --          +5.7159E-13 --%
LP10       --          5.92522E-13 --          --          +5.9252E-13 --%
LP11       --          4.98834E-13 --          --          +4.9883E-13 --%
LP12       --          3.90333E-13 --          --          +3.9033E-13 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         --          0.00013429
J2         --          0.00014995
J3         --          0.00018001
J4         --          0.00012983
J5         --          0.000084655
J6         --          0.00013321
J7         --          0.0002299
J8         --          0.00012983
J9         --          0.00014313
J10        --          0.00011204
J11        --          0.00014944
J12        --          0.00029325

Error bound on extracted values: 4.27715%

Deallocating memory.
Cycles found in 0.029 seconds.
SVD solution in 0.040 seconds.
Job finished in 434.799 seconds.
```

Listing 4.31: RSFQ NOTT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

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*For questions about the library, contact Lieze Schindler, 17528283@sun.ac.za

*$Ports                          a clk q
.subckt LSmitll_NOTT a clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01=1.3488
.param B01rx1=1.2613
.param B01rx2=1.2476
.param B01tx1=2.8510
.param B02=0.7718
.param B03=1.2227
.param B05=1.2221
.param B06=1.0432
.param B07=2.2139
.param B09=1.4100
.param B10=1.7227
.param B11=1.4193
.param IB01rx1=0.000146094
.param IB01rx2=0.000181215
.param IB01tx1=0.000187178
.param IB02=9.6978e-05
.param IB03=9.5221e-05
.param IB04=0.000101564
.param IB06=0.000108369
.param L01=2.2847e-12
.param L01rx1=1.8571e-12
.param L01rx2=2.1457e-12
.param L01tx1=4.5195e-12
.param L02rx1=4.4718e-12
.param L02rx2=2.5468e-12
.param L02tx1=3.4724e-12
.param L03=6.5962e-12
.param L04=4.2413e-13
.param L06=3.2860e-12
.param L07=4.9986e-13
.param L08=8.6946e-13
.param L09=2.8417e-13
.param L10=7.3651e-12
.param L12=2.6532e-12
.param L13=2.1566e-12
.param L16=2.6117e-12
.param L17=9.9180e-13
.param L18=2.5842e-13
.param L19=3.1681e-12
.param L20=1.1676e-12
.param L21=7.4611e-13
.param LRB01=(RB01/Rsheet)*Lsheet
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01rx2=(RB01rx2/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB02=(RB02/Rsheet)*Lsheet
.param LRB03=(RB03/Rsheet)*Lsheet
.param LRB05=(RB05/Rsheet)*Lsheet
.param LRB06=(RB06/Rsheet)*Lsheet
.param LRB07=(RB07/Rsheet)*Lsheet
.param LRB09=(RB09/Rsheet)*Lsheet
.param LRB10=(RB10/Rsheet)*Lsheet
.param LRB11=(RB11/Rsheet)*Lsheet
.param RB01=B0Rs/B01
.param RB01rx1=B0Rs/B01rx1
.param RB01rx2=B0Rs/B01rx2
.param RB01tx1=B0Rs/B01tx1
.param RB02=B0Rs/B02
.param RB03=B0Rs/B03
.param RB05=B0Rs/B05
.param RB06=B0Rs/B06
.param RB07=B0Rs/B07
.param RB09=B0Rs/B09
.param RB10=B0Rs/B10
.param RB11=B0Rs/B11
B01 4 5 jjmit area=B01
B01rx1 17 49 jjmit area=B01rx1
B01rx2 12 37 jjmit area=B01rx2
B01tx1 8 29 jjmit area=B01tx1
B02 14 9 jjmit area=B02
B03 14 15 jjmit area=B03
```

```
B05 10 41 jjmit area=B05
B06 6 25 jjmit area=B06
B07 13 39 jjmit area=B07
B09 7 27 jjmit area=B09
B10 19 53 jjmit area=B10
B11 18 51 jjmit area=B11
IB01rx1 0 44 pwl(0 0 5p IB01rx1)
IB01rx2 0 31 pwl(0 0 5p IB01rx2)
IB01tx1 0 21 pwl(0 0 5p IB01tx1)
IB02 0 33 pwl(0 0 5p IB02)
IB03 0 32 pwl(0 0 5p IB03)
IB04 0 45 pwl(0 0 5p IB04)
IB06 0 20 pwl(0 0 5p IB06)
L01 10 4 L01
L01rx1 a 17 L01rx1
L01rx2 clk 12 L01rx2
L01tx1 7 8 L01tx1
L02rx1 17 46 L02rx1
L02rx2 12 34 L02rx2
L02tx1 8 24 L02tx1
L03 10 36 L03
L04 36 14 L04
L06 35 10 L06
L07 5 9 L07
L08 15 16 L08
L09 5 6 L09
L10 6 22 L10
L12 47 16 L12
L13 34 13 L13
L16 46 18 L16
L17 13 35 L17
L18 16 19 L18
L19 19 48 L19
L20 18 47 L20
L21 22 7 L21
LP01rx1 49 0 0.34p
LP01rx2 37 0 0.34p
LP01tx1 29 0 0.05p
LP05 41 0 0.567p
LP06 25 0 0.27p
LP07 39 0 0.328p
LP09 27 0 0.12p
LP10 53 0 0.239p
LP11 51 0 0.109p
LPR01rx1 46 44 0.2p
LPR01rx2 31 34 0.2p
LPR01tx1 21 8 0.2p
LPR02 33 36 0.023p
LPR03 32 35 0.208p
LPR04 47 45 0.216p
LPR06 20 22 0.13p
LRB01 23 5 LRB01
LRB01rx1 50 0 LRB01rx1
LRB01rx2 38 0 LRB01rx2
LRB01tx1 30 0 LRB01tx1
LRB02 9 11 LRB02
LRB03 43 15 LRB03
LRB05 42 0 LRB05
LRB06 26 0 LRB06
LRB07 40 0 LRB07
LRB09 28 0 LRB09
LRB10 54 0 LRB10
LRB11 52 0 LRB11
RB01 4 23 RB01
RB01rx1 17 50 RB01rx1
RB01rx2 12 38 RB01rx2
RB01tx1 8 30 RB01tx1
RB02 11 14 RB02
RB03 14 43 RB03
RB05 10 42 RB05
RB06 6 26 RB06
RB07 13 40 RB07
RB09 7 28 RB09
RB10 19 54 RB10
RB11 18 52 RB11
RD 48 0 3.54
RINStx1 24 q 1.36
.ends
```

Listing 4.32: RSFQ NOTT JoSIM netlist.

Table 4.21: RSFQ NOTT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ NOTT using JoSIM is shown in Fig. 4.53. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **clk**,

(d) the phase over the input JJ of pin **clk**,

(e) the phase over the output JJ of pin **q**, and

(f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

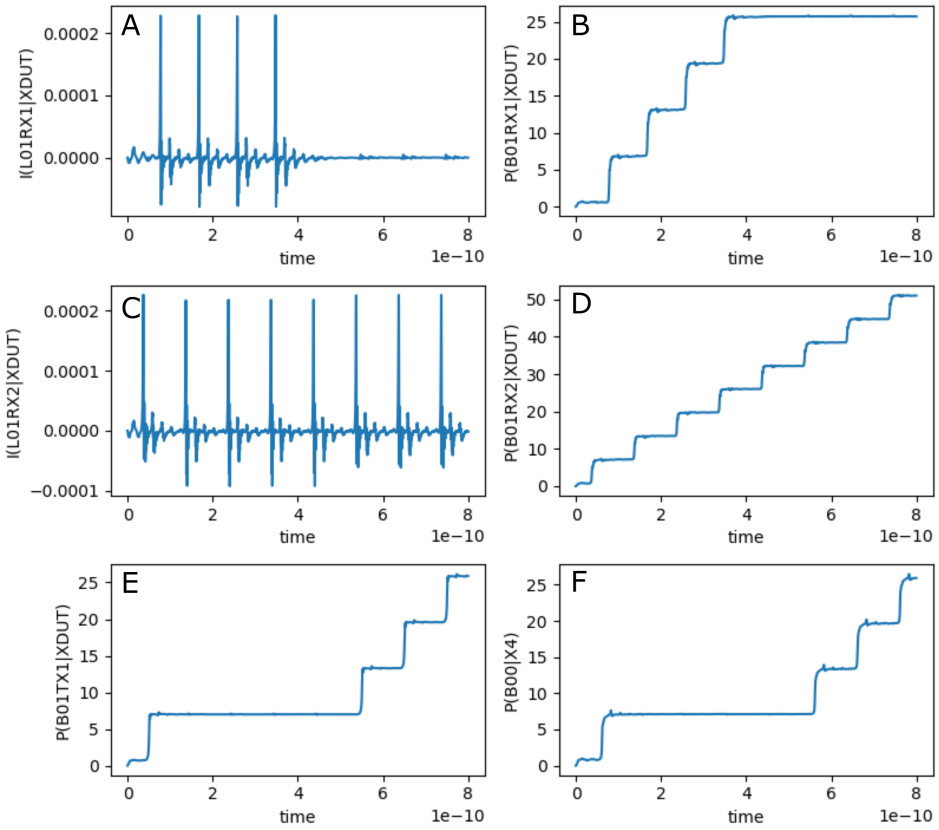

Figure 4.53: RSFQ NOTT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_NOTT_v1p5 (a, clk, q);

input
  a, clk;

output
  q;

reg
  q;

real
  delay_state0_clk_q = 13.5,
  ct_state0_clk_a = 6.6,
  ct_state0_clk_clk = 16.6,
  ct_state1_a_clk = 11.8;

reg
   errorsignal_a,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                        end
                     1: begin
                           errorsignal_clk = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_clk <= #(ct_state1_a_clk) 0;  // Clear error signal
                               ↪  after critical timing expires
                        end
                  endcase
```

```
65                end
66             end
67       end
68
69    always @(posedge clk or negedge clk) // execute at positive and negative edges of input
70       begin
71          if ($time>4) // arbitrary steady-state time)
72             begin
73                if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
74                   begin
75                      outfile = $fopen("errors.txt", "a");
76                      $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                            ↪ ", $stime);
77                      $fclose(outfile);
78                      q <= 1'bX;  // Set all outputs to unknown
79                   end
80                if (errorsignal_clk == 0)
81                   begin
82                      case (cell_state)
83                         0: begin
84                               q <= #(delay_state0_clk_q) !q;
85                               errorsignal_a = 1;  // Critical timing on this input; assign
                                    ↪ immediately
86                               errorsignal_a <= #(ct_state0_clk_a) 0;  // Clear error signal
                                    ↪ after critical timing expires
87                               errorsignal_clk = 1;  // Critical timing on this input; assign
                                    ↪ immediately
88                               errorsignal_clk <= #(ct_state0_clk_clk) 0;  // Clear error
                                    ↪ signal after critical timing expires
89                            end
90                         1: begin
91                               cell_state = 0;  // Blocking statement -- immediately
92                            end
93                      endcase
94                   end
95             end
96       end
97
98    endmodule
```

Listing 4.33: RSFQ NOTT verilog model.

The digital simulation results for the RSFQ NOTT is shown in Fig. 4.54 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.55.

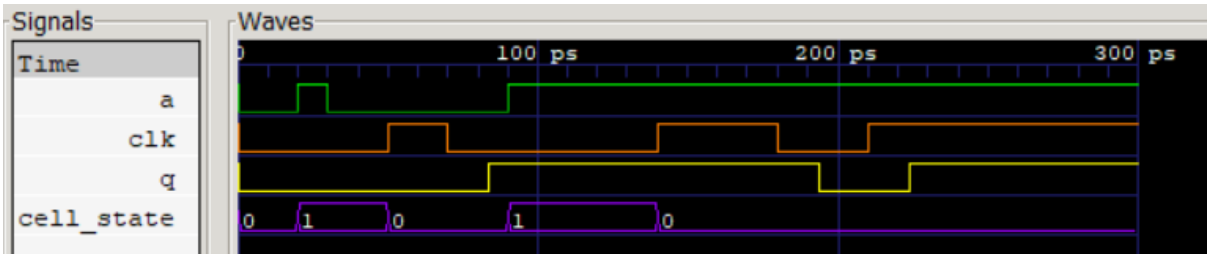

Figure 4.54: RSFQ NOTT digital simulation results.

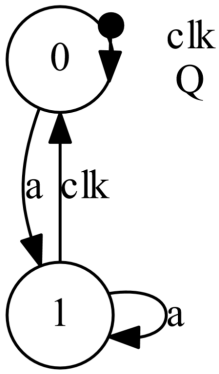

Figure 4.55: RSFQ NOTT Mealy finite state machine diagram.

Power Consumption

Table 4.22: RSFQ NOTT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	238	3.67
2	238	7.33
5	238	18.3
10	238	36.7
20	238	73.3
50	238	183

4.3 Buffers

4.3.1 DFFT

The RSFQ DFFT, D flip-flop, is a multi-state device used to transmit an input set pulse synchronised with a reset (typically clock) signal. The DFFT is designed with integrated PTL transmitters and receivers and is intended to connect directly to PTLs.

Schematic

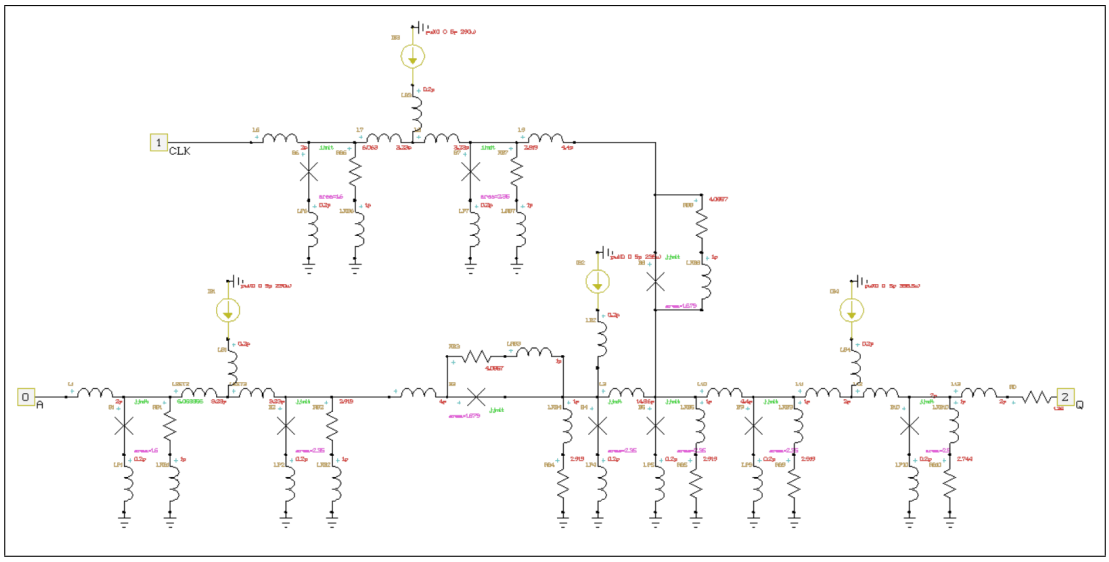

Figure 4.56: Schematic of RSFQ DFFT.

Layout

The physical layout for the RSFQ DFFT is shown in Fig. 4.57 and the resulting InductEx extraction is shown in Listing 4.34. The layout height is 70 μm and the width is 80 μm.

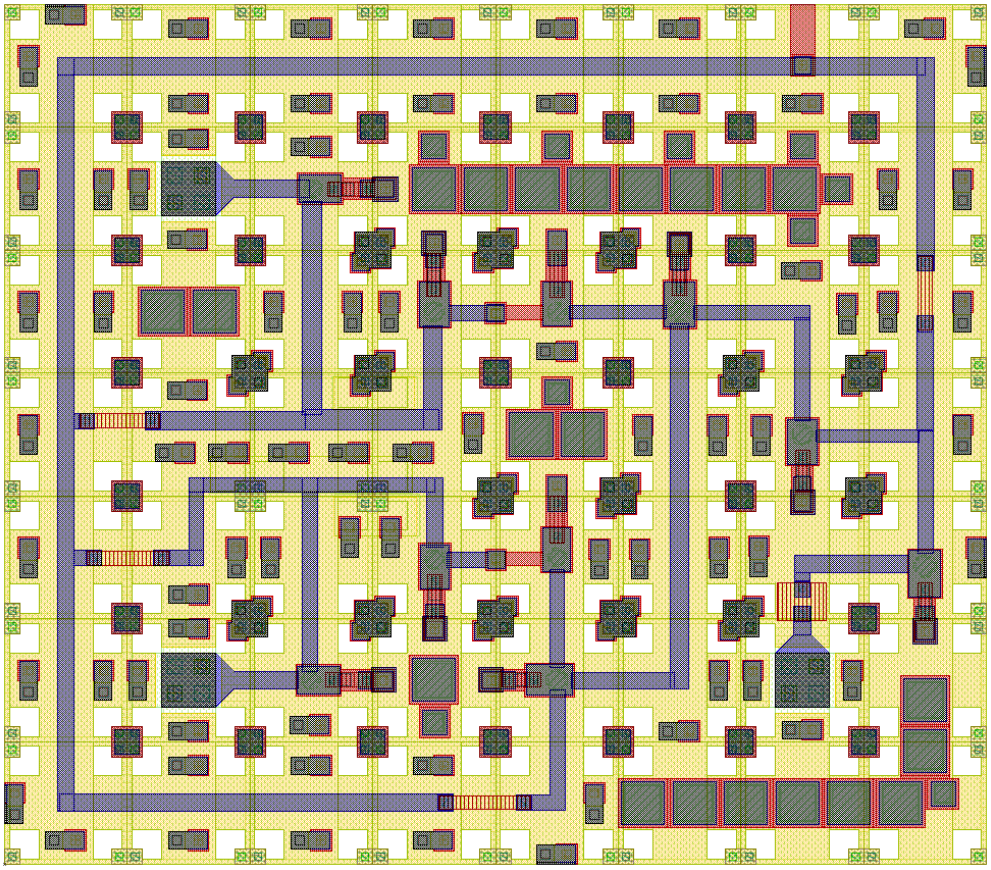

Figure 4.57: RSFQ DFFT Layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_DFFT_v1p5.gds -n LSmitll_DFFT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_DFFT_v1p5_idx.cir read. Totals: L = 25, k = 0, P = 17.
7  Total fundamental loops identified in netlist = 14
8  Using TetraHenry with analytical integration.
9  2405 structures read. Reduced 2405 objects to 2229 polygons and 7 terminals.
10 Top level structure is "LSMITLL_DFFT".
11 GDS file LSmitll_DFFT_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
12 Port clk not in netlist. Ignored.
13 Object in layer I5 moved to TERM layer. (Pj1)
14 Object in layer I5 moved to TERM layer. (Pj2)
15 Object in layer I5 moved to TERM layer. (Pj3)
16 Object in layer I5 moved to TERM layer. (Pj4)
17 Object in layer I5 moved to TERM layer. (Pj5)
18 Object in layer I5 moved to TERM layer. (Pj6)
19 Object in layer I5 moved to TERM layer. (Pj7)
20 Object in layer I5 moved to TERM layer. (Pj8)
21 Object in layer I5 moved to TERM layer. (Pj9)
22 Object in layer I5 moved to TERM layer. (Pj10)
23 Terminal blocks = 17; Labels = 18; Extracted Ports = 17
24
25 Port                  Positive terminal    Negative terminal
```

```
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
P3                    M6,   line along y;  M4,   same as "+" terminal.
PB1                   M6,   line along y;  M4,   same as "+" terminal.
PB2                   M6,   line along y;  M4,   same as "+" terminal.
PB3                   M6,   line along y;  M4,   same as "+" terminal.
PB4                   M6,   line along x;  M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M5,   polygon;       M6,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M6,   polygon;       M5,   same as "+" terminal.
J8                    M5,   polygon;       M6,   same as "+" terminal.
J9                    M6,   polygon;       M5,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 9.759; unknowns = 50; rank = 50.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name       Design      Extracted   Design      Extracted   (L only)    (L only)
L1         --          1.5637E-12  --          --          +1.5637E-12 --%
L2         3.28E-12    3.3024E-12  --          --          +2.2404E-14 +0.68305%
L3         3.28E-12    3.2234E-12  --          --          -5.6604E-14 -1.7257%
L4         4.06E-12    4.01455E-12 --          --          -4.5452E-14 -1.1195%
L5         7.51E-12    7.45324E-12 --          --          -5.6759E-14 -0.75578%
L6         --          1.62164E-12 --          --          +1.6216E-12 --%
L7         3.04E-12    3.06566E-12 --          --          +2.5658E-14 +0.844%
L8         3.04E-12    3.01289E-12 --          --          -2.7114E-14 -0.89191%
L9         4.21E-12    4.20385E-12 --          --          -6.1531E-15 -0.14615%
L10        4.02E-12    3.9935E-12  --          --          -2.6498E-14 -0.65916%
L11        2.15E-12    2.12269E-12 --          --          -2.7311E-14 -1.2703%
L12        2.15E-12    2.1382E-12  --          --          -1.1803E-14 -0.54896%
L13        --          1.85888E-12 --          --          +1.8589E-12 --%
LP1        --          5.12978E-13 --          --          +5.1298E-13 --%
LP2        --          5.1029E-13  --          --          +5.1029E-13 --%
LP4        --          5.20691E-13 --          --          +5.2069E-13 --%
LP5        --          5.28352E-13 --          --          +5.2835E-13 --%
LP6        --          4.99443E-13 --          --          +4.9944E-13 --%
LP7        --          5.15628E-13 --          --          +5.1563E-13 --%
LP9        --          5.1113E-13  --          --          +5.1113E-13 --%
LP10       --          5.12546E-13 --          --          +5.1255E-13 --%
LB1        --          3.81288E-12 --          --          +3.8129E-12 --%
LB2        --          2.46377E-12 --          --          +2.4638E-12 --%
LB3        --          1.72715E-12 --          --          +1.7271E-12 --%
LB4        --          1.95727E-12 --          --          +1.9573E-12 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         0.00016     0.00017055
J2         0.000189    0.00019733
J3         0.000172    0.00017942
J4         0.000232    0.00024083
J5         0.000212    0.00022067
J6         0.00016     0.00017055
J7         0.000198    0.00020657
J8         0.000171    0.00017942
J9         0.000212    0.00022067
J10        0.00025     0.00025893

Error bound on extracted values: 1.52366%

Deallocating memory.
Cycles found in 0.030 seconds.
SVD solution in 0.021 seconds.
Job finished in 293.335 seconds.
```

Listing 4.34: RSFQ DFFT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                              a clk q
.subckt LSMITLL_DFFT a clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap
    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
    ↪ )
.param Phi0=2.067833848E-15
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param LP=0.2p
.param IC=2.5
.param ICreceive=2.0
.param ICtrans=2.5
.param Lptl=2p
.param LB=2p
.param BiasCoef=0.7
.param RD=1.36
.param B1=ICreceive
.param B2=IC
.param B3=IC/1.4
.param B4=IC
.param B5=IC
.param B6=ICreceive
.param B7=IC
.param B8=IC/1.4
.param B9=IC
.param B10=ICtrans
.param IB1=BiasCoef*(B1*Ic0+B2*Ic0)
.param IB2=IC*Ic0
.param IB3=BiasCoef*(B6*Ic0+B7*Ic0)
.param IB4=BiasCoef*(B9*Ic0+B10*Ic0)
.param L1=Lptl
.param L2=(Phi0/(2*B1*Ic0))/2
.param L3=(Phi0/(2*B1*Ic0))/2
.param L4=Phi0/(2*B2*Ic0)
.param L5=Phi0/(B4*Ic0)
.param L6=Lptl
.param L7=(Phi0/(2*B6*Ic0))/2
.param L8=(Phi0/(2*B6*Ic0))/2
.param L9=Phi0/(2*B7*Ic0)
.param L10=Phi0/(2*B5*Ic0)
.param L11=(Phi0/(2*B9*Ic0))/2
.param L12=(Phi0/(2*B9*Ic0))/2
.param L13=Lptl
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param RB5=B0Rs/B5
.param RB6=B0Rs/B6
.param RB7=B0Rs/B7
.param RB8=B0Rs/B8
.param RB9=B0Rs/B9
.param RB10=B0Rs/B10
.param LRB1=(RB1/Rsheet)*Lsheet+LP
.param LRB2=(RB2/Rsheet)*Lsheet+LP
.param LRB3=(RB3/Rsheet)*Lsheet+LP
.param LRB4=(RB4/Rsheet)*Lsheet+LP
.param LRB5=(RB5/Rsheet)*Lsheet+LP
.param LRB6=(RB6/Rsheet)*Lsheet+LP
.param LRB7=(RB7/Rsheet)*Lsheet+LP
.param LRB8=(RB8/Rsheet)*Lsheet+LP
.param LRB9=(RB9/Rsheet)*Lsheet+LP
.param LRB10=(RB10/Rsheet)*Lsheet+LP
.param LP1=LP
.param LP2=LP
.param LP4=LP
.param LP5=LP
.param LP6=LP
.param LP7=LP
.param LP9=LP
.param LP10=LP
.param LB1=LB
.param LB2=LB
.param LB3=LB
.param LB4=LB
IB1 0 5 pwl(0 0 5p IB1)
IB2 0 11 pwl(0 0 5p IB2)
IB3 0 18 pwl(0 0 5p IB3)
IB4 0 25 pwl(0 0 5p IB4)
B1 2 3 jjmit area=B1
B2 6 7 jjmit area=B2
B3 8 9 jjmit area=B3
B4 9 10 jjmit area=B4
B5 12 13 jjmit area=B5
B6 15 16 jjmit area=B6
B7 19 20 jjmit area=B7
B8 21 12 jjmit area=B8
B9 22 23 jjmit area=B9
B10 26 27 jjmit area=B10
L1 a 2 L1
L2 2 4 L2
L3 4 6 L3
L4 6 8 L4
L5 9 12 L5
L6 clk 15 L6
L7 15 17 L7
L8 17 19 L8
L9 19 21 L9
L10 12 22 L10
L11 22 24 L11
L12 24 26 L12
L13 26 28 L13
LP1 3 0 LP1
LP2 7 0 LP2
LP4 10 0 LP4
LP5 13 0 LP5
LP6 16 0 LP6
LP7 20 0 LP7
LP9 23 0 LP9
LP10 27 0 LP10
LB1 4 5 LB1
LB2 9 11 LB2
LB3 17 18 LB3
LB4 24 25 LB4
RB1 2 102 RB1
RB2 6 106 RB2
RB3 8 108 RB3
RB4 9 109 RB4
RB5 12 112 RB5
RB6 15 115 RB6
RB7 19 119 RB7
RB8 21 121 RB8
RB9 22 122 RB9
```

```
RB10 26 126 RB10
LRB1 102 0 LRB1
LRB2 106 0 LRB2
LRB3 108 9 LRB3
LRB4 109 0 LRB4
LRB5 112 0 LRB5
LRB6 115 0 LRB6
LRB7 119 0 LRB7
LRB8 121 12 LRB8
LRB9 122 0 LRB9
LRB10 126 0 LRB10
RD 28 q RD
.ends
```

Listing 4.35: RSFQ DFFT JoSIM netlist.

Table 4.23: RSFQ DFFT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ DFFT using JoSIM is shown in Fig. 4.58. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **clk**,

(d) the phase over the input JJ of pin **clk**,

(e) the phase over the output JJ of pin **q**, and

(f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

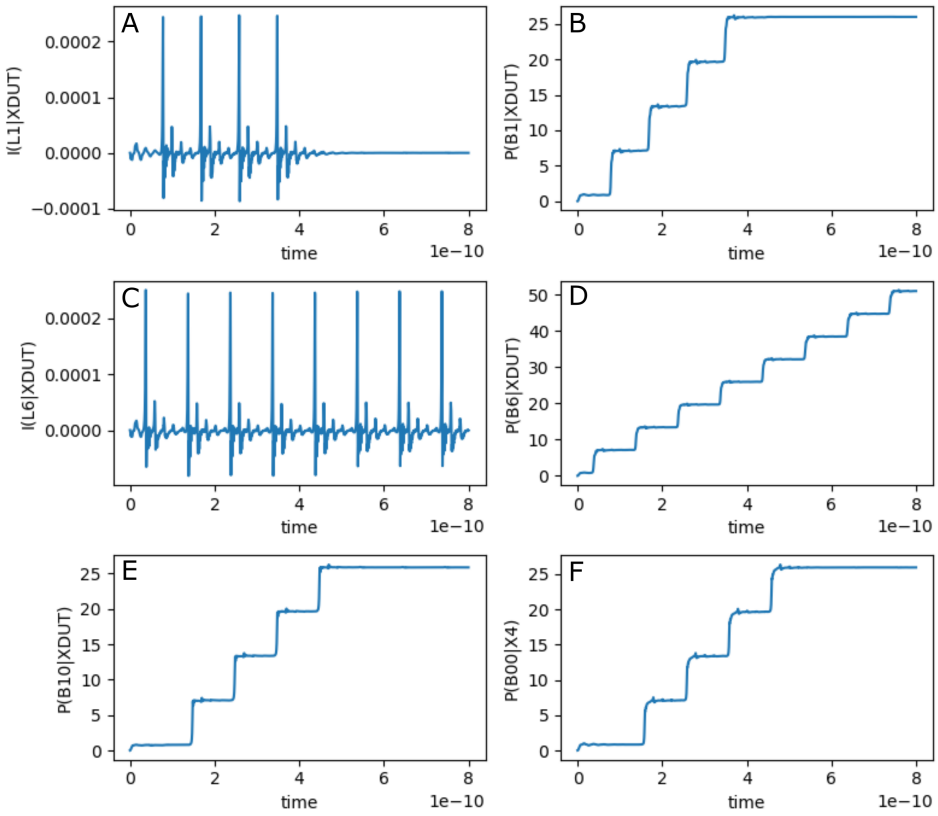

Figure 4.58: RSFQ DFFT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_DFFT_v1p5 (a, clk, q);

input
  a, clk;

output
  q;

reg
  q;

real
  delay_state1_clk_q = 10.3,
  ct_state0_clk_a = 1.0,
  ct_state1_a_clk = 1.0;

reg
   errorsignal_a,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                        end
                     1: begin
                           errorsignal_clk = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_clk <= #(ct_state1_a_clk) 0;  // Clear error signal
                               ↪  after critical timing expires
                        end
                  endcase
               end
```

```
65          end
66      end
67
68  always @(posedge clk or negedge clk) // execute at positive and negative edges of input
69      begin
70          if ($time>4) // arbitrary steady-state time)
71              begin
72                  if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
73                      begin
74                          outfile = $fopen("errors.txt", "a");
75                          $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                                ↪ ", $stime);
76                          $fclose(outfile);
77                          q <= 1'bX;  // Set all outputs to unknown
78                      end
79                  if (errorsignal_clk == 0)
80                      begin
81                          case (cell_state)
82                              0: begin
83                                     errorsignal_a = 1;  // Critical timing on this input; assign
                                           ↪ immediately
84                                     errorsignal_a <= #(ct_state0_clk_a) 0;  // Clear error signal
                                           ↪ after critical timing expires
85                                 end
86                              1: begin
87                                     q <= #(delay_state1_clk_q) !q;
88                                     cell_state = 0;  // Blocking statement -- immediately
89                                 end
90                          endcase
91                      end
92              end
93      end
94
95  endmodule
```

Listing 4.36: RSFQ DFFT verilog model.

The digital simulation results for the RSFQ DFFT is shown in Fig. 4.59 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.60.

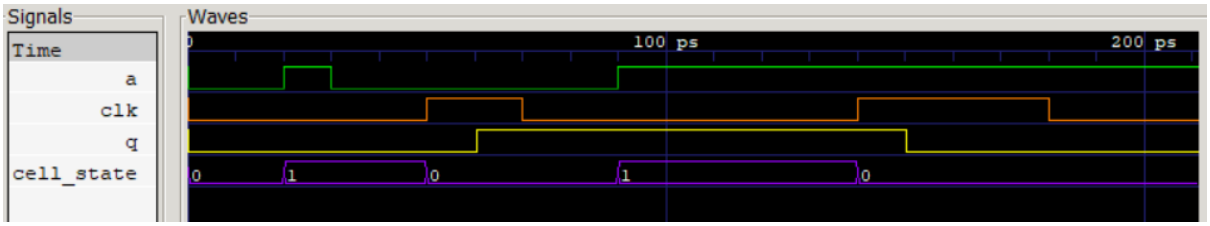

Figure 4.59: RSFQ DFFT digital simulation results.

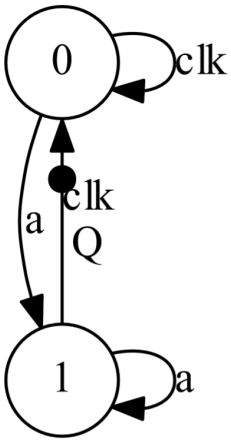

Figure 4.60: RSFQ DFFT Mealy finite state machine diagram.

Power Consumption

Table 4.24: RSFQ JTLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	320	4.67
2	320	9.33
5	320	23.3
10	320	46.7
20	320	93.3
50	320	233

4.3.2 NDROT

The NDROT, non-destructive readout, cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDROT will generate an output pulse after each clock signal until an input reset signal is received. The NDROT is designed with integrated PTL transmitters and receivers and is intended to connect directly to PTLs.

Schematic

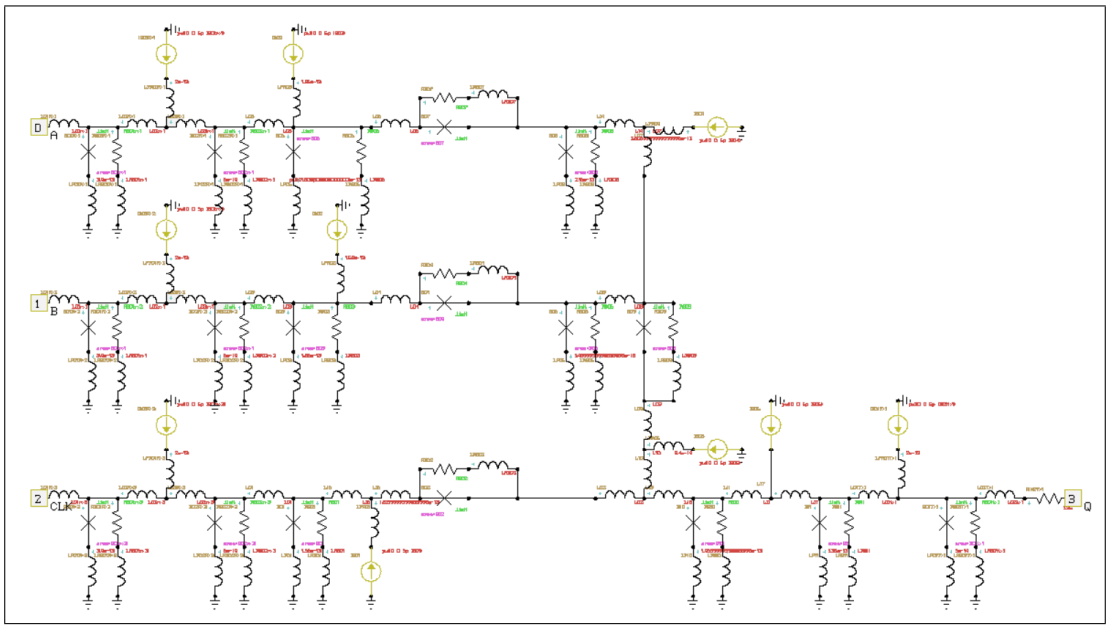

Figure 4.61: Schematic of RSFQ NDROT.

Layout

The physical layout for the RSFQ NDROT is shown in Fig. 4.62 and the resulting InductEx extraction is shown in Listing 4.37. The layout height is 70 μm and the width is 120 μm.

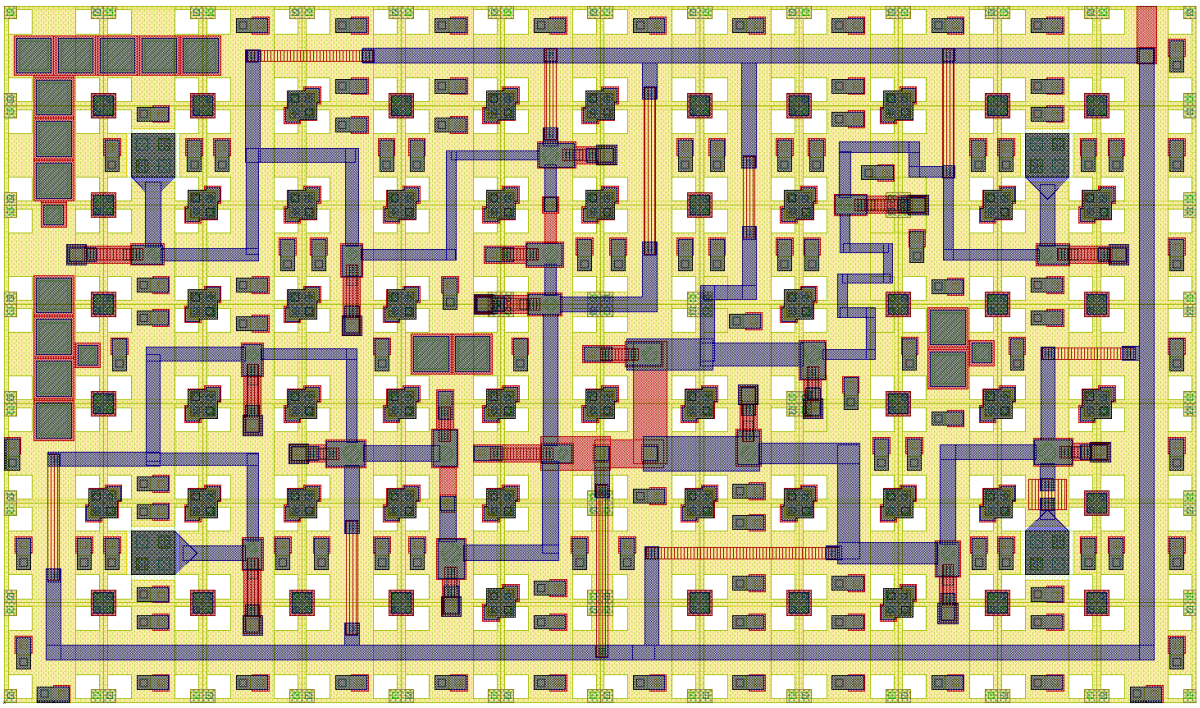

Figure 4.62: RSFQ NDROT Layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_NDROT_v1p5.GDS -n LSmitll_NDROT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_NDROT_v1p5_idx.cir read. Totals: L = 49, k = 0, P = 32.
7  Total fundamental loops identified in netlist = 27
8  Using TetraHenry with analytical integration.
9  3534 structures read. Reduced 3534 objects to 3260 polygons and 14 terminals.
10 Top level structure is "LSMITLL_NDROT_V1P5".
11 GDS file LSmitll_NDROT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 Port in_clk not in netlist. Ignored.
13 Object in layer I5 moved to TERM layer. (Pj1)
14 Object in layer I5 moved to TERM layer. (Pj2)
15 Object in layer I5 moved to TERM layer. (Pj3)
16 Object in layer I5 moved to TERM layer. (Pj4)
17 Object in layer I5 moved to TERM layer. (Pj5)
18 Object in layer I5 moved to TERM layer. (Pj6)
19 Object in layer I5 moved to TERM layer. (Pj7)
20 Object in layer I5 moved to TERM layer. (Pj8)
21 Object in layer I5 moved to TERM layer. (Pj9)
22 Object in layer I5 moved to TERM layer. (Pj10)
23 Object in layer I5 moved to TERM layer. (Pj11)
24 Object in layer I5 moved to TERM layer. (Pj12)
25 Object in layer I5 moved to TERM layer. (Pj13)
26 Object in layer I5 moved to TERM layer. (Pj14)
27 Object in layer I5 moved to TERM layer. (Pj15)
28 Object in layer I5 moved to TERM layer. (Pj16)
29 Object in layer I5 moved to TERM layer. (Pj17)
30 Object in layer I5 moved to TERM layer. (Pj18)
31 Terminal blocks = 32; Labels = 33; Extracted Ports = 32
32
```

Port	Positive terminal	Negative terminal
P1	M6, line along x;	M4, same as "+" terminal.
P2	M6, line along y;	M4, same as "+" terminal.
P3	M6, line along x;	M4, same as "+" terminal.
P4	M6, polygon;	M4, same as "+" terminal.
PB1	M6, polygon;	M4, same as "+" terminal.
PB2	M6, polygon;	M4, same as "+" terminal.
PB3	M6, polygon;	M4, same as "+" terminal.
PB4	M6, polygon;	M4, same as "+" terminal.
PB5	M6, polygon;	M4, same as "+" terminal.
PB6	M6, polygon;	M4, same as "+" terminal.
PB7	M6, polygon;	M4, same as "+" terminal.
PB8	M6, polygon;	M4, same as "+" terminal.
PB9	M6, polygon;	M4, same as "+" terminal.
PB10	M6, polygon;	M4, same as "+" terminal.
J1	M6, polygon;	M5, same as "+" terminal.
J2	M6, polygon;	M5, same as "+" terminal.
J3	M6, polygon;	M5, same as "+" terminal.
J4	M5, polygon;	M6, same as "+" terminal.
J5	M6, polygon;	M5, same as "+" terminal.
J6	M6, polygon;	M5, same as "+" terminal.
J7	M6, polygon;	M5, same as "+" terminal.
J8	M6, polygon;	M5, same as "+" terminal.
J9	M6, polygon;	M5, same as "+" terminal.
J10	M6, polygon;	M5, same as "+" terminal.
J11	M6, polygon;	M5, same as "+" terminal.
J12	M6, polygon;	M5, same as "+" terminal.
J13	M6, polygon;	M5, same as "+" terminal.
J14	M6, polygon;	M5, same as "+" terminal.
J15	M6, polygon;	M5, same as "+" terminal.
J16	M6, polygon;	M5, same as "+" terminal.
J17	M6, polygon;	M5, same as "+" terminal.
J18	M6, polygon;	M5, same as "+" terminal.

SVD info: Condition nr. = 24.05; unknowns = 98; rank = 98.

Impedance	Inductance [H]		Resistance [Ohm]		AbsDiff	PercDiff
Name	Design	Extracted	Design	Extracted	(L only)	(L only)
L1	--	1.48915E-12	--	--	+1.4892E-12	--%
L2	4.0481E-12	4.0116E-12	--	--	-3.6504E-14	-0.90175%
L3	3.6036E-12	3.58661E-12	--	--	-1.6989E-14	-0.47145%
L4	7.2183E-12	7.19858E-12	--	--	-1.9717E-14	-0.27316%
L5	3.0677E-12	3.06389E-12	--	--	-3.8096E-15	-0.12418%
L7	2.5596E-12	2.54719E-12	--	--	-1.2411E-14	-0.48487%
L8	--	1.55031E-12	--	--	+1.5503E-12	--%
L9	4.0481E-12	4.07033E-12	--	--	+2.2227E-14	+0.54906%
L10	3.6036E-12	3.58197E-12	--	--	-2.1631E-14	-0.60026%
L11	4.3879E-12	4.36209E-12	--	--	-2.5815E-14	-0.58831%
L12	3.217E-12	3.21634E-12	--	--	-6.5613E-16	-0.020396%
L13	3.2439E-12	3.25118E-12	--	--	+7.2792E-15	+0.2244%
L14	--	1.54044E-12	--	--	+1.5404E-12	--%
L15	4.3135E-12	4.33251E-12	--	--	+1.901E-14	+0.44072%
L16	3.926E-12	3.92903E-12	--	--	+3.0296E-15	+0.077167%
L17	7.5833E-12	7.50305E-12	--	--	-8.0252E-14	-1.0583%
L18	1.2875E-12	1.30037E-12	--	--	+1.2867E-14	+0.99934%
L19	1.0678E-12	1.50349E-12	--	--	+4.3569E-13	+40.802%
L21	3.7382E-13	5.7611E-13	--	--	+2.0229E-13	+54.114%
L22	5.2995E-13	5.39797E-13	--	--	+9.8473E-15	+1.8582%
L23	9.5137E-13	1.06471E-12	--	--	+1.1334E-13	+11.914%
L24	2.5089E-12	2.50214E-12	--	--	-6.7551E-15	-0.26925%
L25	1.2791E-12	1.2826E-12	--	--	+3.5029E-15	+0.27386%
L26	3.5427E-12	3.55781E-12	--	--	+1.5113E-14	+0.42658%
L27	--	6.57709E-13	--	--	+6.5771E-13	--%
LP1	--	5.46871E-13	--	--	+5.4687E-13	--%
LP2	--	5.85175E-13	--	--	+5.8517E-13	--%
LP3	--	4.31117E-13	--	--	+4.3112E-13	--%
LP5	--	5.99747E-13	--	--	+5.9975E-13	--%
LP6	--	5.10392E-13	--	--	+5.1039E-13	--%
LP7	--	5.64586E-13	--	--	+5.6459E-13	--%
LP8	--	4.84967E-13	--	--	+4.8497E-13	--%

```
LP10       --          4.77636E-13 --          --          +4.7764E-13 --%
LP12       --          5.45247E-13 --          --          +5.4525E-13 --%
LP13       --          5.44328E-13 --          --          +5.4433E-13 --%
LP14       --          4.9116E-13  --          --          +4.9116E-13 --%
LP16       --          4.99509E-13 --          --          +4.9951E-13 --%
LP17       --          5.24198E-13 --          --          +5.242E-13  --%
LP18       --          4.16652E-13 --          --          +4.1665E-13 --%
LB1        --          2.10012E-12 --          --          +2.1001E-12 --%
LB2        --          4.02957E-13 --          --          +4.0296E-13 --%
LB3        --          2.91892E-12 --          --          +2.9189E-12 --%
LB4        --          2.22202E-12 --          --          +2.222E-12  --%
LB5        --          1.45598E-12 --          --          +1.456E-12  --%
LB6        --          2.78673E-13 --          --          +2.7867E-13 --%
LB7        --          2.99385E-12 --          --          +2.9938E-12 --%
LB8        --          9.92666E-13 --          --          +9.9267E-13 --%
LB9        --          4.98289E-13 --          --          +4.9829E-13 --%
LB10       --          2.12412E-12 --          --          +2.1241E-12 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         0.000086    0.000093558
J2         0.0001      0.00010794
J3         0.000191    0.0001998
J4         0.000178    0.00018513
J5         0.000116    0.00012397
J6         0.000086    0.000093558
J7         0.0001      0.00010794
J8         0.000235    0.00024373
J9         0.000196    0.00020513
J10        0.000284    0.00029299
J11        0.000078    0.000085495
J12        0.000099    0.00010693
J13        0.000094    0.00010169
J14        0.000218    0.00022671
J15        0.000165    0.00017332
J16        0.000163    0.00017134
J17        0.000151    0.00015939
J18        0.000236    0.00024495

Error bound on extracted values: 6.07859%

Deallocating memory.
Cycles found in 0.029 seconds.
SVD solution in 0.071 seconds.
Job finished in 675.467 seconds.
```

Listing 4.37: RSFQ NDROT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                          a b clk q
.subckt LSmitll_NDROT a b clk q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B01=2.1788
.param B01rx1=0.8597
.param B01rx3=0.9892
.param B01tx1=2.3613
.param B02=1.6498
.param B02rx1=1.0002
.param B02rx3=0.9426
.param B03=2.3464
.param B04=1.9597
.param B05=2.8368
.param B06=1.9079
.param B07=1.7749
.param B08=1.1619
.param B09=0.7782
.param B10=1.6313
.param B11=1.5079
.param IB01=0.000223851
.param IB01rx1=0.000134142
.param IB01rx3=0.000131798
.param IB01tx1=0.000195509
.param IB02=0.000152193
.param IB03=0.000198086
.param IB04=9.85166e-05
.param IB05=9.47282e-05
.param IB06=6.36747e-05
.param L01=7.5833e-012
.param L01rx1=1.9122e-012
.param L01rx3=1.7869e-12
.param L01tx1=3.5427e-12
.param L02=1.3381e-12
.param L02rx1=4.0481e-12
.param L02rx3=4.3135e-12
.param L02tx1=3.5270e-12
.param L03=4.3879e-12
.param L03rx1=3.6036e-12
.param L03rx3=3.9260e-12
.param L04=3.2170e-12
.param L05=7.2183e-12
.param L06=3.0677e-12
.param L07=2.5596e-12
.param L08=3.2439e-12
.param L09=3.7382e-13
.param L10=5.2995e-13
.param L11=2.5089e-12
.param L13=9.5137e-13
.param L14=4.7528e-14
.param L15=1.2875e-12
.param L16=1.0678e-12
.param L17=1.2791e-12
.param LRB01=(RB01/Rsheet)*Lsheet
.param LRB01rx1=(RB01rx1/Rsheet)*Lsheet
.param LRB01rx3=(RB01rx3/Rsheet)*Lsheet
.param LRB01tx1=(RB01tx1/Rsheet)*Lsheet
.param LRB02=(RB02/Rsheet)*Lsheet
.param LRB02rx1=(RB02rx1/Rsheet)*Lsheet
.param LRB02rx2=(RB02rx2/Rsheet)*Lsheet
.param LRB02rx3=(RB02rx3/Rsheet)*Lsheet
.param LRB03=(RB03/Rsheet)*Lsheet
.param LRB04=(RB04/Rsheet)*Lsheet
.param LRB05=(RB05/Rsheet)*Lsheet
.param LRB06=(RB06/Rsheet)*Lsheet
.param LRB07=(RB07/Rsheet)*Lsheet
.param LRB08=(RB08/Rsheet)*Lsheet
.param LRB09=(RB09/Rsheet)*Lsheet
.param LRB10=(RB10/Rsheet)*Lsheet
.param LRB11=(RB11/Rsheet)*Lsheet
.param RB01=B0Rs/B01
.param RB01rx1=B0Rs/B01rx1
.param RB01rx2=B0Rs/B01rx1
.param RB01rx3=B0Rs/B01rx3
.param RB01tx1=B0Rs/B01tx1
.param RB02=B0Rs/B02
.param RB02rx1=B0Rs/B02rx1
.param RB02rx2=B0Rs/B02rx1
.param RB02rx3=B0Rs/B02rx3
.param RB03=B0Rs/B03
.param RB04=B0Rs/B04
.param RB05=B0Rs/B05
.param RB06=B0Rs/B06
.param RB07=B0Rs/B07
.param RB08=B0Rs/B08
.param RB09=B0Rs/B09
.param RB10=B0Rs/B10
.param RB11=B0Rs/B11
B01 22 66 jjmit area=B01
B01rx1 7 32 jjmit area=B01rx1
B01rx2 13 44 jjmit area=B01rx1
B01rx3 20 62 jjmit area=B01rx3
B01tx1 25 73 jjmit area=B01tx1
B02 18 19 jjmit area=B02
B02rx1 8 34 jjmit area=B02rx1
B02rx2 14 46 jjmit area=B02rx1
B02rx3 21 64 jjmit area=B02rx3
B03 15 48 jjmit area=B03
B04 11 12 jjmit area=B04
B05 12 50 jjmit area=B05
B06 9 36 jjmit area=B06
B07 5 6 jjmit area=B07
B08 6 38 jjmit area=B08
B09 10 16 jjmit area=B09
B10 23 69 jjmit area=B10
B11 24 71 jjmit area=B11
IB01 0 68 pwl(0 0 5p IB01)
IB01rx1 0 26 pwl(0 0 5p IB01rx1)
IB01rx2 0 40 pwl(0 0 5p IB01rx1)
IB01rx3 0 53 pwl(0 0 5p IB01rx3)
IB01tx1 0 55 pwl(0 0 5p IB01tx1)
IB02 0 41 pwl(0 0 5p IB02)
IB03 0 27 pwl(0 0 5p IB03)
IB04 0 30 pwl(0 0 5p IB04)
IB05 0 56 pwl(0 0 5p IB05)
IB06 0 17 pwl(0 0 5p IB06)
L01 21 22 L01
L01rx1 a 7 L01rx1
L01rx2 b 13 L01rx1
```

```
L01rx3 clk 20 L01rx3
L01tx1 24 25 L01tx1
L02 19 58 L02
L02rx1 7 28 L02rx1
L02rx2 13 42 L02rx1
L02rx3 20 57 L02rx3
L02tx1 25 61 L02tx1
L03 14 15 L03
L03rx1 28 8 L03rx1
L03rx2 42 14 L03rx1
L03rx3 57 21 L03rx3
L04 15 11 L04
L05 8 9 L05
L06 9 5 L06
L07 31 10 L07
L08 12 10 L08
L09 16 54 L09
L10 54 58 L10
L11 23 17 L11
L13 58 23 L13
L14 6 31 L14
L15 22 60 L15
L16 60 18 L16
L17 17 24 L17
LP01 66 0 1.56e-13
LP01rx1 32 0 3.4e-13
LP01rx2 44 0 3.4e-13
LP01rx3 62 0 3.4e-13
LP01tx1 73 0 5e-14
LP02rx1 34 0 6e-14
LP02rx2 46 0 6e-14
LP02rx3 64 0 6e-14
LP03 48 0 1.35e-13
LP05 50 0 1.46e-13
LP06 36 0 1.33e-13
LP08 38 0 2.16e-13
LP10 69 0 1.46e-13
LP11 71 0 1.35e-13
LPR01 60 68 1.82e-13
LPR01rx1 26 28 2e-13
LPR01rx2 40 42 2e-13
LPR01rx3 53 57 2e-13
LPR01tx1 55 25 2e-13
LPR02 41 15 1.53e-13
LPR03 27 9 1.85e-13
LPR04 30 31 2.506e-12
LPR05 54 56 3.4e-14
LRB01 67 0 LRB01
LRB01rx1 33 0 LRB01rx1
LRB01rx2 45 0 LRB01rx1
LRB01rx3 63 0 LRB01rx3
LRB01tx1 74 0 LRB01tx1
LRB02 59 19 LRB02
LRB02rx1 35 0 LRB02rx1
LRB02rx2 47 0 LRB02rx2
LRB02rx3 65 0 LRB02rx3
LRB03 49 0 LRB03
LRB04 43 12 LRB04
LRB05 51 0 LRB05
LRB06 37 0 LRB06
LRB07 29 6 LRB07
LRB08 39 0 LRB08
LRB09 52 16 LRB09
LRB10 70 0 LRB10
LRB11 72 0 LRB11
RB01 22 67 RB01
RB01rx1 7 33 RB01rx1
RB01rx2 13 45 RB01rx2
RB01rx3 20 63 RB01rx3
RB01tx1 25 74 RB01tx1
RB02 18 59 RB02
RB02rx1 8 35 RB02rx1
RB02rx2 14 47 RB02rx2
RB02rx3 21 65 RB02rx3
RB03 15 49 RB03
RB04 11 43 RB04
RB05 12 51 RB05
RB06 9 37 RB06
RB07 5 29 RB07
RB08 6 39 RB08
RB09 10 52 RB09
RB10 23 70 RB10
RB11 24 72 RB11
RINStx1 61 q 1.36
.ends
```

Listing 4.38: RSFQ NDROT JoSIM netlist.

Table 4.25: RSFQ NDROT pin list.

Pin	Description
a	Data input (set signal)
b	Data input (reset signal)
clk	Clock input
q	Data output

The simulation results for the RSFQ NDROT using JoSIM is shown in Fig. 4.63. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a** (set signal),

(b) the phase over the input JJ of pin **a**,

(c) the current through the input inductor connected to pin **b** (reset signal),

(d) the phase over the input JJ of pin **b**,

(e) the current through the input inductor connected to pin **clk**,

(f) the phase over the input JJ of pin **clk**,

(g) the phase over the output JJ of pin **q**, and

(h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

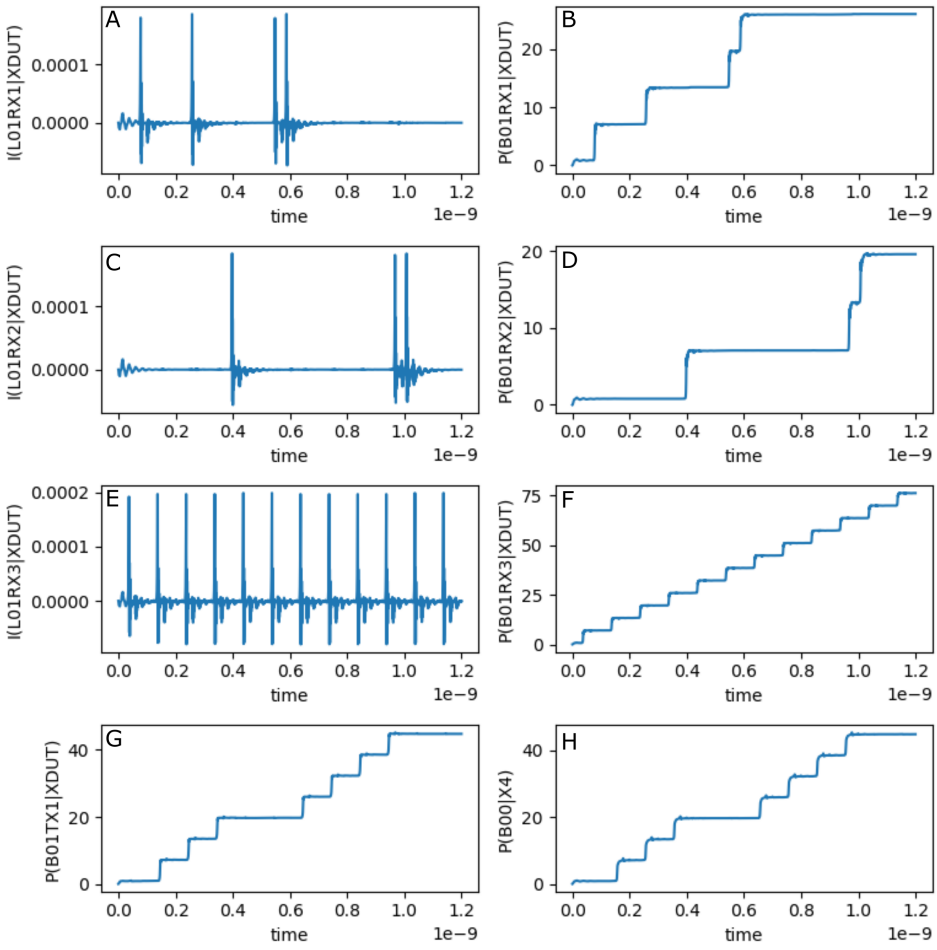

Figure 4.63: RSFQ NDROT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_NDROT_v1p5 (a, b, clk, q);

input
  a, b, clk;

output
  q;

reg
  q;

real
  delay_state1_clk_q = 9.0,
  ct_state0_b_a = 4.5,
  ct_state1_a_b = 0.8,
  ct_state1_clk_clk = 9.5;

reg
   errorsignal_a,
   errorsignal_b,
   errorsignal_clk;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      errorsignal_b = 0;
      errorsignal_clk = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation␣of␣critical␣timing␣in␣module␣%m;␣%0d␣ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           cell_state = 1;  // Blocking statement -- immediately
                        end
                     1: begin
                           errorsignal_b = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_b <= #(ct_state1_a_b) 0;  // Clear error signal
                               ↪ after critical timing expires
```

```
65                         end
66                     endcase
67                 end
68             end
69     end
70
71 always @(posedge b or negedge b) // execute at positive and negative edges of input
72     begin
73         if ($time>4) // arbitrary steady-state time)
74             begin
75                 if (errorsignal_b == 1'b1)  // A critical timing is active for this input
76                     begin
77                         outfile = $fopen("errors.txt", "a");
78                         $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                               ↪ ", $stime);
79                         $fclose(outfile);
80                         q <= 1'bX;  // Set all outputs to unknown
81                     end
82                 if (errorsignal_b == 0)
83                     begin
84                         case (cell_state)
85                             0: begin
86                                    errorsignal_a = 1;  // Critical timing on this input; assign
                                           ↪ immediately
87                                    errorsignal_a <= #(ct_state0_b_a) 0;  // Clear error signal
                                           ↪ after critical timing expires
88                                end
89                             1: begin
90                                    cell_state = 0;  // Blocking statement -- immediately
91                                end
92                         endcase
93                     end
94             end
95     end
96
97 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
98     begin
99         if ($time>4) // arbitrary steady-state time)
100            begin
101                if (errorsignal_clk == 1'b1)  // A critical timing is active for this input
102                    begin
103                        outfile = $fopen("errors.txt", "a");
104                        $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                               ↪ ", $stime);
105                        $fclose(outfile);
106                        q <= 1'bX;  // Set all outputs to unknown
107                    end
108                if (errorsignal_clk == 0)
109                    begin
110                        case (cell_state)
111                            0: begin
112                               end
113                            1: begin
114                                   q <= #(delay_state1_clk_q) !q;
115                                   errorsignal_clk = 1;  // Critical timing on this input; assign
                                           ↪ immediately
116                                   errorsignal_clk <= #(ct_state1_clk_clk) 0;  // Clear error
                                           ↪ signal after critical timing expires
117                               end
118                        endcase
119                    end
120            end
121    end
122
123 endmodule
```

Listing 4.39: RSFQ NDROT verilog model.

The digital simulation results for the RSFQ NDROT is shown in Fig. 4.64 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 4.65.

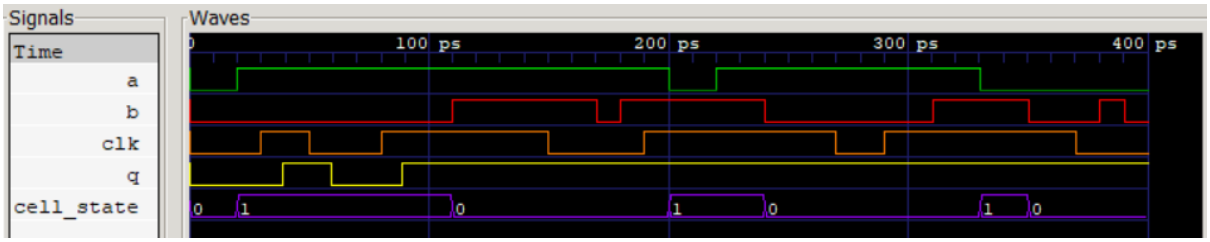

Figure 4.64: RSFQ NDROT digital simulation results.

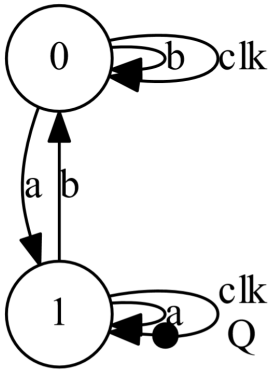

Figure 4.65: RSFQ NDROT Mealy finite state machine diagram.

Power Consumption

Table 4.26: RSFQ NDROT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	371	5.74
2	371	11.5
5	371	28.7
10	371	57.4
20	371	115
50	371	287

4.3.3 BUFF

The RSFQ BUFF cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the CLKSPLT, CLKSPLTT and BUFFT cell. The BUFF does not have integrated PTL transmitters and receivers and connecting the cell directly to a PTL is not recommended.

Schematic

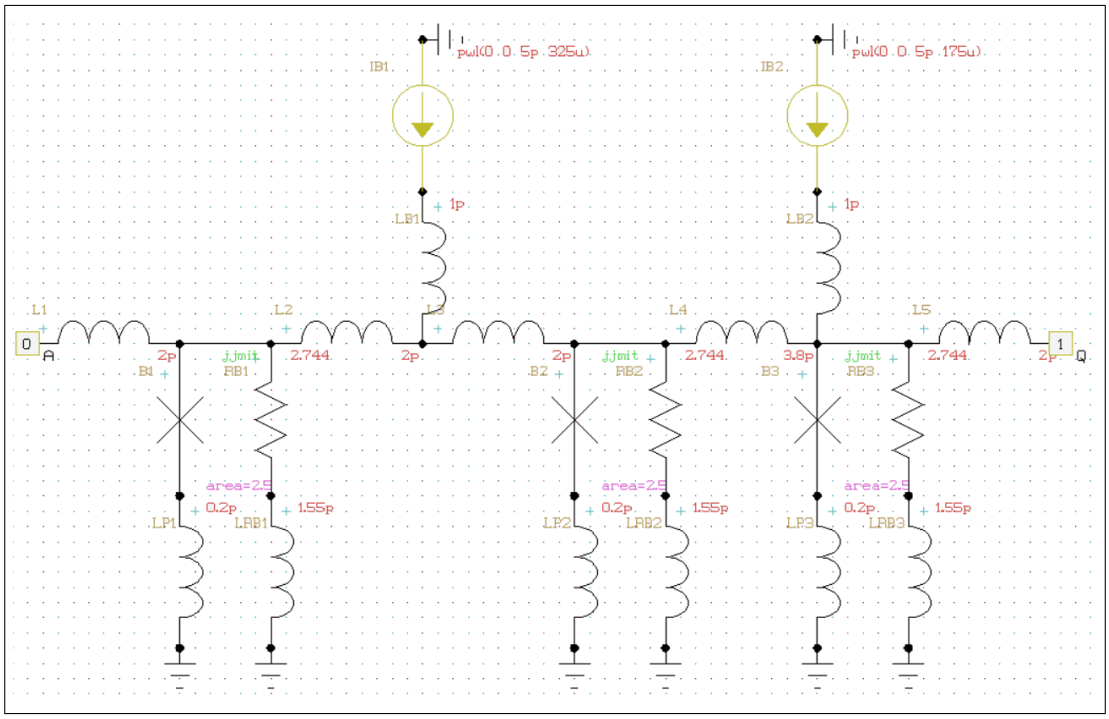

Figure 4.66: Schematic of RSFQ BUFF.

Layout

The physical layout for the RSFQ BUFF is shown in Fig. 4.67 and the resulting InductEx extraction is shown in Listing 4.40. The layout height is 70 μm and the width is 40 μm. If required, an additional and smaller layout can be made to minimize chip space for clock balancing.

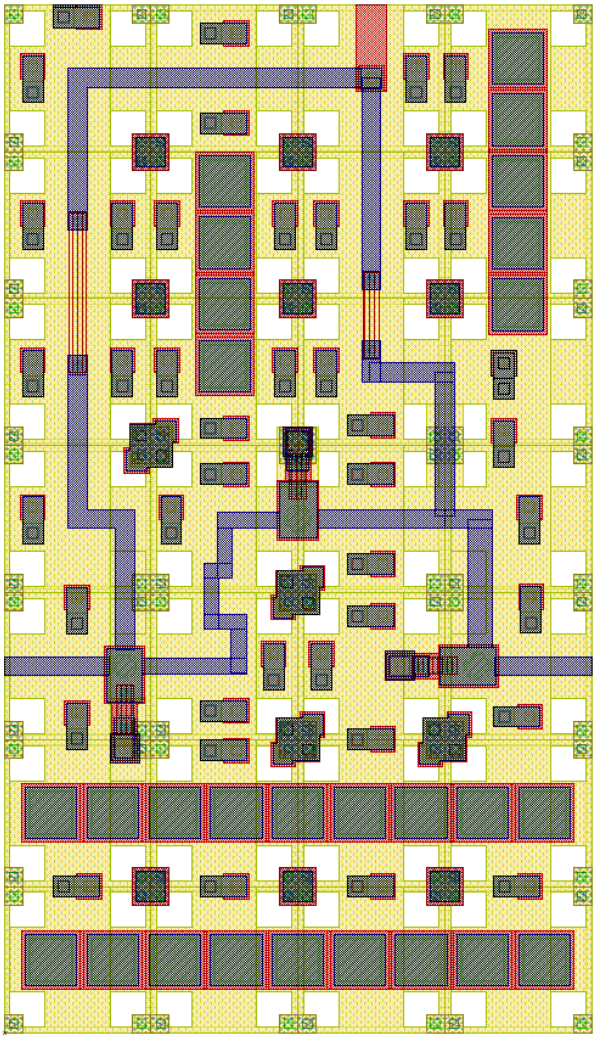

Figure 4.67: RSFQ BUFF Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_BUFF_v1p5.GDS -n LSmitll_BUFF_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_BUFF_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
Total fundamental loops identified in netlist = 6
Using TetraHenry with analytical integration.
1192 structures read. Reduced 1192 objects to 1102 polygons and 4 terminals.
Top level structure is "LSMITLL_BUFF".
GDS file LSmitll_BUFF_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 7; Labels = 7; Extracted Ports = 7

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 6.023; unknowns = 20; rank = 20.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        2E-12       2.03159E-12 --          --          +3.1593E-14 +1.5796%
L2        5.2E-12     5.24662E-12 --          --          +4.6624E-14 +0.89662%
L3        2.07E-12    2.03231E-12 --          --          -3.7686E-14 -1.8206%
L4        2.07E-12    2.03606E-12 --          --          -3.3938E-14 -1.6395%
L5        2E-12       1.93888E-12 --          --          -6.1115E-14 -3.0558%
LB1       --          4.83917E-12 --          --          +4.8392E-12 --%
LB2       --          3.33223E-12 --          --          +3.3322E-12 --%
LP1       --          4.67809E-13 --          --          +4.6781E-13 --%
LP2       --          4.70078E-13 --          --          +4.7008E-13 --%
LP3       --          4.70474E-13 --          --          +4.7047E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.0002      0.00020853
J2        0.00025     0.00025893
J3        0.00025     0.00025893

Error bound on extracted values: 1.46224%

Deallocating memory.
Cycles found in 0.027 seconds.
SVD solution in 0.016 seconds.
Job finished in 111.865 seconds.
```

Listing 4.40: RSFQ BUFF InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 11 June 2020
* Last modification by: L. Schindler

*$Ports                                  a  q
.subckt LSmitll_buff a  q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
B1  3 7  jjmit area=2.5
B2  4 9  jjmit area=2.5
B3 2 11 jjmit area=2.5
IB1 0 5 pwl(0 0 5p 325u)
IB2 0 2 pwl(0 0 5p 175u)
L1 a 3 2p
L2 3 6 2p
L3 6 4 2p
L4 4 2 3.8p
L5 2 q 2p
LB1 5 6 0.2p
LP1 7 0 0.2p
LP2 9 0 0.2p
LP3 11 0 0.2p
LRB1 3 8 1.55E-12
LRB2 4 10 1.55E-12
LRB3 12 0 1.55E-12
RB1 8 0 2.744
RB2 10 0 2.744
RB3 2 12 2.744
.ends
```

Listing 4.41: RSFQ BUFF JoSIM netlist.

Table 4.27: RSFQ BUFF pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFF using JoSIM is shown in Fig. 4.68. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected to pin **q**.

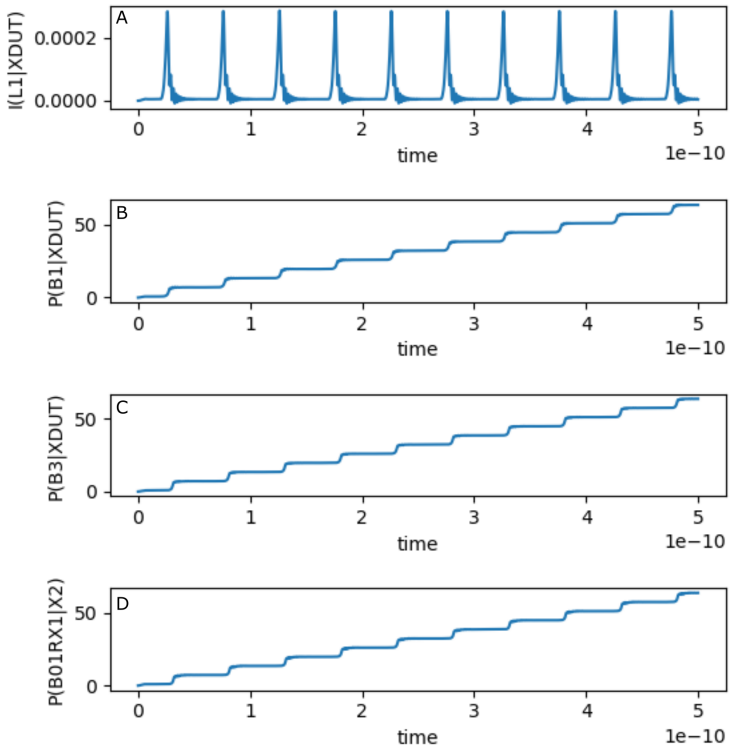

Figure 4.68: RSFQ BUFF analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_buff_v1p5 (a, q);

input
  a;

output
  q;

reg
  q;

real
  delay_state0_a_q = 5.5,
  ct_state0_a_a = 3.5;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end

endmodule
```

Listing 4.42: RSFQ BUFF verilog model.

The digital simulation results for the RSFQ BUFF is shown in Fig. 4.69 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.70.

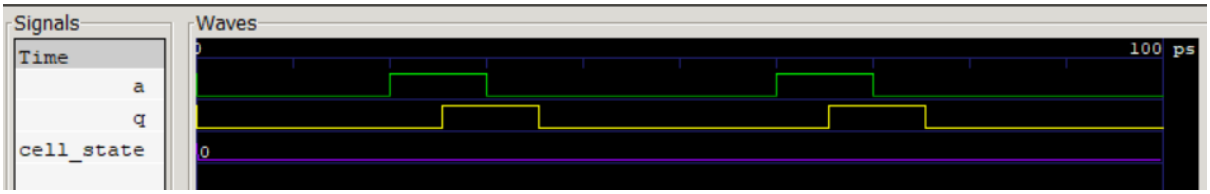

Figure 4.69: RSFQ BUFF digital simulation results.

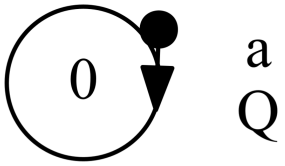

Figure 4.70: RSFQ BUFF Mealy finite state machine diagram.

Power Consumption

Table 4.28: RSFQ BUFF power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	130	1.55
2	130	3.10
5	130	7.75
10	130	15.5
20	130	31.0
50	130	77.5

4.3.4 BUFFT

The RSFQ BUFFT cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the CLKSPLT, CLKSPLTT and BUFF cell. The BUFFT is designed with integrated PTL drivers and receivers and is intended to be connected directly to PTLs.

Schematic

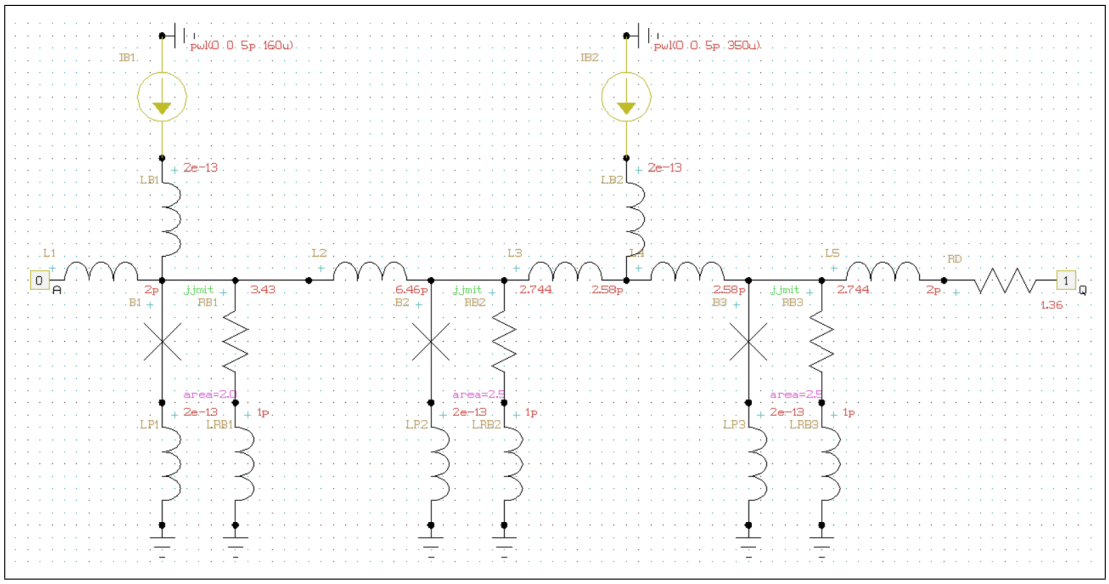

Figure 4.71: Schematic of RSFQ BUFFT.

Layout

The physical layout for the RSFQ BUFFT is shown in Fig. 4.72 and the resulting InductEx extraction is shown in Listing 4.43. The layout height is 70 μm and the width is 40 μm.

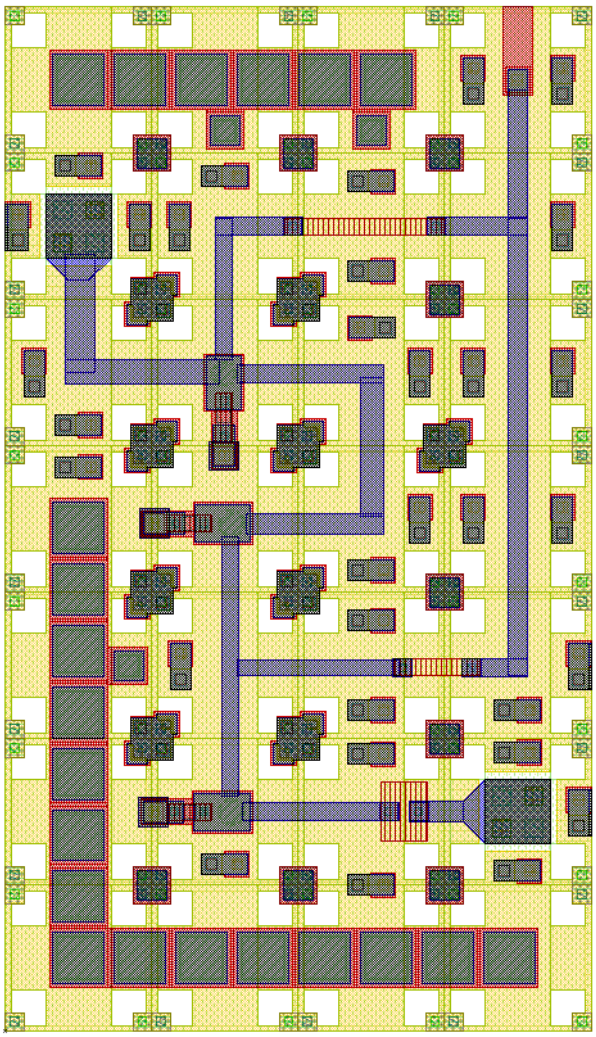

Figure 4.72: RSFQ BUFFT Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_BUFFT_v1p5.GDS -n LSmitll_BUFFT_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_BUFFT_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
Total fundamental loops identified in netlist = 6
Using TetraHenry with analytical integration.
1188 structures read. Reduced 1188 objects to 1118 polygons and 4 terminals.
Top level structure is "LSMITLL_BUFFT_V1P5".
GDS file LSmitll_BUFFT_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 7; Labels = 7; Extracted Ports = 7

Port                  Positive terminal    Negative terminal
P1                    M6,   line along x;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 4.249; unknowns = 20; rank = 20.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          2.88269E-12 --          --          +2.8827E-12 --%
L2        5.2E-12     5.21421E-12 --          --          +1.421E-14  +0.27327%
L3        2.07E-12    2.06667E-12 --          --          -3.3273E-15 -0.16074%
L4        2.07E-12    2.06239E-12 --          --          -7.6057E-15 -0.36743%
L5        --          2.40125E-12 --          --          +2.4013E-12 --%
LB1       --          3.20092E-12 --          --          +3.2009E-12 --%
LB2       --          2.8577E-12  --          --          +2.8577E-12 --%
LP1       --          5.24521E-13 --          --          +5.2452E-13 --%
LP2       --          5.12732E-13 --          --          +5.1273E-13 --%
LP3       --          5.0586E-13  --          --          +5.0586E-13 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.0002      0.00020853
J2        0.00025     0.00025893
J3        0.00025     0.00025893

Error bound on extracted values: 0.779537%

Deallocating memory.
Cycles found in 0.029 seconds.
SVD solution in 0.014 seconds.
Job finished in 112.339 seconds.
```

Listing 4.43: RSFQ BUFFT InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

*$Ports                                  a  q
.subckt LSmitll_bufft  a  q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
B1 2 3 jjmit area=2.0
B2 6 7 jjmit area=2.5
B3 11 12 jjmit area=2.5
IB1 0 5 pwl(0 0 5p 160u)
IB2 0 10 pwl(0 0 5p 350u)
L1 a 2 2p
L2 2 6 5.2p
L3 6 9 2.07p
L4 9 11 2.07p
L5 11 14 2p
RD 14 q 1.36
LP1 3 0 0.2p
LP2 7 0 0.2p
LP3 12 0 0.2p
RB1 2 4 3.43
RB2 6 8 2.744
RB3 11 13 2.744
LRB1 4 0 1.94p
LRB2 8 0 1.55p
LRB3 13 0 1.55p
LB1 2 5 1p
LB2 9 10 1p
.ends
```

Listing 4.44: RSFQ BUFFT JoSIM netlist.

Table 4.29: RSFQ BUFFT pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFFT using JoSIM is shown in Fig. 4.73. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

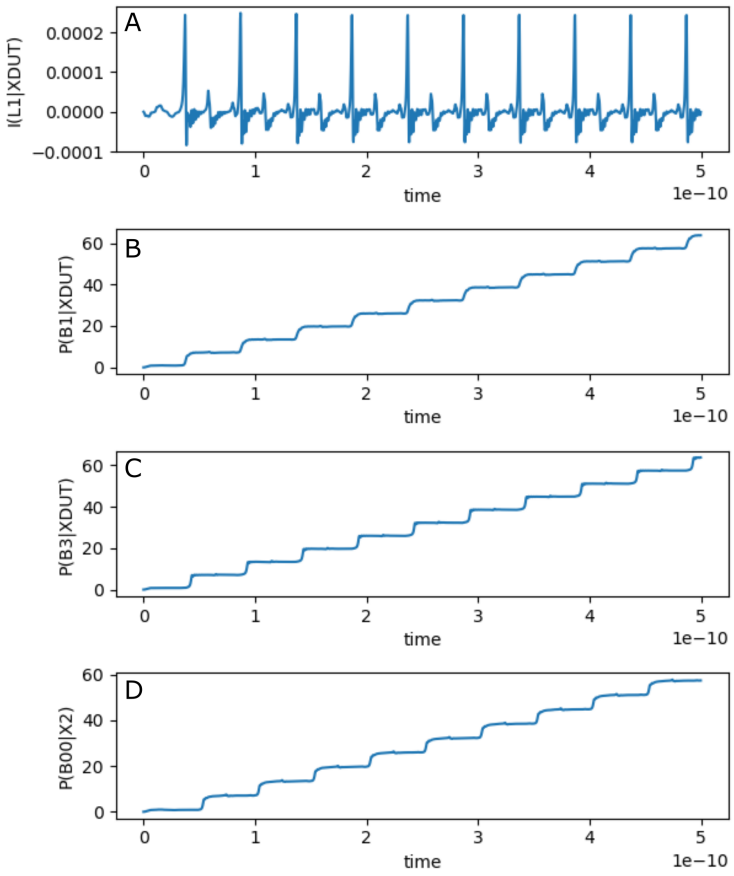

Figure 4.73: RSFQ BUFFT analog simulation results.

Digital model

```
// -------------------------------------------------------------------------
// Automatically extracted verilog file, created with TimEx v2.05
// Timing description and structural design for IARPA-BAA-14-03 via
// U.S. Air Force Research Laboratory contract FA8750-15-C-0203 and
// IARPA-BAA-16-03 via U.S. Army Research Office grant W911NF-17-1-0120.
// For questions about TimEx, contact CJ Fourie, coenrad@sun.ac.za
// (c) 2016-2018 Stellenbosch University
// -------------------------------------------------------------------------
`timescale 1ps/100fs
module LSmitll_bufft_v1p5 (a, q);

input
  a;

output
  q;

reg
  q;

real
  delay_state0_a_q = 5.5,
  ct_state0_a_a = 7.0;

reg
   errorsignal_a;

integer
   outfile,
   cell_state; // internal state of the cell

initial
   begin
      errorsignal_a = 0;
      cell_state = 0; // Startup state
      q = 0; // All outputs start at 0
   end

always @(posedge a or negedge a) // execute at positive and negative edges of input
   begin
      if ($time>4) // arbitrary steady-state time)
         begin
            if (errorsignal_a == 1'b1)  // A critical timing is active for this input
               begin
                  outfile = $fopen("errors.txt", "a");
                  $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
                      ↪ ", $stime);
                  $fclose(outfile);
                  q <= 1'bX;  // Set all outputs to unknown
               end
            if (errorsignal_a == 0)
               begin
                  case (cell_state)
                     0: begin
                           q <= #(delay_state0_a_q) !q;
                           errorsignal_a = 1;  // Critical timing on this input; assign
                               ↪ immediately
                           errorsignal_a <= #(ct_state0_a_a) 0;  // Clear error signal
                               ↪ after critical timing expires
                        end
                  endcase
               end
         end
   end

endmodule
```

Listing 4.45: RSFQ BUFFT verilog model.

The digital simulation results for the RSFQ BUFFT is shown in Fig. 4.74 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 4.75.

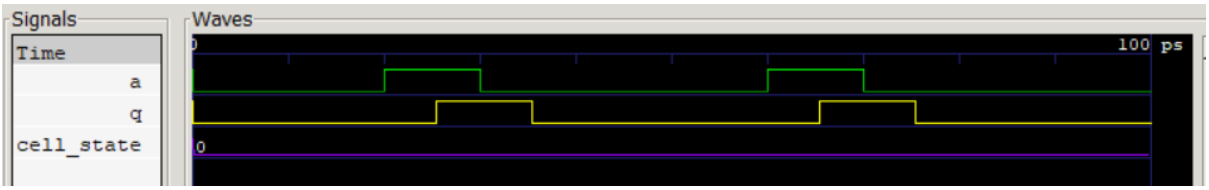

Figure 4.74: RSFQ BUFFT digital simulation results.

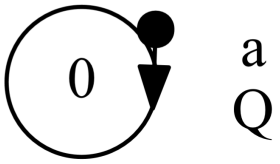

Figure 4.75: RSFQ BUFFT Mealy finite state machine diagram.

Power Consumption

Table 4.30: RSFQ BUFFT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	133	1.45
2	133	2.89
5	133	7.24
10	133	14.5
20	133	28.9
50	133	72.4

4.4 Interface cells

4.4.1 DCSFQ

The RSFQ DCSFQ is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ does not have an integrated PTL transmitter and is not intended to connect directly to a PTL output.

Schematic

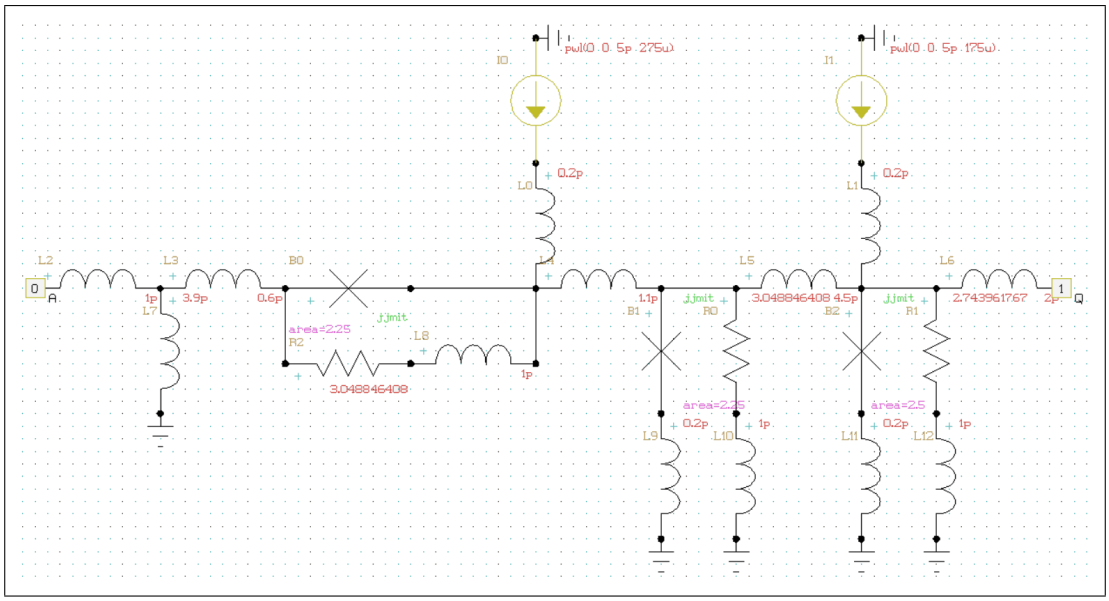

Figure 4.76: Schematic of RSFQ DCSFQ.

Layout

The physical layout for the RSFQ DCSFQ is shown in Fig. 4.77 and the resulting InductEx extraction is shown in Listing 4.46. The layout height is 70 μm and the width is 30 μm.

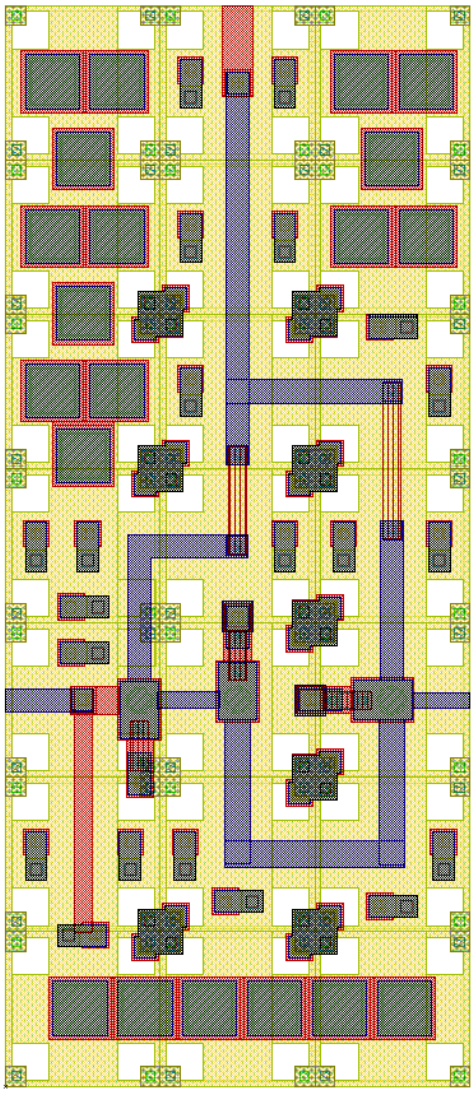

Figure 4.77: RSFQ DCSFQ Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
Licensed to:
  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_DCSFQ_v1p5.GDS -n LSmitll_DCSFQ_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_DCSFQ_v1p5_idx.cir read. Totals: L = 10, k = 0, P = 7.
Total fundamental loops identified in netlist = 6
Using TetraHenry with analytical integration.
838 structures read. Reduced 838 objects to 805 polygons and 4 terminals.
Top level structure is "LSMITLL_DCSFQ_V1P5".
GDS file LSmitll_DCSFQ_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Terminal blocks = 7; Labels = 7; Extracted Ports = 7

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   line along y;  M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M5,   polygon;       M6,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 7.119; unknowns = 20; rank = 20.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        1E-12       1.47068E-12 --          --          +4.7068E-13 +47.068%
L2        3.9E-12     3.91959E-12 --          --          +1.959E-14  +0.50232%
L3        6E-13       5.95746E-13 --          --          -4.2537E-15 -0.70894%
L4        1.1E-12     1.12164E-12 --          --          +2.1639E-14 +1.9672%
L5        4.5E-12     4.70289E-12 --          --          +2.0289E-13 +4.5087%
L6        2E-12       1.52806E-12 --          --          -4.7194E-13 -23.597%
LPB2      --          4.95543E-13 --          --          +4.9554E-13 --%
LPB3      --          4.20985E-13 --          --          +4.2099E-13 --%
LB1       --          2.98424E-12 --          --          +2.9842E-12 --%
LB2       --          2.22935E-12 --          --          +2.2294E-12 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000225    0.00023374
J2        0.000225    0.00023374
J3        0.00025     0.00025893

Error bound on extracted values: 3.60869%

Deallocating memory.
Cycles found in 0.026 seconds.
SVD solution in 0.005 seconds.
Job finished in 70.993 seconds.
```

Listing 4.46: RSFQ DCSFQ InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

* Ports                          a q
.subckt LSmitll_DCSFQ a q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
B0 3 4 jjmit area=2.25
B1 5 10 jjmit area=2.25
B2 6 12 jjmit area=2.5
I0 0 7 pwl(0 0 5p 275u)
I1 0 8 pwl(0 0 5p 175u)
L0 7 4 0.2p
L1 8 6 0.2p
L2 a 9 1p
L3 9 3 0.6p
L4 4 5 1.1p
L5 5 6 4.5p
L6 6 q 2p
L7 9 0 3.9p
L8 14 4 1p
L9 10 0 0.2p
L10 11 0 1p
L11 12 0 0.2p
L12 13 0 1p
R0 5 11 3.048846408
R1 6 13 2.743961767
R2 3 14 3.048846408
.ends
```

Listing 4.47: RSFQ DCSFQ JoSIM netlist.

Table 4.31: RSFQ DCSFQ pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ using JoSIM is shown in Fig. 4.78. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the current through the output inductor connected to pin **q**,

(c) the phase over the output JJ of pin **q**, and

(d) the phase over the input JJ of the load circuit connected to pin **q**.

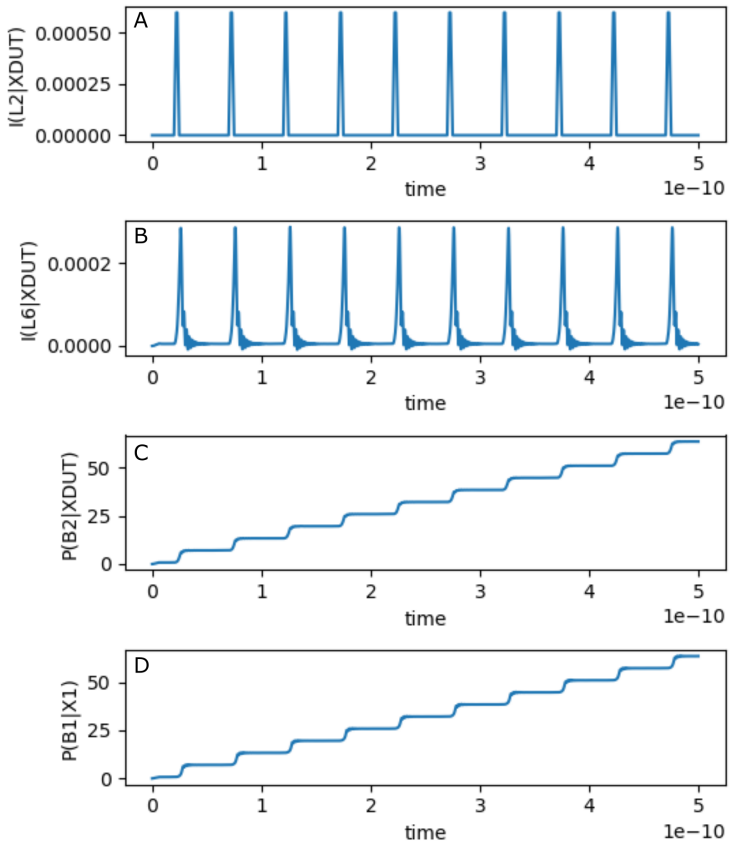

Figure 4.78: RSFQ DCSFQ analog simulation results.

4.4.2 DCSFQ-PTLTX

The RSFQ DCSFQ-PTLTX is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ-PTLTX has an integrated PTL transmitter and is intended to connect directly to a PTL output.

Schematic

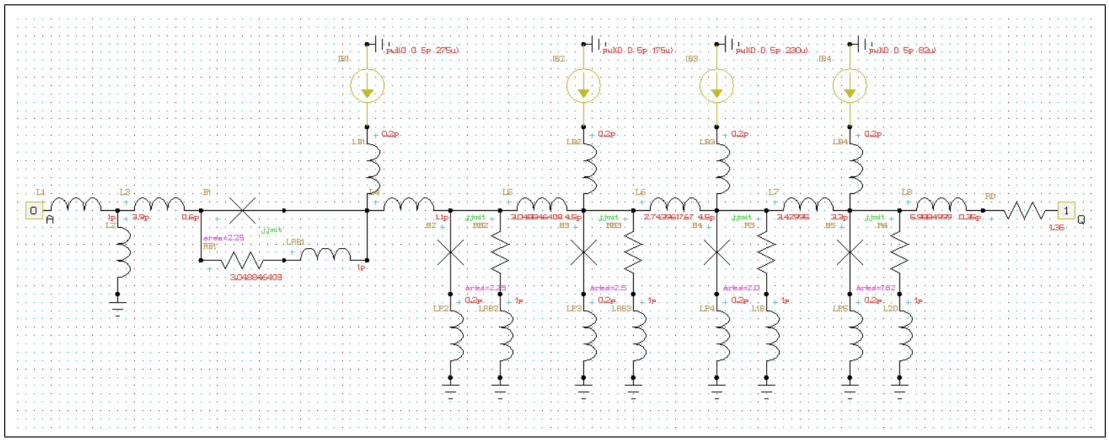

Figure 4.79: Schematic of RSFQ DCSFQ-PTLTX.

Layout

The physical layout for the RSFQ DCSFQ-PTLTX is shown in Fig. 4.80 and the resulting InductEx extraction is shown in Listing 4.48. The layout height is 50 μm and the width is 60 μm.

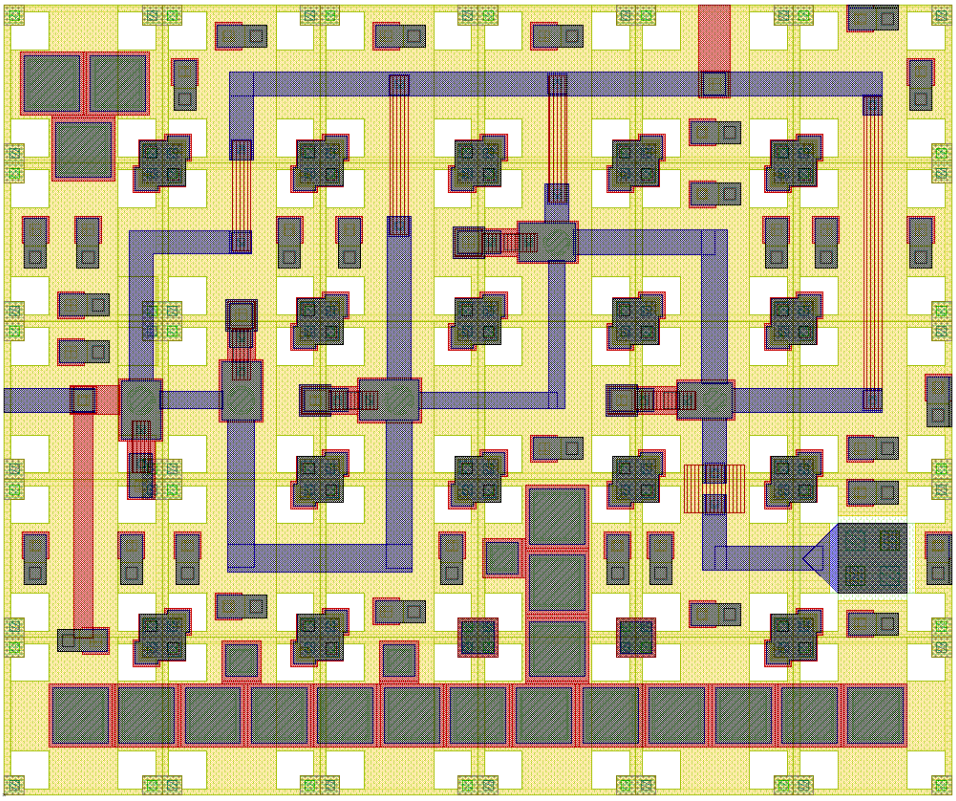

Figure 4.80: RSFQ DCSFQ-PTLTX Layout

```
InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
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  SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
LSmitll_DCSFQ_PTLTX_v1p5.GDS -n LSmitll_DCSFQ_PTLTX_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf
    ↪ -th
Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
Spice netlist LSmitll_DCSFQ_PTLTX_v1p5_idx.cir read. Totals: L = 16, k = 0, P = 11.
Total fundamental loops identified in netlist = 10
Using TetraHenry with analytical integration.
1289 structures read. Reduced 1289 objects to 1193 polygons and 6 terminals.
Top level structure is "LSMITLL_DCSFQ-PTLTX_V1P5".
GDS file LSmitll_DCSFQ_PTLTX_v1p5.GDS read: db units in 1E-9 m, 0.001 units per user unit.
Object in layer I5 moved to TERM layer. (Pj1)
Object in layer I5 moved to TERM layer. (Pj2)
Object in layer I5 moved to TERM layer. (Pj3)
Object in layer I5 moved to TERM layer. (Pj4)
Object in layer I5 moved to TERM layer. (Pj5)
Terminal blocks = 11; Labels = 11; Extracted Ports = 11

Port                  Positive terminal    Negative terminal
P1                    M6,   line along y;  M4,   same as "+" terminal.
P2                    M6,   polygon;       M4,   same as "+" terminal.
PB1                   M6,   polygon;       M4,   same as "+" terminal.
PB2                   M6,   polygon;       M4,   same as "+" terminal.
PB3                   M6,   polygon;       M4,   same as "+" terminal.
PB4                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M5,   polygon;       M6,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 13.28; unknowns = 32; rank = 32.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name      Design      Extracted   Design      Extracted   (L only)    (L only)
L1        --          1.47032E-12 --          --          +1.4703E-12 --%
L2        3.9E-12     3.90992E-12 --          --          +9.916E-15  +0.25426%
L3        6E-13       5.98562E-13 --          --          -1.4379E-15 -0.23966%
L4        1.1E-12     1.1097E-12  --          --          +9.7048E-15 +0.88225%
L5        4.5E-12     4.51344E-12 --          --          +1.3442E-14 +0.29871%
L6        4.5E-12     4.48805E-12 --          --          -1.1947E-14 -0.26548%
L7        3.3E-12     3.31827E-12 --          --          +1.8274E-14 +0.55374%
L8        --          9.57773E-13 --          --          +9.5777E-13 --%
LP2       --          5.05901E-13 --          --          +5.059E-13  --%
LP3       --          5.07474E-13 --          --          +5.0747E-13 --%
LP4       --          4.58516E-13 --          --          +4.5852E-13 --%
LP5       --          4.75969E-13 --          --          +4.7597E-13 --%
LB1       --          2.98109E-12 --          --          +2.9811E-12 --%
LB2       --          2.11931E-12 --          --          +2.1193E-12 --%
LB3       --          5.96227E-13 --          --          +5.9623E-13 --%
LB4       --          2.03793E-12 --          --          +2.0379E-12 --%

Ports     Design    Extracted AbsDiff   PercDiff
J1        0.000225    0.00023374
J2        0.000225    0.00023374
J3        0.00025     0.00025893
J4        0.0002      0.00020853
J5        0.000162    0.00017055

Error bound on extracted values: 3.89487%

Deallocating memory.
Cycles found in 0.030 seconds.
SVD solution in 0.008 seconds.
Job finished in 109.458 seconds.
```

Listing 4.48: RSFQ DCSFQ-PTLTX InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

* Copyright (c) 2018-2020 Lieze Schindler, Stellenbosch University

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* LIBRARY.

*For questions about the library, contact Lieze Schindler, 17528283@sun.ac.za

* Ports                          a q
.subckt LSmitll_DCSFQ_PTLTX a q
.model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param LB=0.2p
.param LP=0.2p
.param B1=2.25
.param B2=2.25
.param B3=2.5
.param B4=2
.param B5=1.62
.param IB1=275u
.param IB2=175u
.param IB3=230u
.param IB4=82u
.param L1=1p
.param L2=3.9p
.param L3=0.6p
.param L4=1.1p
.param L5=4.5p
.param L6=4.5p
.param L7=3.3p
.param L8=0.35p
.param RD=1.36
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param RB5=B0Rs/B5
.param LRB1=(RB1/Rsheet)*Lsheet
.param LRB2=(RB2/Rsheet)*Lsheet
.param LRB3=(RB3/Rsheet)*Lsheet
.param LRB4=(RB4/Rsheet)*Lsheet
.param LRB5=(RB5/Rsheet)*Lsheet

```

```
B1 2 3 jjmit area=B1
B2 6 7 jjmit area=B2
B3 9 10 jjmit area=B3
B4 13 14 jjmit area=B4
B5 17 18 jjmit area=B5
IB1 0 5 pwl(0 0 5p IB1)
IB2 0 12 pwl(0 0 5p IB2)
IB3 0 16 pwl(0 0 5p IB3)
IB4 0 20 pwl(0 0 5p IB4)
LB1 5 3 LB
LB2 12 9 LB
LB3 16 13 LB
LB4 20 17 LB
L1 a 1 L1
L2 1 0 L2
L3 1 2 L3
L4 3 6 L4
L5 6 9 L5
L6 9 13 L6
L7 13 17 L7
L8 17 21 L8
LP2 7 0 LP
LP3 10 0 LP
LP4 14 0 LP
LP5 18 0 LP
LRB1 2 4 LRB1
LRB2 8 0 LRB2
LRB3 11 0 LRB3
LRB4 15 0 LRB4
LRB5 19 0 LRB5
RB1 4 3 RB1
RB2 6 8 RB2
RB3 9 11 RB3
RB4 13 15 RB4
RB5 17 19 RB5
RD 21 q RD
.ends
```

Listing 4.49: RSFQ DCSFQ-PTLTX JoSIM netlist.

Table 4.32: RSFQ DCSFQ-PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ-PTLTX using JoSIM is shown in Fig. 4.81. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the output JJ of pin **q**, and

(c) the phase over the input JJ of the load circuit connected through a PTL to pin **q**.

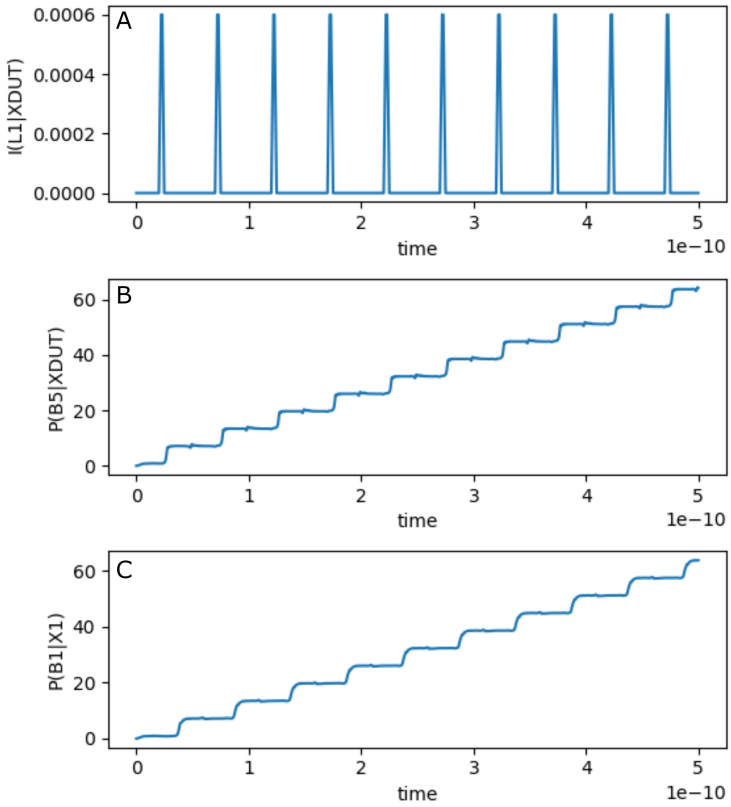

Figure 4.81: RSFQ DCSFQ-PTLTX analog simulation results.

4.4.3 PTLRX-SFQDC

The RSFQ PTLRX-SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The PTLRX-SFQDC has an integrated PTL receiver and is intended to be connected directly to a PTL input.

Schematic

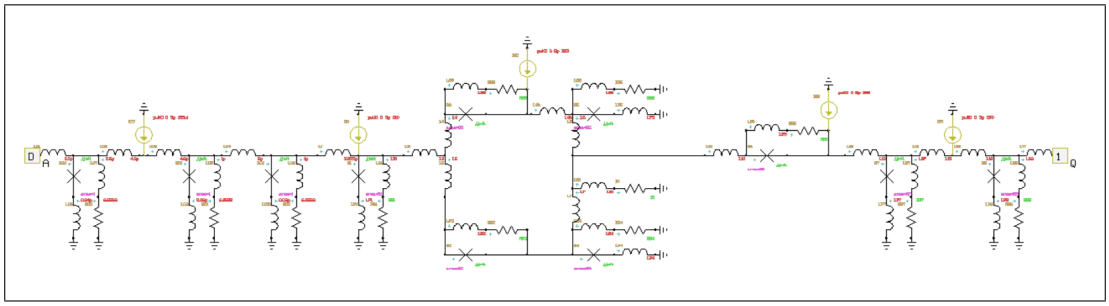

Figure 4.82: Schematic of RSFQ PTLRX-SFQDC.

Layout

The physical layout for the RSFQ PTLRX-SFQDC is shown in Fig. 4.83 and the resulting InductEx extraction is shown in Listing 4.50. The layout height is 70 μm and the width is 100 μm.

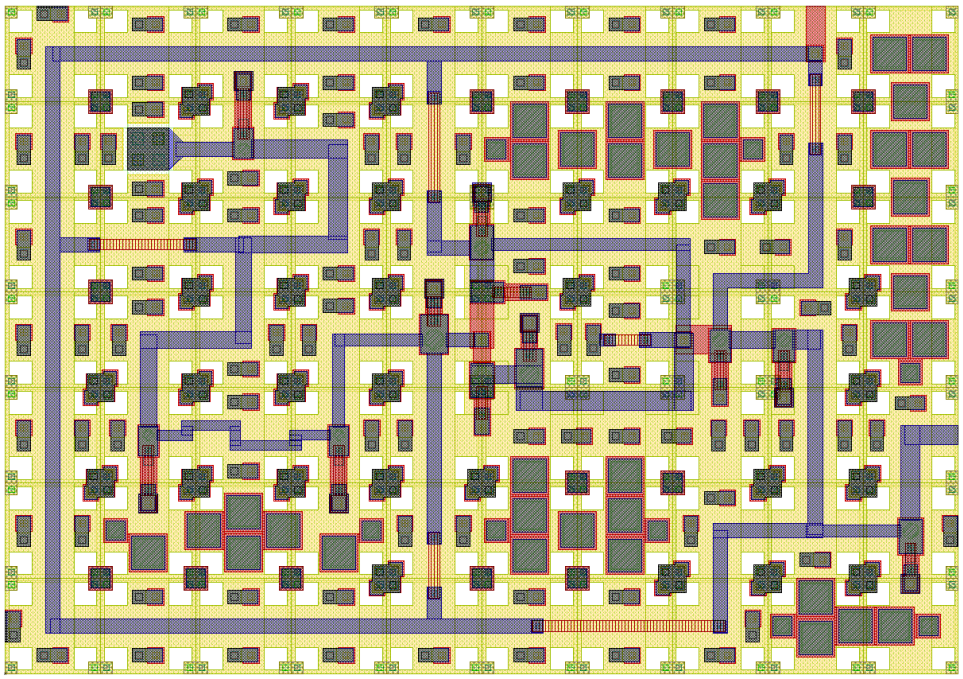

Figure 4.83: RSFQ PTLRX-SFQDC Layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_PTLRX_SFQDC.GDS -n LSmitll_PTLRX_SFQDC_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_PTLRX_SFQDC_v1p5_idx.cir read. Totals: L = 29, k = 0, P = 19.
7  Total fundamental loops identified in netlist = 16
8  Using TetraHenry with analytical integration.
9  3001 structures read. Reduced 3001 objects to 2770 polygons and 8 terminals.
10 Top level structure is "LSMITLL_PTLRX_SFQDC".
11 GDS file LSmitll_PTLRX_SFQDC.GDS read: db units in 1E-9 m, 0.001 units per user unit.
12 Object in layer I5 moved to TERM layer. (Pj1)
13 Object in layer I5 moved to TERM layer. (Pj2)
14 Object in layer I5 moved to TERM layer. (Pj3)
15 Object in layer I5 moved to TERM layer. (Pj4)
16 Object in layer I5 moved to TERM layer. (Pj5)
17 Object in layer I5 moved to TERM layer. (Pj6)
18 Object in layer I5 moved to TERM layer. (Pj7)
19 Object in layer I5 moved to TERM layer. (Pj8)
20 Object in layer I5 moved to TERM layer. (Pj9)
21 Object in layer I5 moved to TERM layer. (Pj10)
22 Object in layer I5 moved to TERM layer. (Pj11)
23 Terminal blocks = 19; Labels = 19; Extracted Ports = 19
24
25 Port                  Positive terminal    Negative terminal
26 P1                    M6,   line along y;  M4,   same as "+" terminal.
27 P2                    M6,   line along y;  M4,   same as "+" terminal.
28 PR1                   M6,   polygon;       M4,   same as "+" terminal.
29 PB1                   M6,   polygon;       M4,   same as "+" terminal.
30 PB2                   M6,   polygon;       M4,   same as "+" terminal.
31 PB3                   M6,   polygon;       M4,   same as "+" terminal.
```

```
PB4                   M6,   polygon;       M4,   same as "+" terminal.
PB5                   M6,   polygon;       M4,   same as "+" terminal.
J1                    M6,   polygon;       M5,   same as "+" terminal.
J2                    M6,   polygon;       M5,   same as "+" terminal.
J3                    M6,   polygon;       M5,   same as "+" terminal.
J4                    M6,   polygon;       M5,   same as "+" terminal.
J5                    M5,   polygon;       M6,   same as "+" terminal.
J6                    M6,   polygon;       M5,   same as "+" terminal.
J7                    M5,   polygon;       M6,   same as "+" terminal.
J8                    M6,   polygon;       M5,   same as "+" terminal.
J9                    M5,   polygon;       M6,   same as "+" terminal.
J10                   M6,   polygon;       M5,   same as "+" terminal.
J11                   M6,   polygon;       M5,   same as "+" terminal.

SVD info: Condition nr. = 10.31; unknowns = 58; rank = 58.

Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
Name       Design      Extracted   Design      Extracted   (L only)    (L only)
L1         --          1.49897E-12 --          --          +1.499E-12  --%
L2         4.3E-12     4.28097E-12 --          --          -1.9028E-14 -0.4425%
L3         4.6E-12     4.58405E-12 --          --          -1.5946E-14 -0.34666%
L4         5E-12       5.02465E-12 --          --          +2.4655E-14 +0.49309%
L5         3.822E-12   3.79261E-12 --          --          -2.9385E-14 -0.76885%
L6         8.27E-13    8.30297E-13 --          --          +3.2969E-15 +0.39865%
L7         1.12884E-12 1.16984E-12 --          --          +4.1002E-14 +3.6322%
L9         5.94E-12    5.94915E-12 --          --          +9.1498E-15 +0.15404%
L10        1.111E-12   1.10679E-12 --          --          -4.2145E-15 -0.37934%
L11        3.216E-12   3.23679E-12 --          --          +2.0788E-14 +0.64639%
L12        9.1E-13     8.90652E-13 --          --          -1.9348E-14 -2.1262%
L14        2.15E-13    5.767E-13   --          --          +3.617E-13  +168.23%
L15        9.54E-13    9.62382E-13 --          --          +8.3823E-15 +0.87865%
L16        3.699E-12   3.7028E-12  --          --          +3.7977E-15 +0.10267%
L17        2.01E-12    2.0198E-12  --          --          +9.8041E-15 +0.48776%
L18        --          2.4843E-12  --          --          +2.4843E-12 --%
LB1        --          1.26626E-12 --          --          +1.2663E-12 --%
LB2        --          3.93331E-12 --          --          +3.9333E-12 --%
LB3        --          1.90746E-12 --          --          +1.9075E-12 --%
LB4        --          5.3918E-12  --          --          +5.3918E-12 --%
LB5        --          3.7848E-12  --          --          +3.7848E-12 --%
LP1        --          5.10892E-13 --          --          +5.1089E-13 --%
LP2        --          6.02837E-13 --          --          +6.0284E-13 --%
LP3        --          5.97395E-13 --          --          +5.9739E-13 --%
LP4        --          4.67037E-13 --          --          +4.6704E-13 --%
LP6        --          4.99355E-13 --          --          +4.9935E-13 --%
LP8        --          4.69276E-13 --          --          +4.6928E-13 --%
LP10       --          5.0831E-13  --          --          +5.0831E-13 --%
LP11       --          5.23487E-13 --          --          +5.2349E-13 --%

Ports      Design    Extracted AbsDiff   PercDiff
J1         0.0001      0.00010794
J2         0.0001      0.00010794
J3         0.0001      0.00010794
J4         0.000325    0.00033376
J5         0.00015     0.00015829
J6         0.000175    0.00018327
J7         0.0002      0.00020853
J8         0.0003      0.00030903
J9         0.00015     0.00015829
J10        0.00015     0.00015829
J11        0.0002      0.00020853

Error bound on extracted values: 1.65942%

Deallocating memory.
Cycles found in 0.028 seconds.
SVD solution in 0.028 seconds.
Job finished in 393.767 seconds.
```

Listing 4.50: RSFQ PTLRX-SFQDC InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 18 June 2020
* Last modification by: L. Schindler

* Ports                          a q
.subckt LSmitll_PTLRX_SFQDC a q
.model jjmit jj(rtype=1, vg=2.8mV, cap
    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
    ↪ )
B00 103 108 jjmit area=1
B01 104 110 jjmit area=1
B02 105 112 jjmit area=1
I00 0 106 pwl(0 0 5p 155u)
L00 106 107 0.2p
L01 a 103 0.2p
L02 103 107 4.3p
L03 107 104 4.6p
L04 104 105 5p
L05 105 5001 2.3p
L06 108 0 0.34p
L07 109 0 0.5p
L08 110 0 0.06p
L09 111 0 1p
L010 112 0 0.03p
L011 113 0 1p
R00 103 109 6.859904418
R01 104 111 6.859904418
R02 105 113 6.859904418

.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B1=3.25
.param B2=2.00
.param B3=1.50
.param B4=3.00
.param B5=1.75
.param B6=1.50
.param B7=1.50
.param B8=2.00
.param L1=1.522p
.param L3=0.827p
.param L4=1.12884p
.param L5=1.11098p
.param L6=5.940p
.param L7=3.216p
.param L10=0.215p
.param L13=3.699p
.param L17=1.510p
.param L18=2.010p
.param L19=0.954p
.param L4b=0.178p
.param LB1=(RB1/Rsheet)*Lsheet
.param LB2=(RB2/Rsheet)*Lsheet
.param LB3=(RB3/Rsheet)*Lsheet
.param LB4=(RB4/Rsheet)*Lsheet
.param LB5=(RB5/Rsheet)*Lsheet
.param LB6=(RB6/Rsheet)*Lsheet
.param LB7=(RB7/Rsheet)*Lsheet
.param LB8=(RB8/Rsheet)*Lsheet
.param LP1=0.140p
.param LP4=0.524p
.param LP5=0.516p
.param LP7=0.086p
.param LP8=0.226p
.param LR1=0.91p
.param R1=0.375
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param RB5=B0Rs/B5
.param RB6=B0Rs/B6
.param RB7=B0Rs/B7
.param RB8=B0Rs/B8
.param IB1=280u
.param IB2=150u
.param IB3=220u
.param IB4=80u
B1 8 20 jjmit area=B1
B2 12 13 jjmit area=B2
B3 3 4 jjmit area=B3
B4 13 29 jjmit area=B4
B5 5 16 jjmit area=B5
B6 6 7 jjmit area=B6
B7 10 22 jjmit area=B7
B8 11 24 jjmit area=B8
IB1 0 8 pwl(0 0 5p IB1)
IB2 0 4 pwl(0 0 5p IB2)
IB3 0 7 pwl(0 0 5p IB3)
IB4 0 18 pwl(0 0 5p IB4)
L1 5001 8 L1
L3 8 17 L3
L4 3 17 L4
L5 17 12 L5
L6 5 9 L6
L7 9 13 L7
L10 9 6 L10
L13 10 18 L13
L17 11 q L17
L18 18 11 L18
L19 7 10 L19
L4b 4 5 L4b
LB1 8 21 LB1
LB2 12 27 LB2
LB3 3 14 LB3
LB4 13 28 LB4
LB5 5 15 LB5
LB6 6 19 LB6
LB7 10 23 LB7
LB8 11 25 LB8
LP1 20 0 LP1
LP4 29 0 LP4
LP5 16 0 LP5
LP7 22 0 LP7
LP8 24 0 LP8
LR1 9 26 LR1
R1 26 0 R1
RB1 21 0 RB1
RB2 27 13 RB2
RB3 14 4 RB3
RB4 28 0 RB4
RB5 15 0 RB5
RB6 19 7 RB6
RB7 23 0 RB7
RB8 25 0 RB8
.ends
```

Listing 4.51: RSFQ PTLRX-SFQDC JoSIM netlist.

Table 4.33: RSFQ PTLRX-SFQDC pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX-SFQDC using JoSIM is shown in Fig. 4.84. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the output inductor connected to pin **q**, and

(c) the voltage over the load resistor connected to pin **q**.

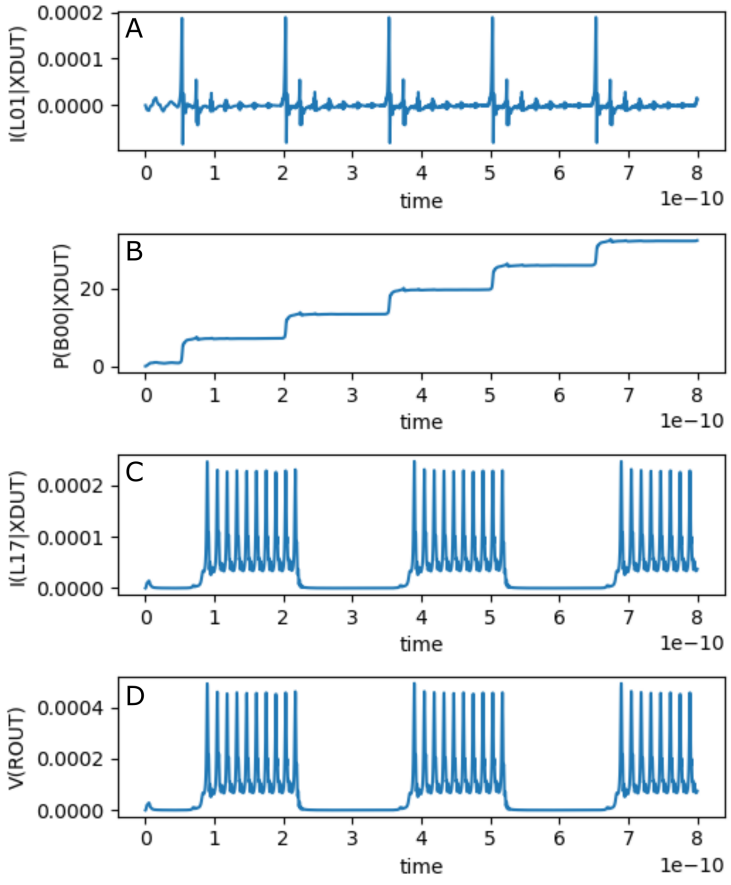

Figure 4.84: RSFQ PTLRX-SFQDC analog simulation results.

4.4.4 SFQDC

The RSFQ SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The SFQDC doen not have an integrated PTL receiver and is not intended to be connected directly to a PTL input.

Schematic

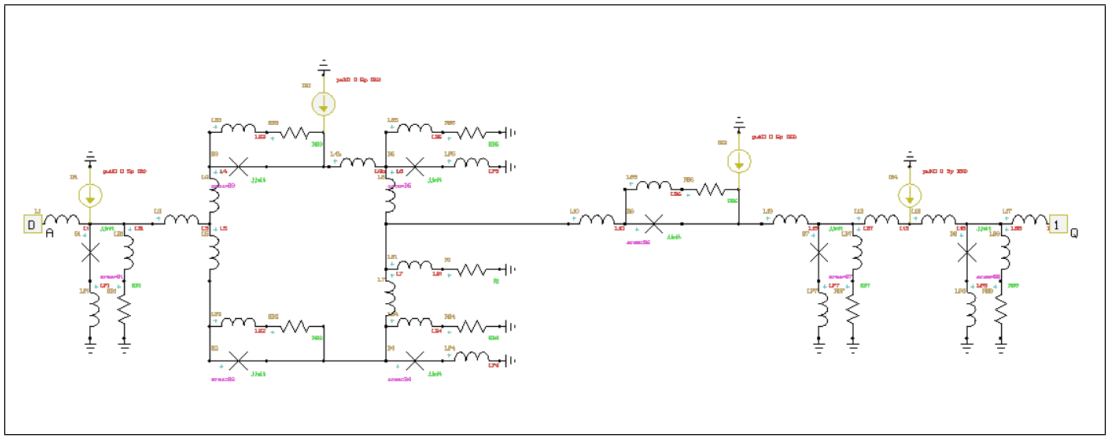

Figure 4.85: Schematic of RSFQ SFQDC.

Layout

The physical layout for the RSFQ SFQDC is shown in Fig. 4.86 and the resulting InductEx extraction is shown in Listing 4.52. The layout height is 70 μm and the width is 60 μm.

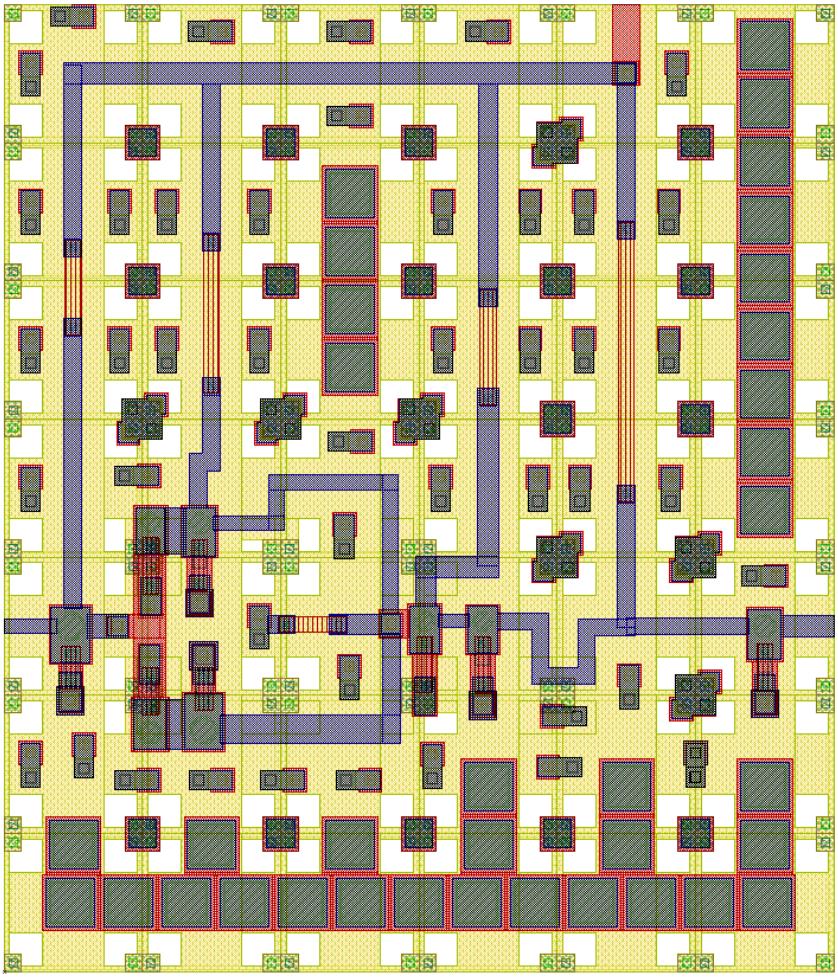

Figure 4.86: RSFQ SFQDC Layout

```
1  InductEx v5.07.48 (19 February 2020). Copyright 2003-2020 Coenrad Fourie
2  Licensed to:
3    SUN Magnetics i9-7940X server, until 31 Dec 2025. [Super with Visualization]
4  LSmitll_SFQDC_v1p5.gds -n LSmitll_SFQDC_v1p5_idx.cir -l mitll_sfq5ee_set2.ldf -th
5  Techfile mitll_sfq5ee_set2.ldf read: Units in 1E-6 m. AbsMin=0.025 SegmentSize=1
6  Spice netlist LSmitll_SFQDC_v1p5_idx.cir read. Totals: L = 21, k = 0, P = 15.
7  Total fundamental loops identified in netlist = 12
8  Using TetraHenry with analytical integration.
9  1715 structures read. Reduced 1715 objects to 1577 polygons and 7 terminals.
10 Top level structure is "LSMITLL_SFQDC1".
11 GDS file LSmitll_SFQDC_v1p5.gds read: db units in 1E-9 m, 0.001 units per user unit.
12 Object in layer I5 moved to TERM layer. (Pj1)
13 Object in layer I5 moved to TERM layer. (Pj2)
14 Object in layer I5 moved to TERM layer. (Pj3)
15 Object in layer I5 moved to TERM layer. (Pj4)
16 Object in layer I5 moved to TERM layer. (Pj5)
17 Object in layer I5 moved to TERM layer. (Pj6)
18 Object in layer I5 moved to TERM layer. (Pj7)
19 Object in layer I5 moved to TERM layer. (Pj8)
20 Terminal blocks = 15; Labels = 15; Extracted Ports = 15
```

```
21
22 Port                  Positive terminal    Negative terminal
23 P1                    M6,   line along y;  M4,   same as "+" terminal.
24 P2                    M6,   polygon;       M4,   same as "+" terminal.
25 P3                    M6,   polygon;       M4,   same as "+" terminal.
26 P4                    M6,   polygon;       M4,   same as "+" terminal.
27 P5                    M6,   polygon;       M4,   same as "+" terminal.
28 P6                    M6,   polygon;       M4,   same as "+" terminal.
29 P7                    M6,   line along y;  M4,   same as "+" terminal.
30 J1                    M6,   polygon;       M5,   same as "+" terminal.
31 J2                    M5,   polygon;       M6,   same as "+" terminal.
32 J3                    M5,   polygon;       M6,   same as "+" terminal.
33 J4                    M6,   polygon;       M5,   same as "+" terminal.
34 J5                    M6,   polygon;       M5,   same as "+" terminal.
35 J6                    M5,   polygon;       M6,   same as "+" terminal.
36 J7                    M6,   polygon;       M5,   same as "+" terminal.
37 J8                    M6,   polygon;       M5,   same as "+" terminal.
38
39 SVD info: Condition nr. = 6.634; unknowns = 42; rank = 42.
40
41 Impedance     Inductance [H]        Resistance [Ohm]      AbsDiff     PercDiff
42 Name       Design      Extracted   Design      Extracted   (L only)    (L only)
43 L1         1.522E-12   1.41237E-12 --          --          -1.0963E-13 -7.2029%
44 L3         8.27E-13    9.13884E-13 --          --          +8.6884E-14 +10.506%
45 L4         1.12884E-12 1.2865E-12  --          --          +1.5766E-13 +13.967%
46 L5         1.11098E-12 1.31119E-12 --          --          +2.0021E-13 +18.021%
47 L5B        3.216E-12   3.31349E-12 --          --          +9.7492E-14 +3.0315%
48 L6         5.94E-12    5.80096E-12 --          --          -1.3904E-13 -2.3407%
49 L10        2.15E-13    4.43293E-13 --          --          +2.2829E-13 +106.18%
50 L19        9.54E-13    7.57432E-13 --          --          -1.9657E-13 -20.605%
51 L13        3.699E-12   3.47827E-12 --          --          -2.2073E-13 -5.9674%
52 L18        2.01E-12    2.08681E-12 --          --          +7.6812E-14 +3.8215%
53 L17        1.51E-12    1.22092E-12 --          --          -2.8908E-13 -19.144%
54 LR1        9.1E-13     9.09181E-13 --          --          -8.1939E-16 -0.090042%
55 LB1        --          4.77388E-12 --          --          +4.7739E-12 --%
56 LB2        --          2.20374E-12 --          --          +2.2037E-12 --%
57 LB3        --          3.68595E-12 --          --          +3.686E-12  --%
58 LB4        --          2.08951E-12 --          --          +2.0895E-12 --%
59 LP1        --          3.69143E-13 --          --          +3.6914E-13 --%
60 LP4        --          4.10393E-13 --          --          +4.1039E-13 --%
61 LP5        --          4.92418E-13 --          --          +4.9242E-13 --%
62 LP7        --          5.08136E-13 --          --          +5.0814E-13 --%
63 LP8        --          4.00262E-13 --          --          +4.0026E-13 --%
64
65 Ports      Design    Extracted AbsDiff   PercDiff
66 J1         0.000325    0.00033376
67 J2         0.0002      0.00020853
68 J3         0.00015     0.00015829
69 J4         0.0003      0.00030903
70 J5         0.000175    0.00018327
71 J6         0.00015     0.00015829
72 J7         0.00015     0.00015829
73 J8         0.0002      0.00020853
74
75 Error bound on extracted values: 5.15319%
76
77 Deallocating memory.
78 Cycles found in 0.028 seconds.
79 SVD solution in 0.015 seconds.
80 Job finished in 199.026 seconds.
```

Listing 4.52: RSFQ SFQDC InductEx extraction.

Analog model

```
* Author: L. Schindler
* Version: 1.5.1
* Last modification date: 25 June 2020
* Last modification by: L. Schindler

*$ports         a       q
.subckt LSmitll_SFQDC a q
.model jjmit jj(rtype=1, vg=2.8mV, cap
    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
    ↪ )
.param B0=1
.param Ic0=0.0001
.param IcRs=100u*6.859904418
.param B0Rs=IcRs/Ic0*B0
.param Rsheet=2
.param Lsheet=1.13e-12
.param B1=3.25
.param B2=2.00
.param B3=1.50
.param B4=3.00
.param B5=1.75
.param B6=1.50
.param B7=1.50
.param B8=2.00
.param L1=1.522p
.param L3=0.827p
.param L4=1.12884p
.param L5=1.11098p
.param L6=5.940p
.param L7=3.216p
.param L10=0.215p
.param L13=3.699p
.param L17=1.510p
.param L18=2.010p
.param L19=0.954p
.param L4b=0.178p
.param LB1=(RB1/Rsheet)*Lsheet
.param LB2=(RB2/Rsheet)*Lsheet
.param LB3=(RB3/Rsheet)*Lsheet
.param LB4=(RB4/Rsheet)*Lsheet
.param LB5=(RB5/Rsheet)*Lsheet
.param LB6=(RB6/Rsheet)*Lsheet
.param LB7=(RB7/Rsheet)*Lsheet
.param LB8=(RB8/Rsheet)*Lsheet
.param LP1=0.140p
.param LP4=0.524p
.param LP5=0.516p
.param LP7=0.086p
.param LP8=0.226p
.param LR1=0.91p
.param R1=0.375
.param RB1=B0Rs/B1
.param RB2=B0Rs/B2
.param RB3=B0Rs/B3
.param RB4=B0Rs/B4
.param RB5=B0Rs/B5
.param RB6=B0Rs/B6
.param RB7=B0Rs/B7
.param RB8=B0Rs/B8
.param IB1=280u
.param IB2=150u
.param IB3=220u
.param IB4=80u
B1 8 20 jjmit area=B1
B2 12 13 jjmit area=B2
B3 3 4 jjmit area=B3
B4 13 29 jjmit area=B4
B5 5 16 jjmit area=B5
B6 6 7 jjmit area=B6
B7 10 22 jjmit area=B7
B8 11 24 jjmit area=B8
IB1 0 8 pwl(0 0 5p IB1)
IB2 0 4 pwl(0 0 5p IB2)
IB3 0 7 pwl(0 0 5p IB3)
IB4 0 18 pwl(0 0 5p IB4)
L1 a 8 L1
L3 8 17 L3
L4 3 17 L4
L5 17 12 L5
L6 5 9 L6
L7 9 13 L7
L10 9 6 L10
L13 10 18 L13
L17 11 q L17
L18 18 11 L18
L19 7 10 L19
L4b 4 5 L4b
LB1 8 21 LB1
LB2 12 27 LB2
LB3 3 14 LB3
LB4 13 28 LB4
LB5 5 15 LB5
LB6 6 19 LB6
LB7 10 23 LB7
LB8 11 25 LB8
LP1 20 0 LP1
LP4 29 0 LP4
LP5 16 0 LP5
LP7 22 0 LP7
LP8 24 0 LP8
LR1 9 26 LR1
R1 26 0 R1
RB1 21 0 RB1
RB2 27 13 RB2
RB3 14 4 RB3
RB4 28 0 RB4
RB5 15 0 RB5
RB6 19 7 RB6
RB7 23 0 RB7
RB8 25 0 RB8
.ends
```

Listing 4.53: RSFQ SFQDC JoSIM netlist.

Table 4.34: RSFQ SFQDC pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ SFQDC using JoSIM is shown in Fig. 4.87. The figure shows the graph for:

(a) the current through the input inductor connected to pin **a**,

(b) the phase over the input JJ of pin **a**,

(c) the current through the output inductor connected to pin **q**, and

(c) the voltage over the load resistor connected to pin **q**.

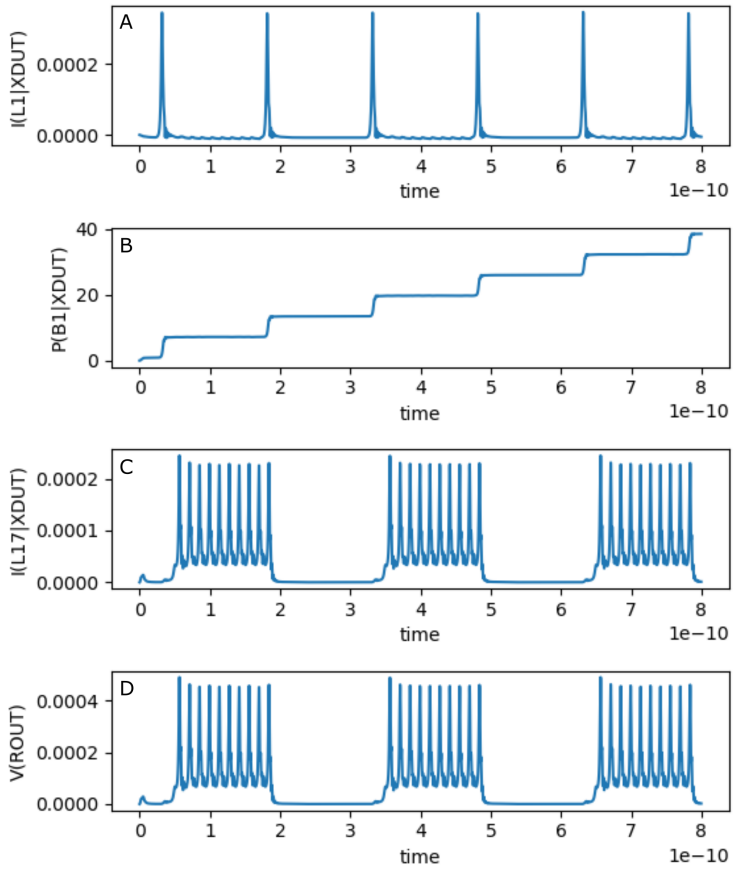

Figure 4.87: RSFQ SFQDC analog simulation results.

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